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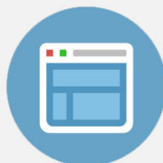

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Characteristics and stress-induced degradation of laser-activated low temperature polycrystalline silicon thin-film transistors

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The characteristics and reliability of laser-activated polycrystalline silicon thin-film transistors (poly-Si TFTs) under the stress condition of drain voltage $(V_d)=12$ V and gate voltage $(V_g)=15$ V have been investigated. In spite of reducing the source/drain resistivity by using laser activation method, the leakage current $(V_g<0)$ is larger for laser-activated poly-Si TFTs in comparison with traditional furnace-activated counterparts. It is also found that the post-stress leakage and on/off current ratio degrade much faster for laser-activated poly-Si TFTs, while the degradation rates of threshold voltage and subthreshold swing are comparable to those of traditional furnace-activated TFTs. The laser activation modifies the grain structure between drain and channel region and causes grain discontinuity extending from the drain side to the channel region. The grain discontinuity near drain side in the polysilicon film has been investigated by transmission electron microscopy analysis. The effective trap state density calculated from typical $I-V$ curve has been compared for laser-activated and furnace-activated TFTs. As a result, an inferior reliability with extra trap state density and larger leakage current was observed in the laser-activated poly-Si TFTs.
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I. INTRODUCTION

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been extensively investigated for applications in large-area electronics, especially for switching devices or peripheral driving circuits in the active matrix liquid crystal display (AMLCD).[1,2] In order to realize low-cost AMLCD with integrated peripheral circuits, it is essential to reduce the maximum process temperature for high-performance TFTs. The low process temperature would reduce manufacturing costs by allowing use of inexpensive glass substrates such as Corning 7059 or even plastic substrates (e.g., PET)[3] rather than quartz substrates. To crystallize the amorphous-Si channel film, the traditional TFT process typically uses a top gate self-aligned TFT architecture with a solid phase crystallization (SPC)[4,5] or a laser crystallization (LC) method.[6–9] The SPC usually requires a high temperature annealing, typically 600 °C for several hours, and results in smaller grain size in the channel film, compared to that for LC method. In contrast, the LC technique not only obtains larger grain size but features a low temperature process, which is suitable for AMLCD application. However, the activation after source/drain implantation still needs a high temperature annealing,[10] generally 600 °C for several hours in nitrogen ambient, which is inefficient for low temperature consideration. For very low temperature processes on glass substrates or plastic substrates, the laser activation after self-aligned implantation or gas immersion laser doping (GILD) method replaces the furnace activation step to reduce the maximum process temperature.[11] The self-aligned GILD method uses laser to simultaneously incorporate and activate the dopant in source and drain region. Excimer laser activation reduces not only the postannealing temperature but also the resistivity of source and drain regions, which helps improve device turn-on characteristics compared to traditional furnace activation. Therefore, it is also essential to investigate the correlations between the grain structures near drain side and $I-V$ characteristics for the reliability consideration of laser-activated TFTs.

The research purpose of the present paper is to compare the $I-V$ characteristics of poly-Si TFTs between using laser activation (LA) and traditional furnace activation (FA) for SPC and LC TFTs. In addition, the physical mechanism on the reliability of both poly-Si TFTs is studied comprehensively by using electrical and material analysis. Even if laser activation can effectively reduce the source/drain resistivity, it is found that laser activation results in larger leakage current and poorer reliability for LC TFTs, which is considered to be due to extra trap state density generated near the drain side during laser activation. Although no GILD is used in our experiment, we believe that similar results are expected for the GILD method, which needs to be carefully taken into

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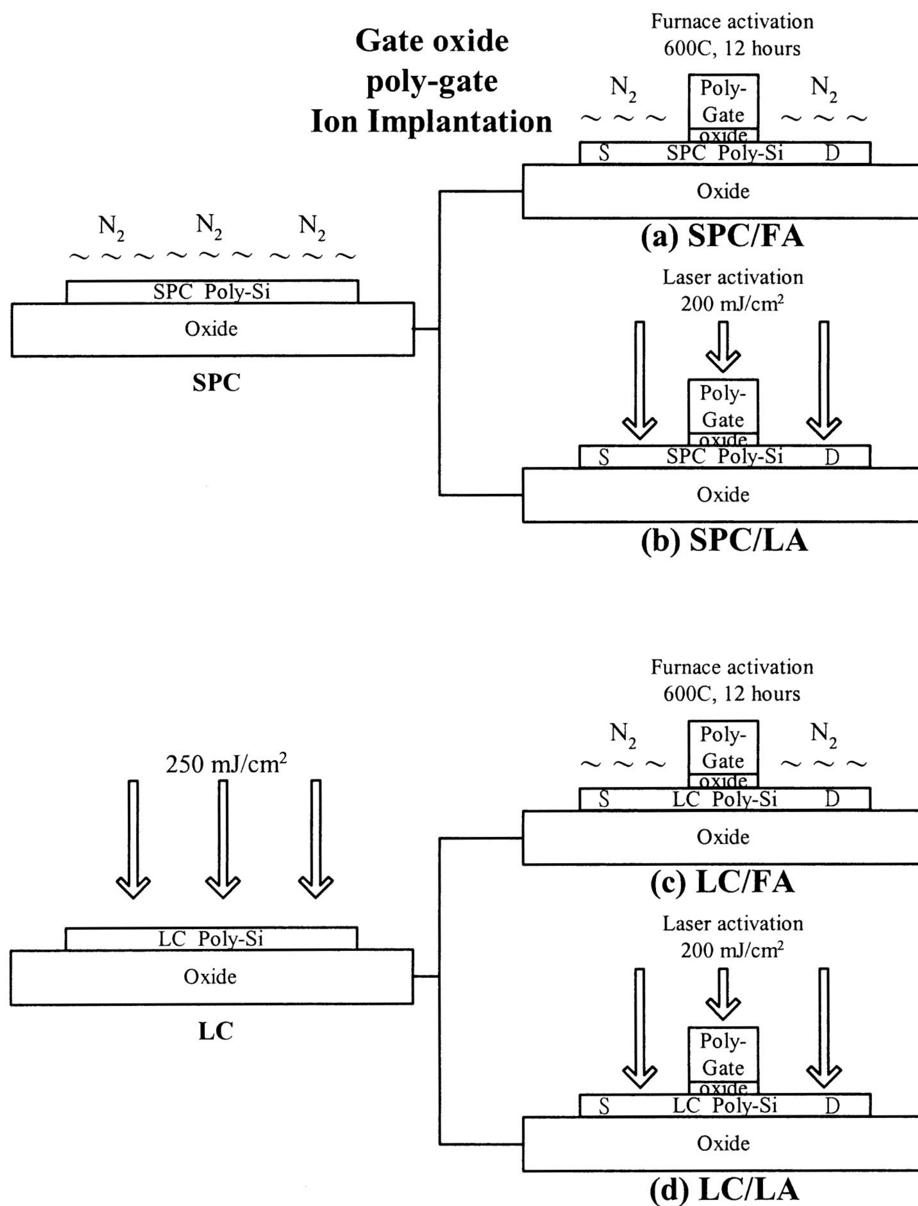

FIG. 1. Key process steps with cross-sectional schematic for four different poly-Si TFTs, (a) solid phase crystallization channel and furnace activation (SPC/FA), (b) solid phase crystallization channel and laser activation (SPC/LA), (c) laser crystallized channel and furnace activation (LC/FA), and (d) laser crystallized channel and laser activation (LC/LA).

consideration for future low temperature poly-Si TFTs fabricated on plastic substrates.

II. EXPERIMENTS

In this work, four different TFTs have been fabricated to compare their device performances such as leakage current and stability, which may help analyze how the laser activation (LA) affects device characteristics. Figure 1 depicts the key process for the four different TFTs, the major differences between these devices are channel film crystallization and post-implant activation. Silicon wafers coated with a 500 nm thermal oxide were used as the starting substrates. An 80 nm undoped amorphous-Si (*a*-Si) layer was deposited by low-pressure chemical vapor deposition at 550 °C. The deposited *a*-Si layer was then crystallized by solid phase crystallization (SPC) method in furnace at 600 °C for 24 h. After patterning and wet etching to form the active device island, a 50 nm gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) method. This was followed by the deposition and patterning of a 300 nm poly-Si gate layer. The gate electrode and source/drain regions were implanted by phosphorus ions at a dosage of $5\times10^{15}\,\mathrm{cm}^{-2}$, and an energy of 35 keV. Some of the wafers were then subjected to furnace activation (FA) at 600 °C in nitrogen ambient for 12 h, which is denoted as SPC/FA as shown in Fig. 1(a). The other wafers were activated by laser activation (LA) at room temperature. The laser for dopant activation was performed at an energy density of $200\,\mathrm{mJ/cm}^2$, denoted as SPC/LA as shown in Fig. 1(b). Next, a 300-nm-thick oxide was formed as the cap layer by PECVD. Finally, contact hole definition and Al metallization were performed, followed by a 400 °C sintering in nitrogen ambient for 30 min.

For comparison, wafers with channel film crystallized by laser crystallization (LC) method were also processed on the same run. The applied laser energy density for crystallization is $250\,\mathrm{mJ/cm}^2$. After self-aligned ion implantation, some wafers were furnace activated, denoted as LC/FA as shown in Fig. 1(c). The others were laser-activated, denoted as LC/LA

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TABLE I. Key parameters for four different poly-Si TFTs. All parameters are extracted at $V_d = 0.1$ V except for on/off current ratio, which is evaluated at $V_d = 5$ V . (a), (b), (c), and (d) are associated with TFT structures shown in Fig. 1

	Threshold voltage (V)	Subthreshold swing (V/decade)	Mobility (cm^2/V s)	On/off current ratio ($\times 10^6$)	Source/drain resistivity (mΩ cm)
(a) SPC/FA	3.8	1.25	30	1.18	3.5
(b) SPC/LA	4.7	1.32	30	0.79	1.06
(c) LC/FA	2.6	0.8	32	2.96	2.43
(d) LC/LA	3	0.92	35	1.53	1.41

as shown in Fig. 1(d). The activation conditions were the same as those for SPC TFTs. The measured resistivities were 1.41 and 2.43 mΩ cm for LC/LA and LC/FA TFTs, respectively, indicating that a significant reduction in source/drain resistance was indeed obtained by using laser activation method. The resistivities were measured by four point probe equipment after dopant activation for source and drain regions. Similar results were found for SPC/LA and SPC/FA TFTs. The measured resistivities were 1.06 and 3.5 mΩ cm for SPC/LA and SPC/FA TFTs, respectively, as listed in Table I.

III. RESULTS AND DISCUSSION

A. Characteristics

Figures 2(a) and 2(b) show the cross-sectional transmission electron microphotograph (TEM) photos of SPC and LC poly-Si films, respectively. We can see that the grains in LC film are generally larger and presenting the columnar grain structure compared to those for SPC films, which are random grain structure. Figure 3 shows the experimental $I_d - V_g$ characteristics of the LC/LA and LC/FA TFTs. It can be seen from Fig. 3 that the leakage current ($V_g < 0$) is obviously larger for LC/LA TFTs, and there is only slight difference for turn-on characteristics such as threshold voltage and subthreshold swing. Note also that there is not much difference on turn-on current for both LC/LA and LC/FA TFTs. Some of the parameters are summarized in Table I. Leakage current is generally attributed to the electric field and the number of trap state density near drain side.[12–14] Under the identical electric field applied in both LC/LA and LC/FA TFTs, a higher leakage current suggests that there is more trap state density near drain side for LC/LA TFTs. The insert plot of Fig. 3 shows the effective trap state density (N_t), extracted from the following equation[15] for LC/LA and LC/FA TFTs;

$$I_d = \left(\frac{W}{L}\right) C_{ox}(V_g - V_{fb}) V_d \mu \times \exp\left(\frac{-q^2 N_t^2 t_{ox}}{\sqrt{\varepsilon_{Si}\varepsilon_{SiO_2}} C_{ox}(V_g - V_{fb})^2}\right), \quad (1)$$

where V_{fb} is the flat band voltage of the device, and ε_{Si} and ε_{Sio_2} are the dielectric constant for silicon and gate oxide, respectively. C_{ox} and t_{ox} and are the gate oxide capacitance and thickness, respectively. We can see from Eq. (1) that the slope of $\ln[I_d/(V_g - V_{fb})]$ vs $(V_g - V_{fb})^{-2}$ gives N_t. A larger slope indicates a larger effective trap state density. As can be seen in the insert of Fig. 3, the effective trap state density for LC/LA TFTs and LC/FA TFTs are 11.9 and 9.6 $\times 10^{12}$ cm^{-2}, respectively. Figures 4(a) and 4(b) are the cross-sectional TEM photos of TFTs for LC/LA and LC/FA, respectively. It can be seen from Fig. 4(a) that there is modification on the grain structures extending from drain side to channel region. During laser activation, the drain region is exposed to laser beam while the channel region is shielded from the laser beam because of the thick poly-gate on top. While the drain is molten, the channel region remains relatively "cool." There exists a lateral temperature gradient and the lateral growth of the grain therefore results from the

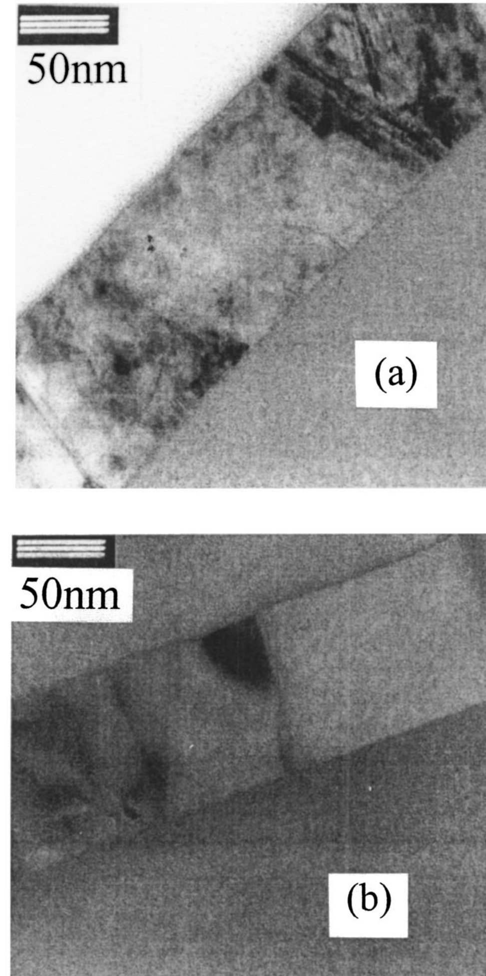

FIG. 2. Transmission electron microphotograph (TEM) for (a) SPC channel film, (b) LC channel film.

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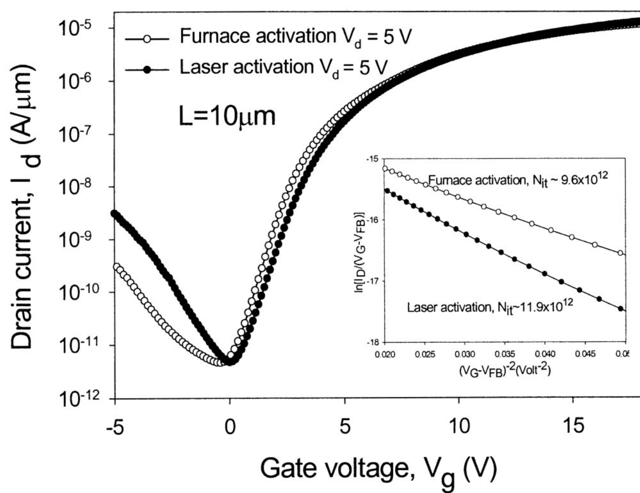

FIG. 3. Comparison of $I_d - V_g$ characteristics of LC/FA and LC/LA poly-Si TFTs. The leakage current is larger for LC/LA TFT. The insert plot compares the effective trap state density for LC/FA and LC/FA poly-Si TFTs, and the larger slope indicates more effective trap state density.

''cool'' channel region stretching out to the molten drain region,[16] as shown in Fig. 4(a). The discontinuity of the grain structure from drain to channel may therefore result in extra trap state density. For comparison, we have shown in Fig. 4(b) the LC/FA TFTs, for which we do not find similar results. From Fig. 3, the insert of Fig. 3, and Fig. 4, we suggest that the extra trap state density is near drain side and is caused by laser activation.

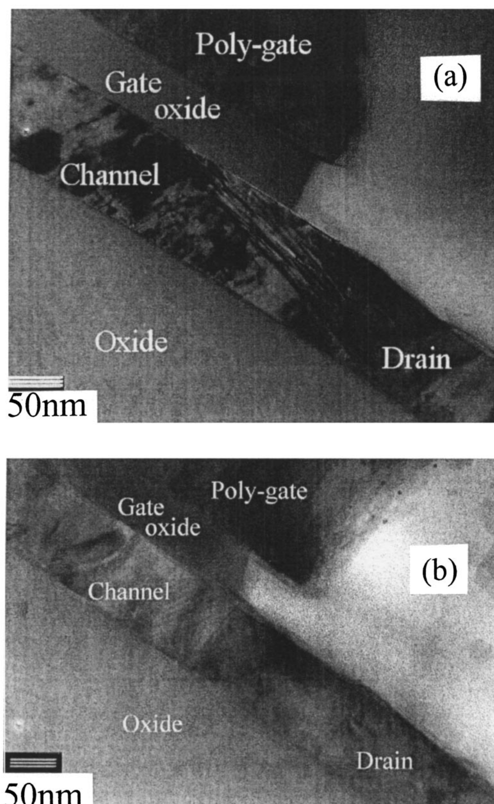

FIG. 4. Cross-sectional TEM of (a) LC/LA TFTs and (b) LC/FA TFTs. Note the lateral growth of grain structure near drain side for LC/LA TFTs.

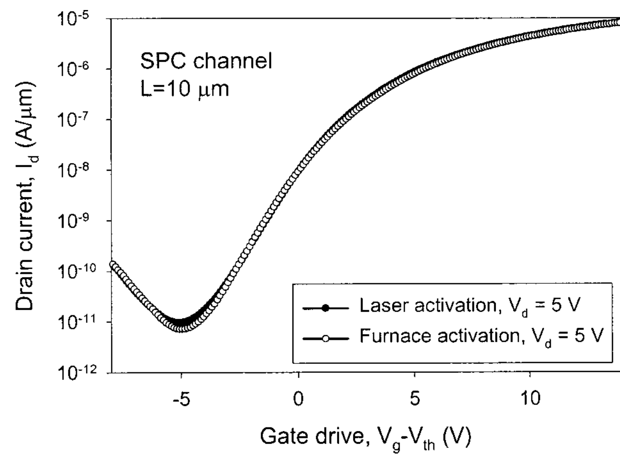

FIG. 5. Comparison of $I_d - V_g$ characteristics of SPC/FA and SPC/LA poly-Si TFTs. The leakage current is almost the same for the two TFTs with the same gate drive.

This phenomenon, however, seemed not so obvious for SPC TFTs. Figure 5 shows the comparison of $I_d - V_g$ curves between SPC/LA and SPC/FA TFTs. It can be seen that, unlike Fig. 3, as V_g becomes more negative, only slight difference on leakage current could be found for SPC/LA and SPC/FA TFTs, as shown in Fig. 5. From Figs. 3 and 5, we conclude that as SPC channel film was used, the deviation of leakage current was not obvious, compared to that of LC channel film, for either LA or FA applied for post-implant activation. The reason for the minor difference of leakage current obtained by using SPC channel film might be due to the smaller grain size in the film. In LC channel film, the LA process caused smaller and lateral growth of grain near drain side as shown in Fig. 4(a), which resulted in extra trap state density. However, in SPC film, the grain size was inherently small and randomly distributed. After LA process, the size of regrown grain near the drain side was comparable to the original grain. Therefore, the effect of extra trap density, and hence the increase of leakage current was not significant after LA process for SPC film.

B. Reliability

Figures 6(a) and 6(b) depict the variations of typical $I_d - V_g$ curves ($V_d = 5$ V) after dc stress for LC/LA and LC/FA TFTs, respectively. The stress condition was chosen from the output characteristic when kink effect occurs, i.e., $V_d = 12$ V and $V_g = 15$ V. The interval of stress time was 30 min starting from 10 min to 190 min. It can be seen that after stress, while there is not much degradation on leakage current for LC/FA TFTs, much degradation is observed with stress time for LC/LA TFTs. The turn-on current however, has little degradation after stress for both LC/LA and LC/FA TFTs. Figure 7 shows the degradation rate of the on/off current ratio for both devices. The aggravated degradation of the on/off ratio is due to the increased leakage current for LC/LA TFTs. For comparison, we have also stressed the SPC/LA and SPC/FA TFTs with the same dc stress condition. Figures 8(a) and 8(b) show the results after stress for SPC/LA and SPC/FA TFTs, respectively. From Fig. 8, we found that not much variation on leakage current for either SPC/LA or

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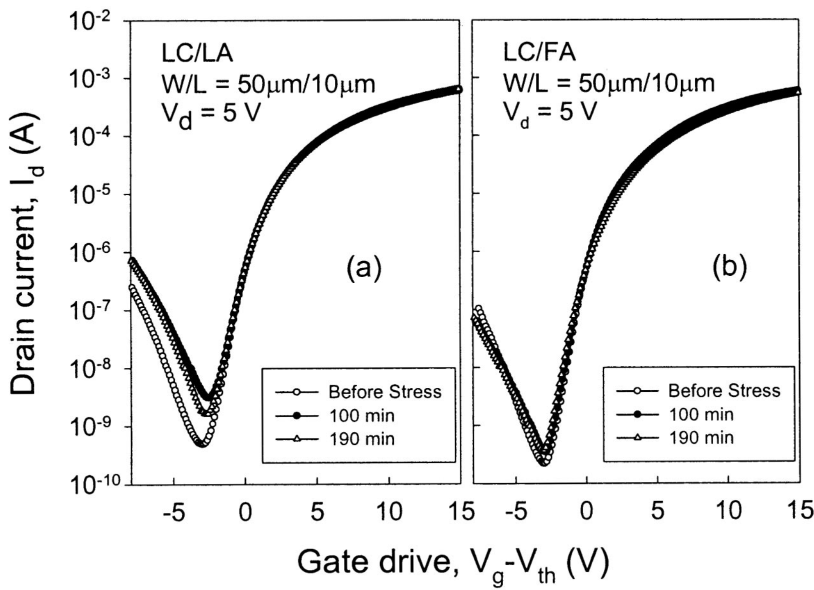

FIG. 6. The variations of $I_d - V_g$ curves after dc stress for (a) LC/LA and (b) LC/FA poly-Si TFTs. The stress condition is $V_{ds} = 12$ V and $V_{gs} = 15$ V. Note that only three measured time intervals were shown here for 0, 100, and 190 min.

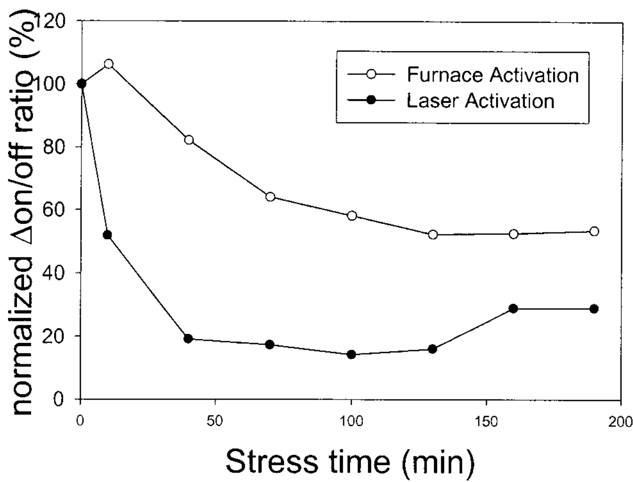

FIG. 7. Difference of variation on on/off current ratio for LC/LA and LC/FA poly-Si TFTs. The stress time started at 10 to 190 min with 30 minute time intervals.

SPC/FA TFTs could be obtained compared to the LC/LA in Fig. 6(a). The result is consistent with what was described previously—that laser activation has little effect on producing the extra trap density for SPC film.

The extra trap state density near drain side caused by laser activation in LC/LA TFTs result in accelerated degradation during stress. As a result, even more trap state density is generated near the drain side. To support this argument, we also consider two other parameters, i.e., threshold voltage (V_{th}) and subthreshold swing (SS). Figures 9 and 10 show the degradation rate of V_{th} and SS after dc stress for LC/LA and LC/FA TFTs, respectively. It is interesting to note that there is no dramatic difference in degradation rate for V_{th} and SS between both LC/LA and LC/FA TFTs. This indicates that under this stress condition, the extra trap density caused by laser activation has little impact on channel and channel/oxide interface. Therefore, this is consistent with our inference that the extra trap density after laser activation results in

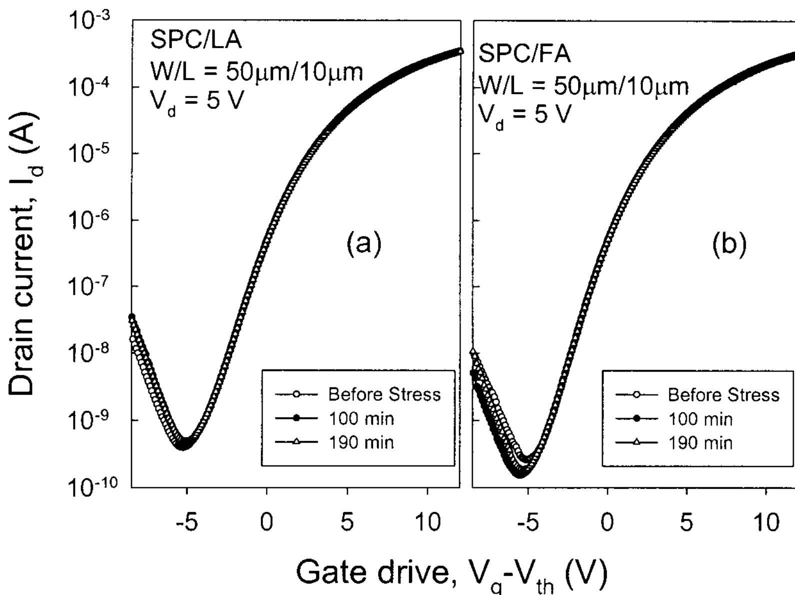

FIG. 8. The variations of $I_d - V_g$ curves after dc stress for (a) SPC/LA and (b) SPC/FA poly-Si TFTs. The stress condition is $V_{ds} = 12$ V and $V_{gs} = 15$ V. Only three measured time intervals were shown here for 0, 100, and 190 min.

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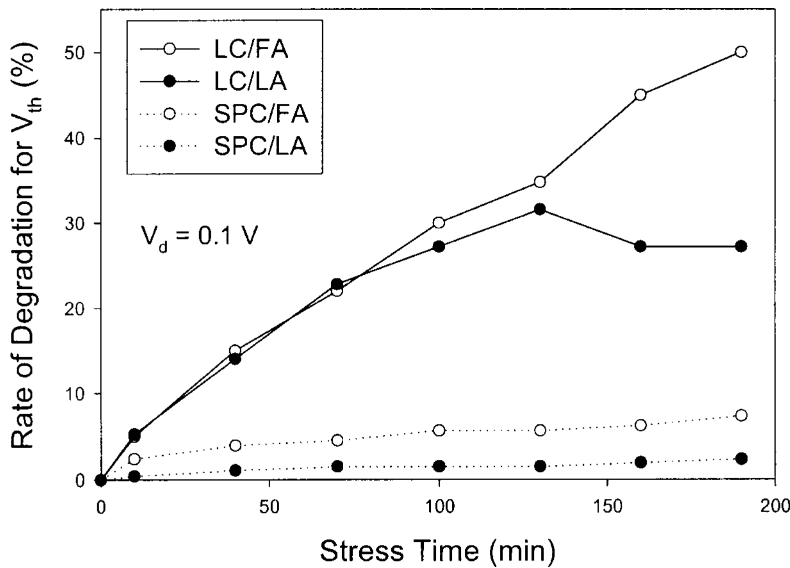

FIG. 9. Comparison of degradation rate of threshold votage (V_{th}) after dc stress for LC/LA and LC/FA poly-Si TFTs (solid lines) as well as for SPC/LA and SPC/FA poly-Si TFTs (dotted lines).

more trap density only near drain side after stress and affects device degradation such as increased leakage current. The shifts of V_{th} and SS after dc stress for SPC TFTs are also included in Figs. 9 and 10, respectively. In comparison with LC TFTs, the degradations for SPC TFTs are quite smaller. This is due to the fact that under the same stress condition, the stress current for LC TFTs is about two times larger than that for SPC TFTs from their output characteristics, which results in severe degradation for LC TFTs. Note also that there is little deviation on V_{th} and SS shift for SPC/FA and SPC/LA TFTs. We therefore summarize that for SPC TFTs, the degradation and hence reliability is similar for either LA or FA. For LC TFTs, although the degradation of V_{th} and SS behave quite the same, LA generates more extra trap state near drain side as compared to FA, which would cause reliability problems for long-term consideration.

IV. CONCLUSION

We have examined the characteristics and the reliability of the laser-involved activation for both SPC and LC channel films. Laser activation has the advantage of decreasing the maximum process temperature and reducing the resistivity of source/drain region. However, experimental results also reveal that after laser activation, leakage current will become larger and more trap state density will be generated near drain side especially for LC channel films. This may cause a reliability problem for long-term consideration. Although the gas immersion laser doping method (GILD) is not used in our work, we believe that similar results are expected for the GILD method, which needs to be carefully taken into consideration for future low temperature poly-Si TFTs fabricated on plastic substrates.

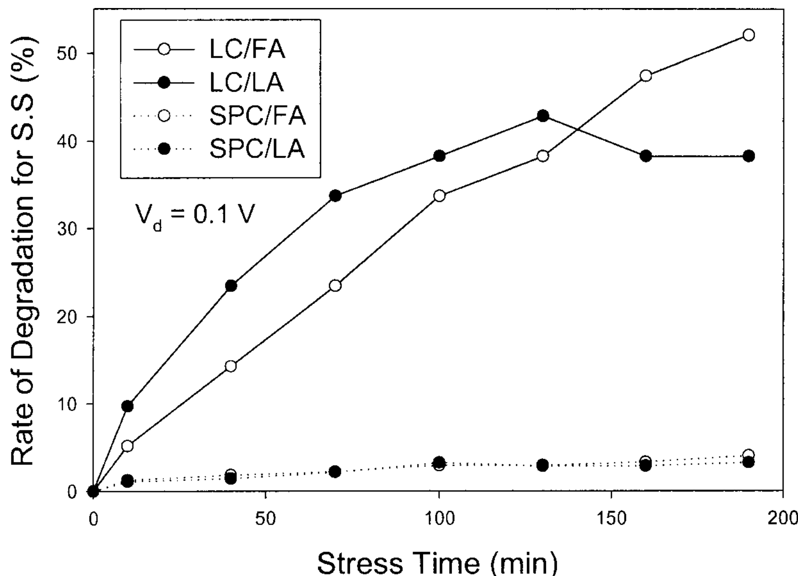

FIG. 10. Comparison of degradation rate of subthreshold swing (SS) after dc stress for LC/LA and LC/FA poly-Si TFTs (solid lines) as well as SPC/LA and SPC/FA poly-Si TFTs (dotted lines).

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