Substrate-Triggered SCR Device for On-Chip ESD Protection in Fully Silicided Sub-0.25-μm CMOS Process

Ming-Dou Ker, *Senior Member, IEEE,* and Kuo-Chun Hsu, *Student Member, IEEE*

***Abstract*—The turn-on mechanism of a silicon-controlled rectifier (SCR) device is essentially a current triggering event. While a current is applied to the base or substrate of the SCR device, it can be quickly triggered into its latching state. In this paper, a novel design concept to turn on the SCR device by applying the substrate-triggered technique is first proposed for effective on-chip electrostatic discharge (ESD) protection. This novel substrate-triggered SCR device has the advantages of controllable switching voltage and adjustable holding voltage and is compatible with general CMOS processes without extra process modification such as the silicide-blocking mask and ESD implantation. Moreover, the substrate-triggered SCR devices can be stacked in ESD protection circuits to avoid the transient-induced latch-up issue. The turn-on time of the proposed substrate-triggered SCR devices can be reduced from 27.4 to 7.8 ns by the substrate-triggering technique. The substrate-triggered SCR device with a small active area of only 20 μm $\times$ 20 μm can sustain the HBM ESD stress of 6.5 kV in a fully silicided 0.25-μm CMOS process.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, silicon controlled rectifier (SCR), substrate-triggered technique.**

I. Introduction

ELECTROSTATIC discharge (ESD) failure has become a main reliability concern in ULSI products, especially in the scaled-down CMOS technologies. To provide whole-chip ESD protection for CMOS ICs, the on-chip ESD protection circuits have to be placed around the input, output, and power pads. The lateral silicon-controlled rectifier (LSCR) device was therefore used in the input (or output) ESD protection circuits to protect the CMOS IC against ESD damage [1]–[6]. Due to the low holding voltage ($Vhold$, about $\sim$1 V in general CMOS processes) of the SCR device, the power dissipation (power $\cong I_{\rm ESD} \times Vhold$) located on the SCR device during ESD stress is less than that located on other ESD protection devices (such as the diode, MOS, BJT, or field-oxide device). So, the SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs. However, the SCR device still has a higher switching voltage ($\sim$20 V) in subquarter-micrometer CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stages. Therefore, the SCR device needs the additional secondary protection circuit to perform the overall ESD protection function [2]. To provide more effective on-chip ESD protection, the modified lateral SCR (MLSCR) [3] and the low-voltage-trigger SCR (LVTSCR) [4], [5] were invented to reduce the switching voltage of the SCR device. Moreover, some advanced circuit techniques were also reported to enhance the turn-on speed of ESD protection devices, such as the gate-coupled technique [6], the substrate-triggered technique [7], [8], and the GGNMOS-triggered technique [9].

In this paper, the novel substrate-triggered SCR (STSCR) device having the ability of controllable switching voltage is proposed, which is compatible with general CMOS processes without extra process modification. Furthermore, the STSCR devices in stacked configuration have the advantage of adjustable holding voltage, so the ESD protection circuit with stacked STSCR devices can be designed free of the latch-up issue. Such stacked STSCR devices are designed to be kept off during the normal circuit operating conditions and to be quickly triggered on by a substrate-triggered technique during the ESD zapping conditions. The on-chip ESD protection circuits designed with such stacked STSCR devices for input pads, output pads, and power rails have been successfully verified in a 0.25-μm salicided CMOS process [10].

II. Novel STSCR Device

The switching voltage of an LVTSCR device [4] relies on the drain breakdown voltage of the inserted NMOS, which is about $\sim$8 V in the 0.25-μm CMOS process. Under ESD stress, the LVTSCR is triggered on by the current generated from the drain avalanche breakdown of the inserted NMOS. On the moment of ESD energy discharging, some electrons or holes from the ESD current of several amperes near the drain side might be injected into the gate oxide of the NMOS [11], [12]. Therefore, for LVTSCRs, the issue that ESD charges may be injected into the thinner gate oxide of the inserted NMOS in subquarter-micrometer CMOS processes must be well controlled.

Based on the above discussion, the ESD protection circuits designed with a LVTSCR might have the reliability issue if the ESD event is frequent and the gate oxide becomes much thinner. In this work, the STSCR device with lower switching voltage and higher ESD robustness is proposed, which has no gate-oxide reliability issue under low-level ESD zaps. The device structure of the proposed STSCR device is shown in Fig. 1, where the

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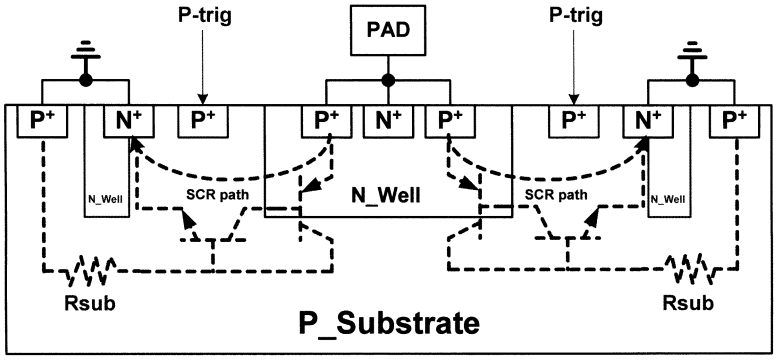
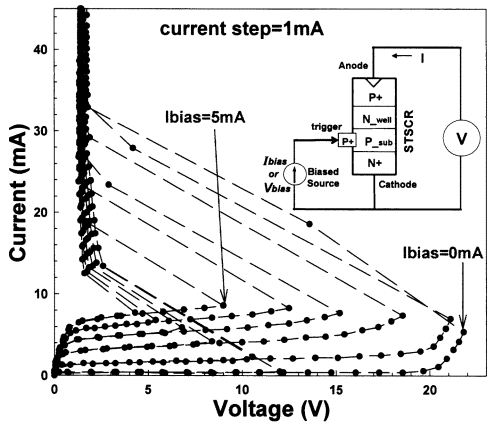


Fig. 1. Device structure of the proposed STSCR device.

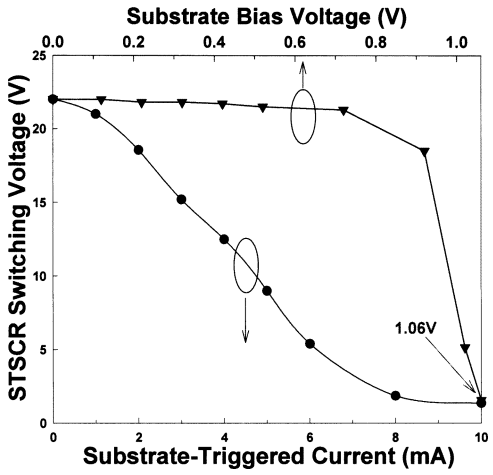
SCR current paths are indicated by the dashed lines. As compared to the traditional LSCR device structure [1], the extra P+ diffusions are inserted into the STSCR device structure. The inserted P+ diffusions are connected out as the trigger node of the STSCR device. When a trigger current is applied into this trigger node, the STSCR will be triggered into its latching state. The additional N-well regions under the cathode (N+ diffusion) of the STSCR device is used to further enhance the turn-on speed of the STSCR for more effective ESD protection, because they increase the equivalent substrate resistance $(Rsub)$.

Such an STSCR device has been fabricated in a 0.25-μm salicided CMOS process. The I–V curves of the STSCR device under various substrate-triggered currents are measured and shown in Fig. 2(a). The experimental setup to measure I–V characteristics of the STSCR device is inserted into Fig. 2(a). When the STSCR device has no substrate-triggered current ($Ibias = 0$), the STSCR is essentially triggered on by junction avalanche breakdown between its N-well and P-substrate. In Fig. 2(a), the switching voltage of the fabricated STSCR device is as high as 22 V, when the substrate-triggered current is zero. However, the switching voltage is reduced to only 9 V, when the substrate-triggered current is 5 mA. Moreover, the switching voltage is reduced to only 1.85 V, when the substrate-triggered current is increased to 8 mA. The dependence of the switching voltage of the STSCR device on the substrate-triggered current or the substrate bias voltage is shown in Fig. 2(b). The higher substrate-triggered current or substrate bias voltage leads to a much lower switching voltage in the STSCR device. ESD protection devices with low switching voltage can be turned on more quickly to discharge ESD energy and to provide more effective protection for internal circuits.

Another issue of using the SCR device as the ESD protection device is the transient-induced latch-up concern [13], when the IC is operating under normal circuit operation. As a result, the total holding voltage of the ESD protection circuit with SCR devices must be designed to be greater than the maximum voltage level of V_{DD} to avoid the latch-up issue. This can be achieved by stacking the STSCR devices in the ESD protection circuits. The measured I–V curves of two STSCR devices in stacked configuration, which is marked as 2STSCR, under different temperatures are shown in Fig. 3(a). The insert in Fig. 3(a) is the enlarged view around the holding point. The total holding voltage has a bit of degradation when the temperature is increased, because the current gain (β) of the parasitic bipolar transistor in the SCR device is increased with the increase of temperature. The holding voltages of 2STSCR, for example, are 2.9, 2.7, and

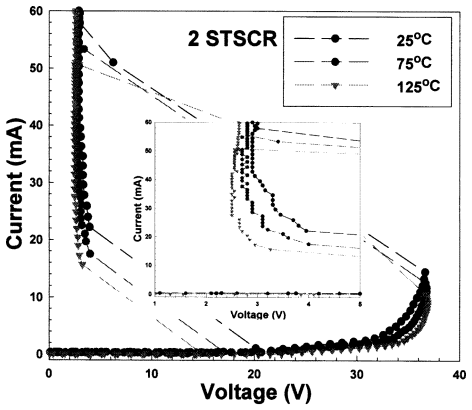


(a)

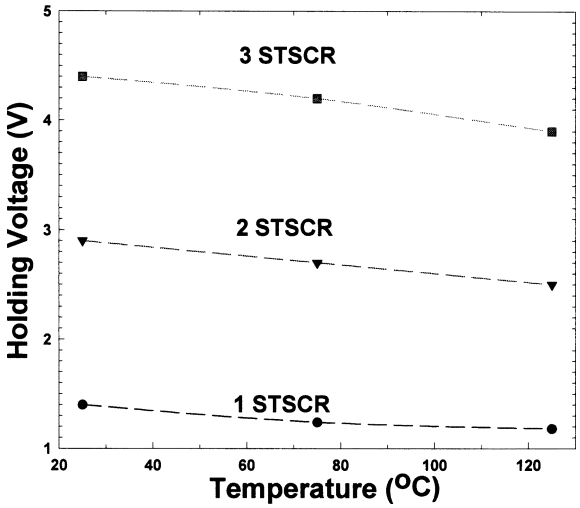


(b)

Fig. 2. (a) Measured I–V curves of the STSCR device under different substrate-triggered currents. (b) The dependence of the switching voltage of the STSCR on the substrate-triggered current and/or the substrate bias voltage in the STSCR device.



(a)



(b)

Fig. 3. (a) Measured I–V curves of two STSCR devices in stacked configuration (2STSCR) at different temperatures. (b) The relation between the holding voltage and the operating temperature under different numbers of stacked STSCR devices.

2.5 V at temperatures of 25 °, 75 °, and 125 °C, respectively. The total holding voltage, however, can be still raised up by increasing the number of the STSCR devices in the stacked configuration. The measured results of the dependence of holding voltage on temperature in the stacked STSCR devices are summarized in Fig. 3(b). The holding voltages of 1STSCR, 2STSCR, and 3STSCR at a temperature of 25 °C are 1.4, 2.9, and 4.4 V, respectively. Although the STSCR devices in stacked configuration have increased switching voltage, such stacked STSCR devices can still be quickly triggered on to provide effective ESD protection, if the substrate-triggered current can be simultaneously applied to the trigger nodes of the stacked STSCR devices.

To investigate the characteristics of the stacked STSCR devices, the measured I–V curves are depicted in Fig. 4 and the measurement setup is also shown in the insert of Fig. 4. If a 3.5-V voltage bias is simultaneously applied to the trigger nodes of two STSCR devices, the switching voltage of 2STSCR is reduced to ~5 V in Fig. 4. Hence, the stacked STSCR configuration can be still turned on quickly if there is a suitable substrate bias. The diodes, $Db1 \sim Db2$, in the insert of Fig. 4 are used to block the current flowing through the metal connected among

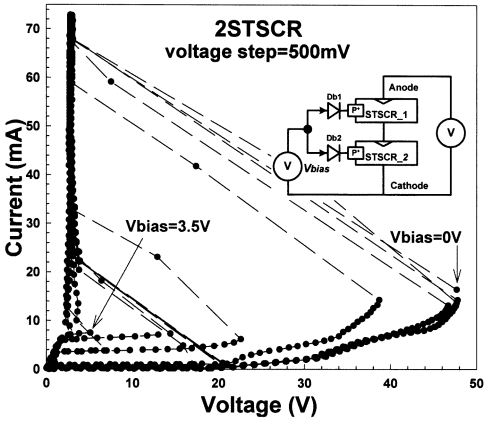


Fig. 4. Measured I–V curves of the two STSCR devices in stacked configuration (2STSCR) when the substrate bias voltages are applied to the trigger nodes.

the trigger nodes of the stacked STSCR devices. Without the blocking diodes, the accumulative property in holding voltage for the stacked STSCR configuration does not exist.

III. On-Chip ESD Protection Circuits With STSCR Devices

A. ESD Protection Circuit for the Input/Output Pads

The ESD protection circuits for input and output pads, realized with the stacked STSCR devices and ESD-detection circuit, are shown in Fig. 5(a) and (b), respectively. All the p-trigger nodes of the stacked STSCR devices are connected to the output node of the ESD-detection circuit, which is formed with an RC and an inverter, through the blocking diodes. The input node of the inverter is connected to V_{DD} through the resistor R. The resistor R is better realized by using the diffusion resistance for the concern of antenna effect [14]. A capacitor C is placed between the input node of the inverter and V_{SS}. This capacitor can be formed by the parasitic capacitance at the input node of the inverter. Under normal circuit operating conditions with V_{DD} and V_{SS} power supplies, the input voltage of the inverter is kept at V_{DD}. Therefore, the output voltage of the inverter is biased at V_{SS} due to the turn-on of NMOS in the inverter. The p-trigger nodes of the stacked STSCR devices are biased at V_{SS} by the output voltage of the inverter, so the stacked STSCR devices are guaranteed to be kept off under the normal circuit operating conditions. When a positive-to-V_{SS} ESD stress is zapping on the pad, the input voltage of the inverter is initially kept at zero and the inverter is biased by the ESD energy on the pad. The output voltage of the inverter is charged up by the ESD energy to generate the trigger current into the trigger nodes of the stacked STSCR devices. Therefore, the STSCR devices are turned on and the ESD current is discharged from the pad to V_{SS} through the stacked STSCR devices. However, the input voltage of the inverter may be charged up by the ESD energy through the forward-biased diode between the pad and V_{DD} power rail. Therefore, the RC time constant in the ESD-detection circuit is designed to keep the input voltage of inverter with a relative low voltage level during the ESD stress condition. The design and simulation of this RC-delay ESD-detection circuit will be described in the following subsections.

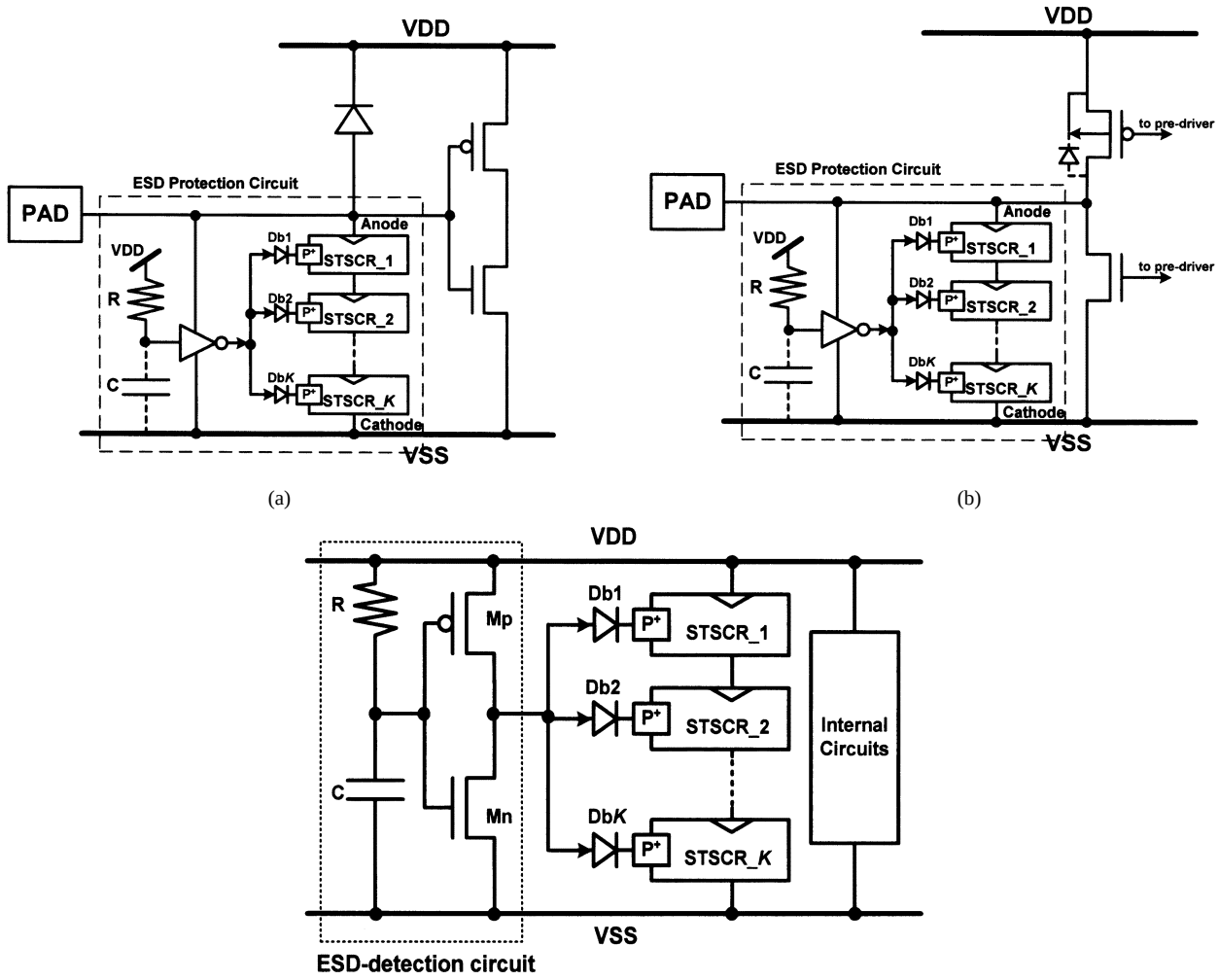


Fig. 5. ESD protection circuits designed for (a) the input pad, (b) the output pad, and (c) the V_{DD}-to-V_{SS} ESD clamp circuit, by using the proposed STSCR devices in a stacked configuration.

B. ESD Clamp Circuit Between the Power Rails

The stacked STSCR devices can be also applied to design the power-rail ESD clamp circuit. The V_{DD}-to-V_{SS} ESD clamp circuit realized with the stacked STSCR devices is shown in Fig. 5(c). The number of the stacked STSCR devices between V_{DD} and V_{SS} power rails is dependent on the maximum voltage level between V_{DD} and V_{SS} in the normal circuit operating conditions to avoid the latch-up issue. The RC time constant is designed to distinguish the V_{DD} power-on event (with a rise time of $\sim$ms) from the ESD-stress events (with a rise time of $\sim$ns) [15]. During the normal V_{DD} power-on transition (from low to high), the input voltage of the inverter in Fig. 5(c) can follow up in time with the power-on V_{DD} signal, so the output voltage of the inverter is kept at zero. Hence, the stacked STSCR devices are kept off and do not interfere with the functions of internal circuits.

When a positive ESD voltage is applied to the V_{DD} pin with the V_{SS} pin relatively grounded, the RC delay will keep the input voltage of the inverter at a low voltage level for a long time; therefore, the output voltage of the inverter will become high to trigger the stacked STSCR devices. While the stacked STSCR devices are triggered on, the ESD current is discharged from V_{DD} to V_{SS} through the stacked STSCR devices. By suitable design on the ESD-detection circuit, the stacked STSCR devices can be quickly triggered on to discharge ESD current. The detection of ESD transition is based on the RC delay in the ESD-detection circuits, which are the same function in the input/output ESD protection circuits and the V_{DD}-to-V_{SS} ESD clamp circuit. So, the RC circuits for the input, output, and power pads in Fig. 5 can be implemented with the same one in a CMOS IC to save the chip layout area.

C. Circuit Simulation

The optimum design on the ESD-detection circuit with the RC inverter to trigger on the stacked STSCR devices for discharging ESD current from V_{DD} to V_{SS} is studied in Fig. 6. The design parameters of the R, C, and PMOS channel width (Wp) of the inverter are first considered. Fig. 6(a) shows the transient simulations of the ESD-detection circuit under different resistances of R, where C is fixed at 1 pF and the device dimensions W/L of the PMOS and NMOS are 30/0.5 and 10/0.5, respectively. An 8-V voltage pulse with a rise time of 10 ns is applied to the V_{DD} pin to simulate the ESD event. The Y axis in

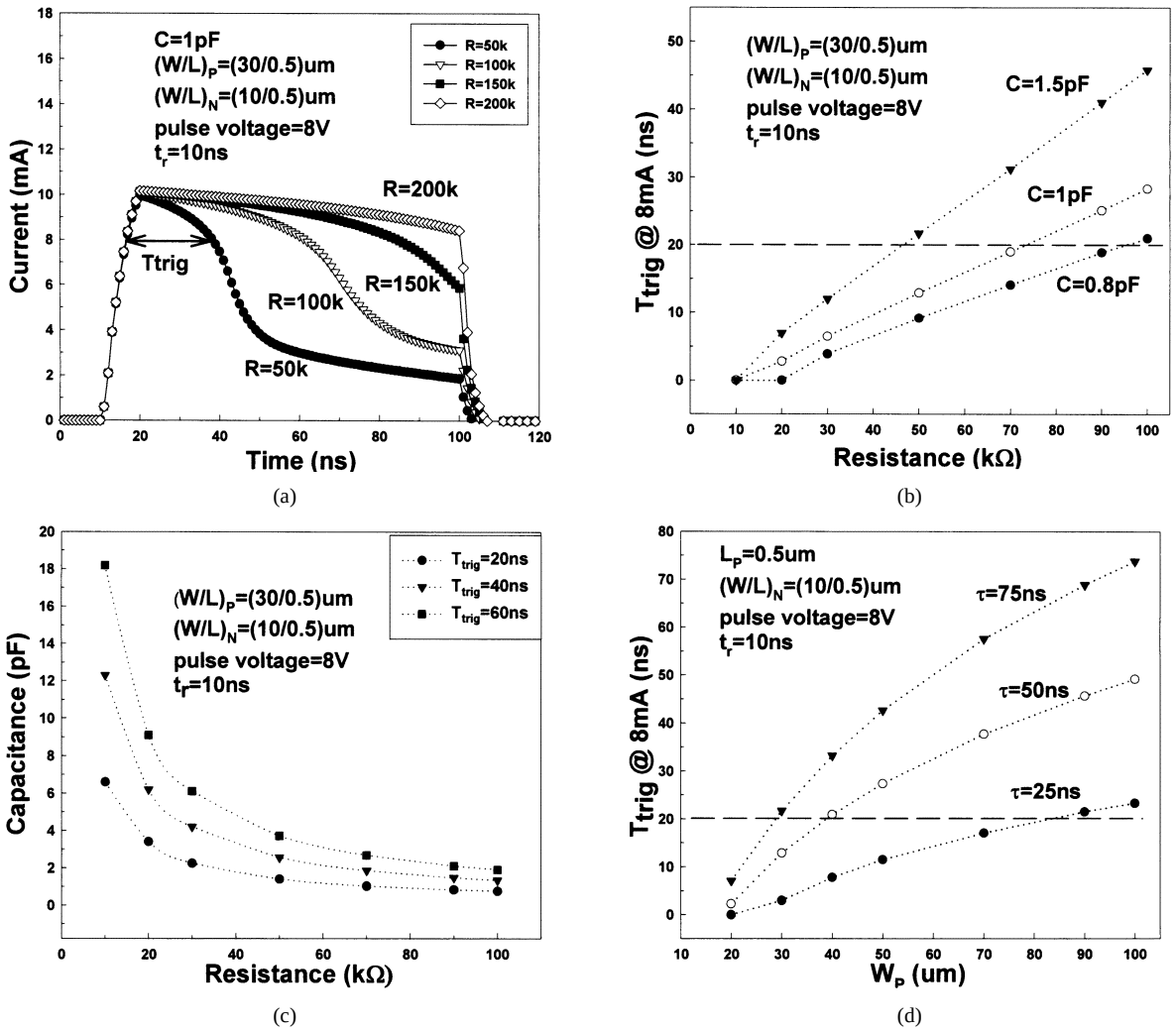


Fig. 6. Dependence of the various design parameters in the ESD-detection circuit on the trigger time ($\mathrm{T_{trig}}$) by SPICE simulation, when the output current of inverter is greater than 8 mA. (a) The transient simulations of the ESD-detection circuit under different resistances of R but with a fixed C of 1 pF. (b) The dependence of the $\mathrm{T_{trig}}$ on the resistance R under different capacitance C. (c) The relation between the resistance R and the capacitance C under different $\mathrm{T_{trig}}$ time periods. (d) The relation between the channel width (W_p) of inverter's PMOS and the $\mathrm{T_{trig}}$ under different RC time constants.

Fig. 6(a) is the output current from the inverter of the ESD-detection circuit. In Fig. 2(b), the switching voltage of the STSCR device is reduced to only 1.85 V, if the substrate-triggered current is 8 mA. Based on this condition, the trigger time when the output current of inverter is greater than 8 mA is defined as "$\mathrm{T_{trig}}$" in Fig. 6. $\mathrm{T_{trig}}$ is increased with the increase of the resistance R in Fig. 6(a). If the turn-on time of the STSCR device, which is defined as the corresponding time from triggering state to latching state, will take about 20 ns, the $\mathrm{T_{trig}}$ must be designed greater than 20 ns to ensure that the STSCR device can enter into latching state. The dependence of the $\mathrm{T_{trig}}$ on the resistance (R) under different capacitance (C) is simulated and shown in Fig. 6(b). $\mathrm{T_{trig}}$ is increased while the resistance (R) or the capacitance (C) is increased, because the input voltage of the inverter can be kept at a low level for a relatively longer time. The relation between the resistance (R) and capacitance (C) under different $\mathrm{T_{trig}}$ time periods are simulated and shown in Fig. 6(c). The suitable values for the resistance (R) and capacitance (C) can be finely tuned from Fig. 6(b) and (c). Under ESD zapping, the PMOS is on and NMOS is off initially, thus the output current of the inverter is dominated by the PMOS. The relations between channel width (Wp) of PMOS and the $\mathrm{T_{trig}}$ under different RC time constants (τ) are shown in Fig. 6(d). With the increase of the channel width of PMOS or the RC time constant, the corresponding $\mathrm{T_{trig}}$ is increased. To meet the $Trig$ of 20 ns, the PMOS with a larger channel width only needs a smaller RC time constant. Such an optimum design on device parameters in the ESD-detection circuit can be finely tuned by SPICE simulation for different CMOS IC applications.

IV. Experimental Results

The proposed ESD protection circuits have been designed with different numbers of stacked STSCR devices and fabricated in a 0.25-μm salicided CMOS process. The STSCR device is realized with a layout area of 40 μm $\times$ 20 μm including P+ and N-well rings in the 0.25-μm salicided CMOS process. However, the active area of each STSCR without including the guard rings is only 20 μm $\times$ 20 μm. The human-body-model (HBM) and machine-model (MM) ESD stresses are applied to the ESD protection circuits to verify their ESD robustness. The HBM and MM ESD test results on the stacked STSCR devices

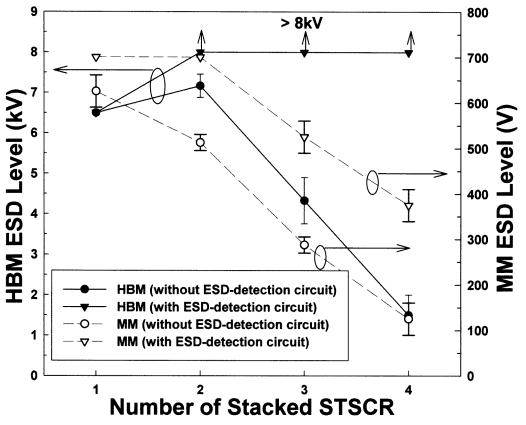


Fig. 7. Dependence of the HBM and MM ESD levels of stacked STSCR configuration on the number of stacked STSCR devices (failure criterion: $I_{\rm Leakage} > 1\ \mu$A @ 2.5 V bias).

in the device level (without the ESD-detection circuit) and circuit level (with a ESD-detection circuit) are compared in Fig. 7. In this experimental measurement, the ESD-detection circuit including R, C, and the inverter are realized with $R = 100$ kΩ, $C = 3$ pF, PMOS dimension $W/L = 80/0.5$, and NMOS dimension $W/L = 20/0.5$. In this ESD verification, the failure criterion is defined as the leakage current of the device or circuit after ESD stress is greater than 1 μA under a voltage bias of 2.5 V. For device level, because the total holding voltage of the stacked STSCR configuration is increased with an increase of the number of stacked STSCR devices, the HBM ESD robustness of the stacked STSCR is decreased with an increase of the number of stacked STSCR devices except for the condition of 2STSCR. It is supposed that there are additional parasitic SCR paths among the two STSCR devices, which can be triggered on in time to discharge ESD energy. So, the HBM ESD robustness of 2STSCR is slightly greater than that of 1STSCR. The anticipated ESD discharging path is from STSCR_1 to STSCR_2. The additional ESD discharging path is from the P+, N-well (STSCR_1), P-substrate to N+ (STSCR_2), and so on. However, for 3STSCR or 4STSCR, the HBM ESD robustness is dominated by the total holding voltage, whereas the additional parasitic SCR path cannot be triggered on in time to bypass the ESD current. So, the HBM ESD levels of 3STSCR and 4STSCR are degraded while the number of stacked STSCRs is increased. However, the ESD level of stacked STSCR devices can be greatly improved especially for 3STSCR or 4STSCR, if the ESD-detection circuit is used to trigger the stacked STSCR devices. In Fig. 7, the HBM ESD levels of the stacked STSCR with ESD-detection circuit are all boosted up to >8 kV. For MM ESD event, because it has a faster ESD transition than the HBM event, the additional parasitic SCR paths in the stacked STSCR may not be triggered on in time to bypass the ESD current under such fast MM ESD zapping conditions. So, for the device level, the MM ESD level is decreased when the number of stacked STSCR devices is increased. However, the MM ESD levels of the stacked STSCR devices can be also improved if the ESD-detection circuit is used to trigger the stacked STSCR devices.

TABLE I
COMPARISON OF THE ESD ROBUSTNESS BETWEEN THE STACKED STSCR DEVICES AND THE GGNMOS

Device	2STSCR	3STSCR	GGNMOS
Active Area (μm^2)	20×20×2	20×20×3	25.8×50
HBM (kV)	> 8	> 8	3.5
$\frac{V_{ESD,HBM}}{Area}$ (V/μm^2)	> 10	> 6.67	2.71
MM (V)	700	525	375
$\frac{V_{ESD,MM}}{Area}$ (V/μm^2)	0.88	0.44	0.29

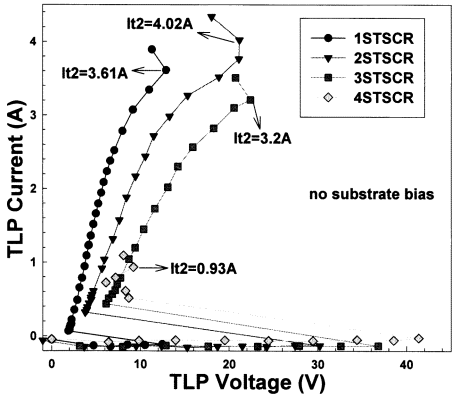


Fig. 8. TLP-measured I–V curves of the stacked STSCR configuration without substrate bias under different numbers of stacked STSCR devices.

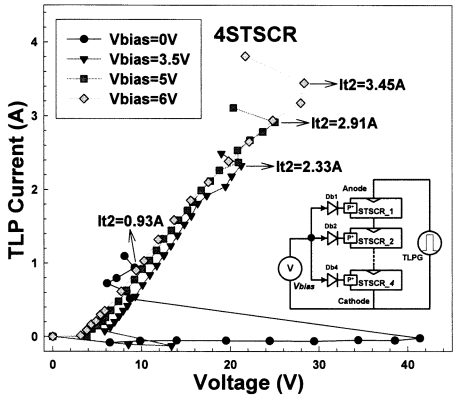
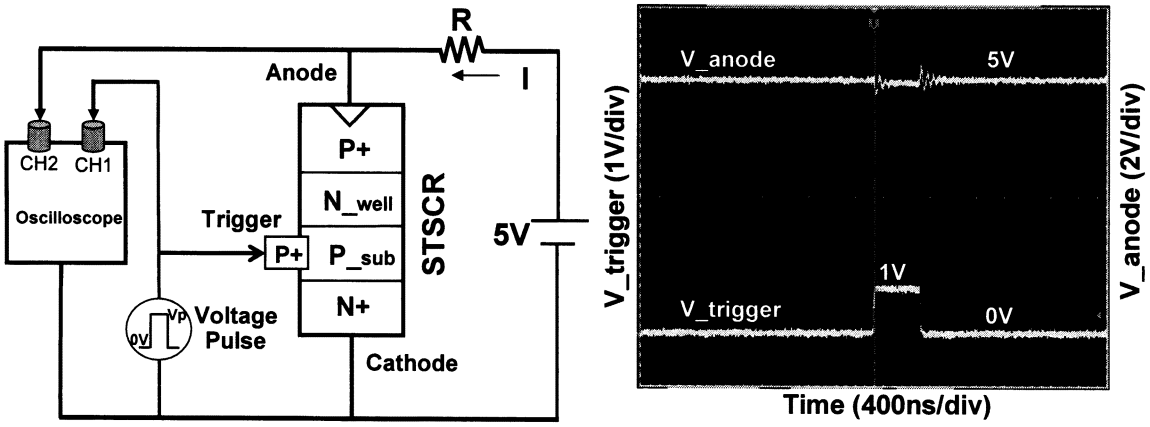
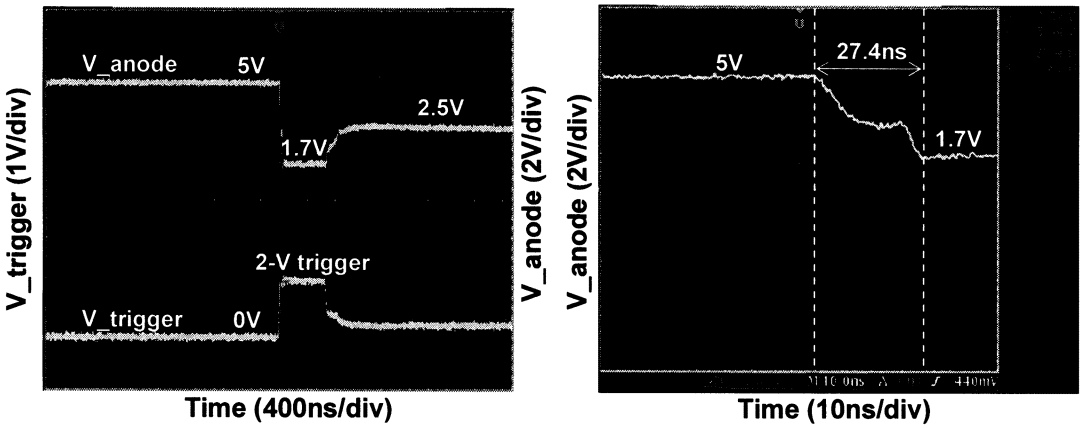


Fig. 9. TLP-measured I–V curves of the four STSCR devices in the stacked configuration (4STSCR) under different substrate bias voltages.

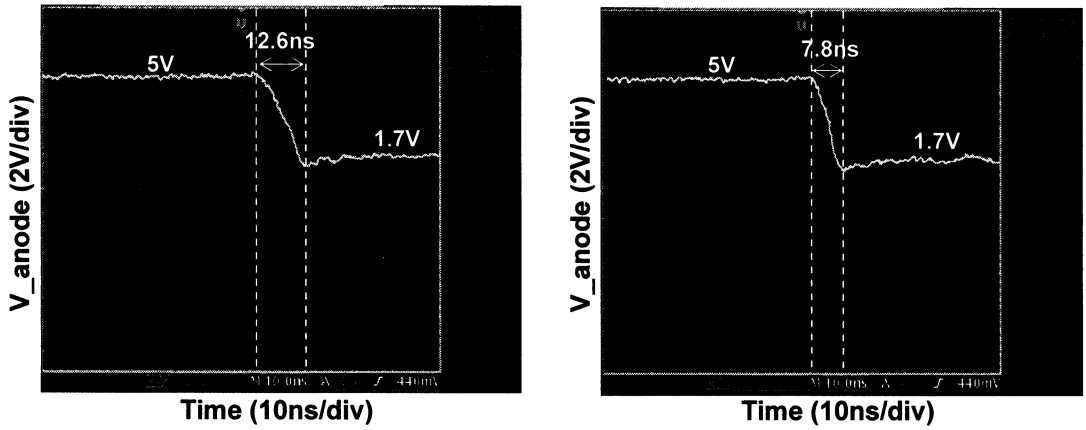
A gate-grounded NMOS (GGNMOS) device with W/L of 200/0.5 had been fabricated in the same CMOS process with extra silicide-blocking mask for comparison reference. Such a GGNMOS occupying a large active layout area of 25.8 μm × 50 μm can sustain the HBM ESD level of 3.5 kV. The comparison on the ESD robustness between the stacked STSCR devices and GGNMOS is shown in Table I. For the ESD protection circuit designed with 2STSCR and the



(a) (b)



(c) (d)



(e) (f)

Fig. 10. Turn-on verification of STSCR device under different substrate biases. (a) Experimental setup. The measured voltage waveforms on the anode and trigger nodes of the STSCR device under (b) 1-V voltage triggering and (c) 2-V voltage triggering. The close-up views of the V_anode at the falling edge while the STSCR is triggered by the voltage pulse of (d) 1.5 V, (e) 2 V, and (f) 4 V into the P+ trigger node.

ESD-detection circuit, the HBM (MM) ESD level per layout area is >10 V/μm^2 (0.88 V/μm^2), but it is only 2.71 V/μm^2 (0.29 V/μm^2) for the GGNMOS. This has verified the excellent area efficiency of the ESD protection circuits realized with the proposed stacked STSCR devices.

By using the transmission line pulsing (TLP) measurement [16], [17], the secondary breakdown current $(It2)$ of the STSCR device can be found. The $It2$ is another index for the HBM ESD robustness, which is indicated in this work by the sudden increase of the leakage current at the voltage bias of 2.5 V. The

relation between the second breakdown current $(It2)$ and HBM ESD level $(V_{\rm ESD})$ can be approximated as

$$V_{\rm ESD} \cong (1500 + Ron) \times It2 \quad (1)$$

where Ron is the dynamic turn-on resistance of the device under test. The TLP-measured I–V curves of the stacked STSCR devices with different numbers of STSCR devices are shown in Fig. 8. The $It2$ in Fig. 8 is almost decreased with an increase of the number of stacked STSCR devices except for the condition of 2STSCR, which is similar to the results of HBM ESD level. The above hypothesis about the existence of the additional parasitic SCR paths can also be used to explain why the 2STSCR has a higher $It2$. The TLP-measured I–V curves of the 4STSCR under different substrate bias voltages are shown in Fig. 9. Although the $It2$ of 4STSCR without substrate bias is only 0.93 A, it can be improved to 3.45 A if a 6-V voltage bias is applied to the trigger nodes through the blocking diodes in Fig. 9. By increasing the substrate bias voltage, the $It2$ of the stacked 4STSCR is also increased. In Fig. 9, the switching voltage of the stacked STSCR devices can also be reduced to a low voltage level when the voltage bias is applied to the trigger nodes, which is consistent with the results shown in Fig. 4.

In order to investigate the turn-on efficiency of the ESD protection circuit realized with STSCR devices, the experimental setup to measure the required turn-on time of the STSCR device is illustrated in Fig. 10(a). The measured results in the time domain are shown in Fig. 10(b)-(f), where the V_anode (V_trigger) is the voltage waveform on the anode (trigger) of the STSCR shown in Fig. 10(a). A 5-V voltage bias is connected to the anode of the STSCR device through a resistance of 47 Ω, which is used to limit the sudden large transient current from power supply when the STSCR is turned on. A voltage pulse with a pulse width of 400 ns and a rise time of 10 ns is applied to the trigger node. While a voltage pulse of 1 V is applied to the trigger node, the V_anode has no change, as shown in Fig. 10(b). So, the STSCR device has at least a substrate noise margin of 1 V. The V_anode, however, is triggered into the latching state while the pulse voltage is increased to 2 V, as shown in Fig. 10(c). The forward-biased P+ trigger node to cathode in the STSCR device limited the full swing of the 2-V applied voltage waveform in Fig. 10(c). After the triggering the 2-V voltage pulse, the V_anode is still kept at a low voltage level of 2.5 V. The STSCR device has been successfully triggered on and provided a low-impedance path to discharge current from its anode to its cathode. The required turn-on time for the STSCR device into its latching state is observed by the close-up views of the V_anode waveform at the falling edge, which are shown in Fig. 10(d)-(f) under different triggering voltage pulses. From Fig. 10(d)-(f), the turn-on time of the STSCR device can be reduced from 27.4 to 7.8 ns, while the pulse height of the triggering voltage pulse is increased from 1.5 to 4 V. The turn-on speed is improved with a factor of ∼4. The measured results have confirmed that the ESD protection circuit with the STSCR devices proposed in this paper can indeed be turned on more quickly to discharge ESD current.

To verify the property of free to latch-up issue, another verification to measure the holding voltages of the stacked STSCR devices is tested under transient conditions, and the results are shown in Fig. 11. The stacked STSCR devices can be triggered on by the ESD-detection circuit and provide a low impedance path to discharge the ESD energy. In Fig. 11, a 0–8 V voltage pulse applied to the V_{DD} line of Fig. 5(c) is clamped to 1.6 V (3.2 V) by the ESD protection circuit with the 1STSCR (2STSCR) device and the ESD-detection circuit. The clamped voltage level of the ESD protection circuit can be linearly adjusted by changing the number of stacked STSCR devices for practical applications in CMOS IC products with different V_{DD} voltage levels.

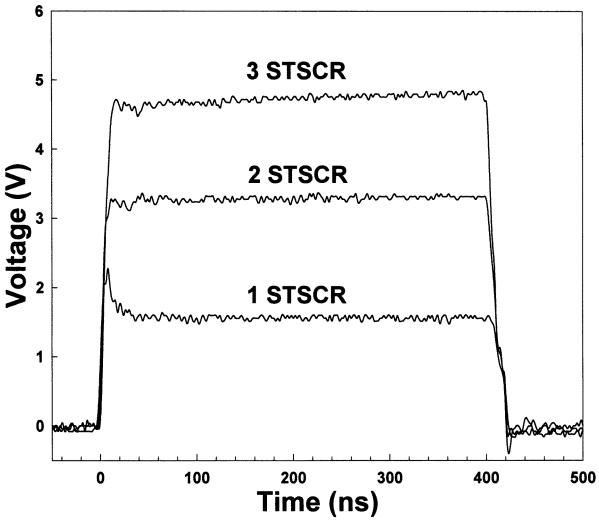


Fig. 11. Measured voltage waveform on the V_{DD} line, clamped by different stacked STSCR devices with ESD-detection circuit, when a 0–8 V voltage pulse is applied to the V_{DD} line of the V_{DD}-to-V_{SS} ESD clamp circuit with the V_{SS} grounded.

V. Conclusion

A novel STSCR device used for on-chip ESD protection circuits has been successfully investigated in a 0.25-μm salicided CMOS process. By using the substrate-triggered technique, the STSCR device has the advantages of controllable switching voltage (∼1.85 V @ 8 mA or ∼1.55 V @ 1.06 V) and high ESD robustness in a smaller layout area (∼16 V/μm^2). On-chip ESD protection circuits designed with the stacked STSCR devices and ESD-detection circuit have the advantages of free to latch-up issue, adjustable holding voltage, fast turn-on speed, and higher ESD robustness, which are very useful in CMOS IC products in subquarter-micrometer CMOS processes. The experimental result has shown that the turn-on time of STSCR can be reduced from 27.4 to 7.8 ns by the substrate-triggering technique. For the IC application with a V_{DD} of 2.5 V, the ESD protection circuit designed with two STSCR devices in a stacked configuration has a clamp voltage of ∼3.2 V and the HBM (MM) ESD level per area of >10 V/μm^2 (0.88 V/μm^2) in a 0.25-μm fully salicided CMOS process without using extra process modification.

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