Substrate-Triggered ESD Protection Circuit Without Extra Process Modification

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***Abstract*—A substrate-triggered technique is proposed to improve electrostatic discharge (ESD) protection efficiency of ESD protection circuits without extra salicide blocking and ESD-implantation process modifications in a salicided shallow-trench-isolation CMOS process. By using the layout technique, the whole ESD protection circuit can be merged into a compact device structure to enhance the substrate-triggered efficiency. This substrate-triggered design can increase ESD robustness and reduce the trigger voltage of the ESD protection device. This substrate-triggered ESD protection circuit with a field oxide device of channel width of 150 μm can sustain a human-body-model ESD level of 3250 V without any extra process modification. Comparing to the traditional ESD protection design of gate-grounded nMOS (ggnMOS) with silicide-blocking process modification in a 0.25-μm salicided CMOS process, the proposed substrate-triggered design without extra process modification can improve ESD robustness per unit silicon area from the original 1.2 V/μm^2 of ggnMOS to 1.73 V/μm^2.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuits, gate-coupled technique, substrate-triggered technique.**

I. Introduction

ELECTROSTATIC discharge (ESD) damage has become the main reliability issue for deep-submicron CMOS integrated circuit (IC) products. To overcome this ESD problem, on-chip ESD protection circuits have been added around the input and output pads of the CMOS ICs against ESD damages. But the effectiveness of ESD protection circuits is seriously degraded by the advanced CMOS fabrication technologies, especially when the lightly doped drain (LDD) structure and silicided diffusion are used [1]. Therefore, salicide blocking [2], [3] and ESD implantation [4]–[8] process modifications have been added into the CMOS processes to improve the ESD robustness of the MOSFET. These additional process modifications in CMOS technology must be done with extra process steps and mask layers, which increase the fabrication cost and slow down the throughput of production. Moreover, with aggressive device scaling, the circuit operating voltage has been decreased correspondingly. Some early 5-V systems have changed from 5 to 3.3 V, or even 1.8 V. Thus, system voltages have not been kept at 5 V but mixed 5 and 3.3 V. For mixed-voltage I/O design [9]–[12], the IC with 3.3-V power supply needs to accept 5-V input signals. In the traditional ESD protection design, the normal input signal with high voltage may turn on the ESD protection device, which is connected between the input pad and V_{DD} power line. Therefore, the traditional input ESD protection circuit must be modified for application in this mixed-voltage interface.

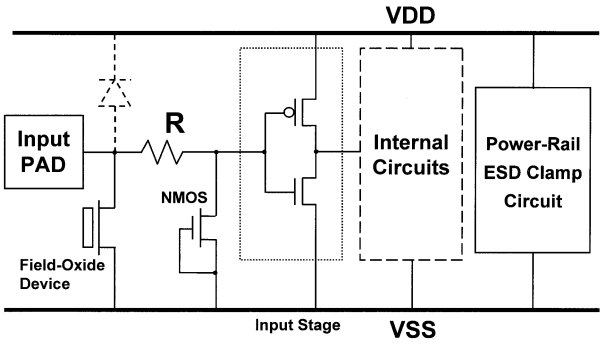

Fig. 1. Traditional input ESD protection circuit for digital input pin in CMOS ICs.

The ESD stress on an input pin has four modes of pin combination: positive-to-V_{SS}, negative-to-V_{SS}, positive-to-V_{DD}, and negative-to-V_{DD} [13]. To protect the thinner gate oxide of the input stage in CMOS ICs under all ESD stress conditions, a traditional two-stage ESD protection circuit for the digital input pin is shown in Fig. 1. A gate-grounded short-channel nMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD protection level, a robust field-oxide device (FOD) is often used as the main discharge element in the primary protection stage to discharge ESD current. Between the primary and secondary stages, a resistor R is added to limit ESD current flowing through the short-channel nMOS in the secondary stage. The primary ESD clamp device must be triggered on to discharge ESD current before the gate-grounded nMOS (ggnMOS) in the secondary stage is damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance of R should be large enough, even on the order of kilohms. Under the positive-to-V_{SS} and negative-to-V_{SS} ESD stress conditions, the ESD current can be discharged through the FOD and ggnMOS devices. However, in the mixed-voltage situation, the diode or pMOS connected from the pad to V_{DD} power line is forbidden by the normal circuit operation with a high-voltage input signal. Without the diode or pMOS connected from the pad to V_{DD}, the positive-to-V_{DD} and negative-to-V_{DD} ESD stresses are still discharged from the pad to V_{SS} power line and

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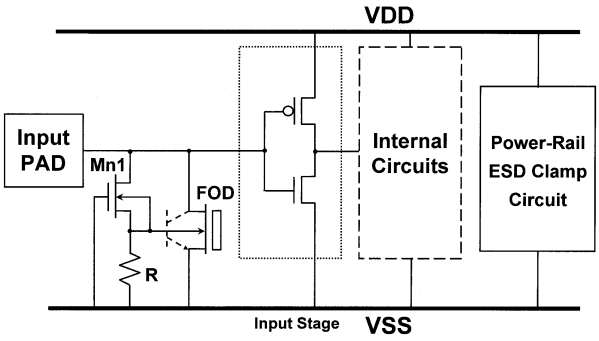


Fig. 2. Proposed ESD protection circuit with substrate-triggered FOD to protect the input stage.

then conducted through the power-rail ESD clamp circuit to the grounded $V_{\rm DD}$ pin. The efficient power-rail ESD clamp circuit is important under such ESD stress conditions to bypass ESD current away from the internal circuits [14].

To sustain the required ESD level, the ESD protection device must be drawn with larger device dimensions, which has often been realized in layout with multiple fingers to reduce the total silicon area. But, during ESD stress, the multiple fingers of the ESD protection MOSFET cannot be uniformly turned on. Only several fingers of the MOSFET are turned on and, therefore, damaged by ESD [15], [16]. This often causes a low ESD level in the ESD protection circuit, even if the MOSFET has been drawn with a large device dimension. To efficiently improve the turn-on uniformity among those multiple fingers, the gate-driven design [16]–[18] has been reported to increase ESD robustness of the large-device-dimension nMOS. Recently, some studies have found that ESD robustness of the gate-driven nMOS was decreased dramatically when the gate voltage was somewhat increased [18], [19]. The gate-driven design causes ESD current to discharge mainly through the surface channel of the nMOS, therefore, the nMOS is easily burned out by ESD energy. To avoid the sudden degradation on ESD level of the gate-driven devices, the substrate-triggered design has been proposed to improve ESD robustness of the ESD protection devices [20]–[22].

In this paper, a new substrate-triggered design is proposed to improve ESD robustness of the ESD protection circuit without extra silicide-blocking and ESD-implantation process modifications. Such design can be further modified for use in CMOS output buffers to improve ESD robustness.

II. Substrate-Triggered ESD Protection Circuits

A. Substrate-Triggered Input ESD Protection Circuit

The proposed input ESD protection circuit with the substrate-triggered design is shown in Fig. 2. This input ESD protection circuit is combined with a short-channel gate-grounded nMOS (Mn1), a resistor (R), and a FOD. During ESD stress, the short-channel gate-grounded nMOS with a lower snapback breakdown voltage can be more quickly triggered on than the FOD with a higher breakdown voltage. Both the source and the substrate of the gate-grounded nMOS is connected to the substrate of the FOD to form a trigger path to the base of the parasitic lateral bipolar junction transistor (LBJT), which is shown by the dashed line beside the FOD in Fig. 2. The collector/emitter of the parasitic LBJT is formed with the drain/source of the FOD and the base formed from the substrate of the FOD. To effectively trigger on this parasitic LBJT, a suitable voltage is applied on the resistance R to turn on the base–emitter junction of parasitic LBJT during ESD stress.

When a positive ESD voltage is zapping on the input pad with $V_{\rm SS}$ grounded, the ESD voltage can trigger Mn1 into snapback breakdown. Therefore, a substrate current generated by the turned-on Mn1 will flow into the base of the parasitic LBJT in the FOD. The parasitic LBJT of the FOD will be triggered on by the substrate current. Because the nMOS with shorter channel length has smaller snapback breakdown voltage, the channel length of Mn1 has to be designed as small as possible to quickly trigger Mn1 on during ESD events. When the FOD in Fig. 2 is applied with a positive substrate bias, the trigger voltage of FOD will become lower than the original drain breakdown voltage of the FOD without substrate bias. During the ESD event, the combination of Mn1 and resistor R can provide a substrate-triggered current to trigger on the parasitic LBJT of the FOD, which provides the desired ESD protection for the input stage of ICs in deep-submicron CMOS process.

During negative-to-$V_{\rm SS}$ ESD stress condition, the negative ESD voltage can forward bias the p-n junction between the substrate and the drain of the FOD (or Mn1) to discharge ESD current. The forward-biased p-n junction with a low operating voltage (as a diode) in the FOD (or Mn1) can sustain much higher ESD levels. During the positive-to-$V_{\rm DD}$ or the negative-to-$V_{\rm DD}$ ESD stress conditions, the ESD current is still discharged from the pad to the $V_{\rm SS}$ power line and then conducted through the power-rail ESD clamp circuit to the grounded $V_{\rm DD}$ pin. A turn-on efficient power-rail ESD clamp circuit [14] should be included in the chip to provide overall ESD protection for the input pin.

By using the substrate-triggered design, the FOD in Fig. 2 can be uniformly turned on to sustain higher ESD levels than the traditional design in Fig. 1, under the positive ESD stress conditions. The two-stage ESD protection design in Fig. 1 may provide high ESD protection levels for the digital input pins, but because the large series resistance and the junction capacitance of the ESD clamp devices cause a long *RC* delay to the input signal, such a traditional design is not suitable for analog pins. For current-mode input signals or high-frequency applications, the series resistance between the input pad and input stage is forbidden. The traditional two-stage ESD protection design in Fig. 1 is no longer suitable for analog applications. On the contrary, the proposed substrate-triggered ESD protection circuit without series resistance, as that shown in Fig. 2, can provide lower triggered voltage to effectively protect the thin gate oxide of the input stage. It is, therefore, more suitable for analog circuit applications.

B. Alternative Substrate-Triggered Input ESD Protection Circuit

An alternative design of the proposed input ESD protection circuit with a long-channel-length nMOS is shown in Fig. 3. The alternative design is similar to the proposed circuit in Fig. 2, but the long-channel-length nMOS (Mn2) is used in place of

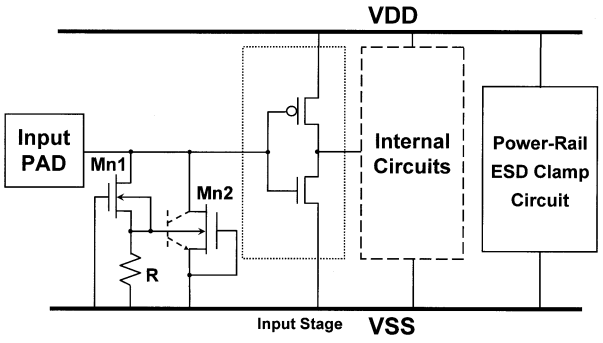


Fig. 3. Alternative design of the proposed substrate-triggered ESD protection circuit with long-channel-length nMOS Mn2 to protect the input stage.

the FOD. The alternative ESD protection circuit includes a first nMOS (Mn1), a resistor (R) and a second nMOS (Mn2). Both the source and the substrate of Mn1 are also connected to the substrate-triggered point of Mn2. The gate of Mn2 is connected to V_{SS}. Mn1 is designed with a lower snapback breakdown voltage than that of Mn2 to quickly generate the substrate-triggered current. Further, a parasitic LBJT is also included in Mn2, as shown by the dashed lines beside the Mn2 in Fig. 3. The parasitic LBJT has a collector/emitter formed with the drain/source of Mn2 and a base formed from the substrate of Mn2.

Under positive ESD stress, the parasitic LBJT in Mn2 can be triggered on by the substrate current generated from Mn1 and resistor R. The operation principles of the input ESD protection circuit with the long-channel-length nMOS are similar to that of the input ESD protection circuit with the FOD.

C. Realization of Substrate-Triggered ESD Protection Circuits

To realize the effective substrate-triggered input ESD protection circuit, the whole circuit is merged into a single device structure. The cross-sectional view and layout top view of the input ESD protection circuit in Fig. 2 are shown in Fig. 4, which is fabricated in a 0.25-μm salicided shallow-trench-isolation (STI) CMOS technology [23]. The symmetric device structure in Fig. 4 allows a balanced current path that can help to increase the current uniformity among the multiple fingers of the FOD in the input ESD protection circuit. As shown in Fig. 4, the nMOS Mn1 with thin gate oxide, the resistor R, and the FOD are formed on the same p-type substrate, where neither silicide-blocking nor ESD-implantation process modifications are added in the device structure.

Without using the silicide-blocking process, a first n-well is connected to the input pad and also to the drain of Mn1 to protect Mn1 from being burned out during ESD stress. Because Mn1 is formed with short-channel LDD and silicided diffusion, which would be weak to ESD stress [1], the first n-well can help Mn1 to sustain some ESD overstress before the FOD is triggered on. The resistor R is realized by the parasitic substrate resistance. The second n-well is formed into the drain of the FOD. This n-well also has the effect of increasing the equivalent resistance of the resistor R. The n+ diffusion in the source of the FOD can collect the triggering current from the trigger point of p+ diffusion, which is directly connected to the source of Mn1 by the low-resistance silicided layer upon the diffusion, to trigger on

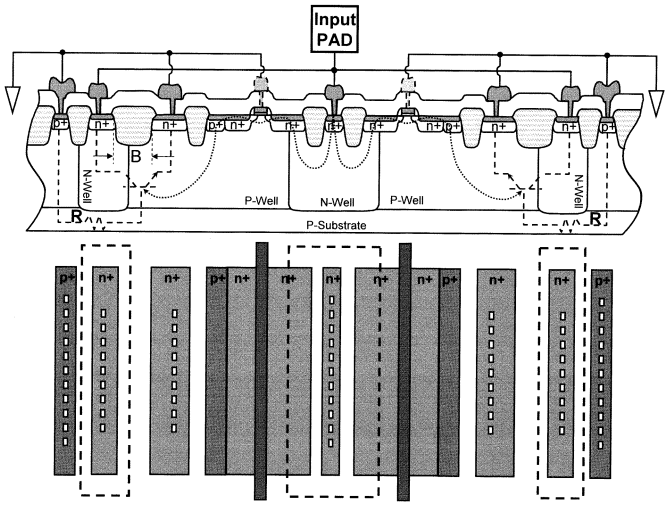


Fig. 4. Merged device structure of the whole input ESD protection circuit with the substrate-triggered FOD in Fig. 2.

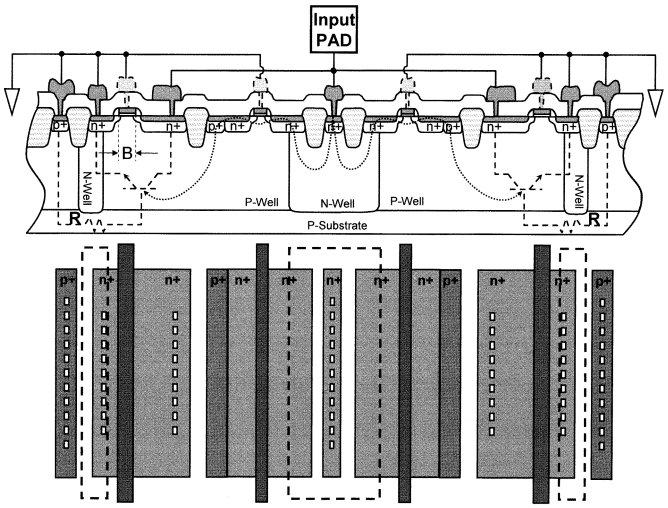
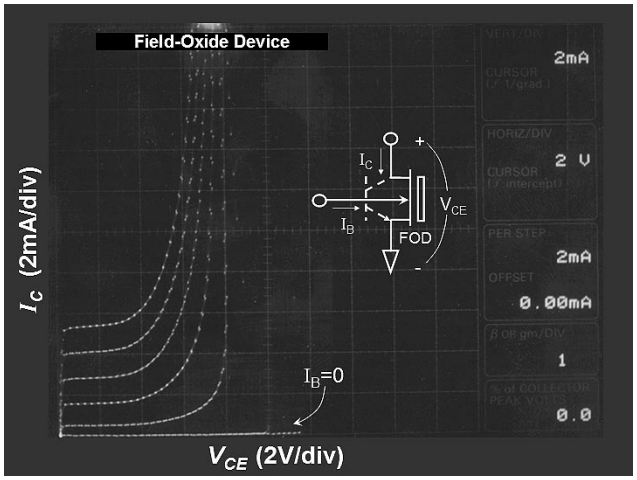


Fig. 5. Merged device structure of the whole alternative input ESD protection circuit with substrate-triggered nMOS Mn2 in Fig. 3.

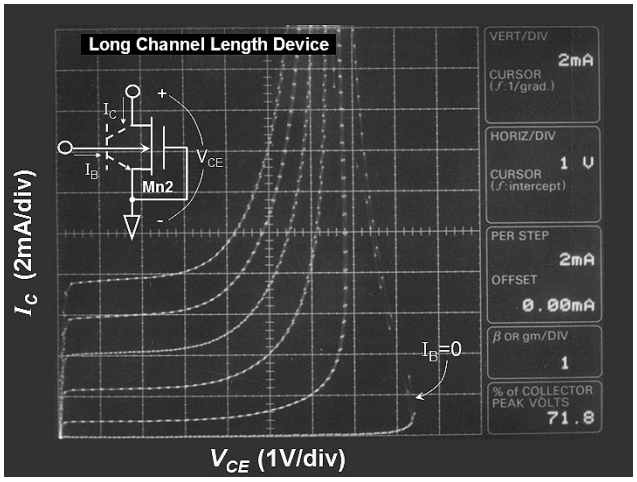
the parasitic LBJT in the FOD during ESD stress. The proposed input ESD protection circuit is, thus, considerably enhanced in its ESD robustness through the substrate-triggered design.

The geometric spacing between two n+ diffusions of the FOD is marked with "B" in Fig. 4. This can affect the turn-on efficiency of the parasitic LBJT during ESD stress. In Fig. 4, the n-well overlapped spacing from the edge of drain diffusion to the edge of the n-well is kept at 0.3 μm for those FOD devices drawn with different B spacings in the experimental test chip.

The cross-sectional view and layout top view of the input ESD protection circuit with the long-channel-length nMOS (Mn2) in Fig. 3 are shown in Fig. 5. The realization of this alternative input ESD protection circuit is also formed with the first and second n-wells. The first n-well can suppress ESD current flowing through the short-channel nMOS (Mn1). The second n-well covers the partial source region of Mn2, as that shown in Fig. 5, to enhance the performance of the parasitic LBJT in Mn2 and also to increase the equivalent substrate resistance R. The channel length of Mn2 is marked with "B"



(a)



(b)

Fig. 6. Measured dc I–V curves of the standalone (a) FOD and (b) nMOS, with a B spacing of 2 μm under different substrate current biases.

in Fig. 5 to compare with that in the FOD device. Neither silicide-blocking nor ESD-implantation process modifications are added in this alternative input ESD protection circuit in the experimental test chip.

III. Experimental Results

The proposed input ESD protection circuits with thin gate oxide and silicided diffusion, but no ESD implantation, have been designed and fabricated in a 0.25-μm salicided STI CMOS process. Compared with the traditional design, some ggnMOS devices with extra silicide-blocking processes are also designed and fabricated in the same 0.25-μm salicided CMOS process. To clearly investigate the characteristics of the LBJTs in the FOD of Fig. 2 or in the nMOS Mn2 of Fig. 3, the standalone FOD and nMOS Mn2 are also fabricated in the test chip.

A. Device Characteristics

The Tek 370A curve tracer, produced by Tektronix Inc., is used to measure the dc I–V curves of the LBJTs in the FOD or nMOS devices. The measured dc I–V curves of the LBJT in the FOD with spacing B of 2 μm under different substrate currents I_B are shown in Fig. 6(a). The original snapback breakdown

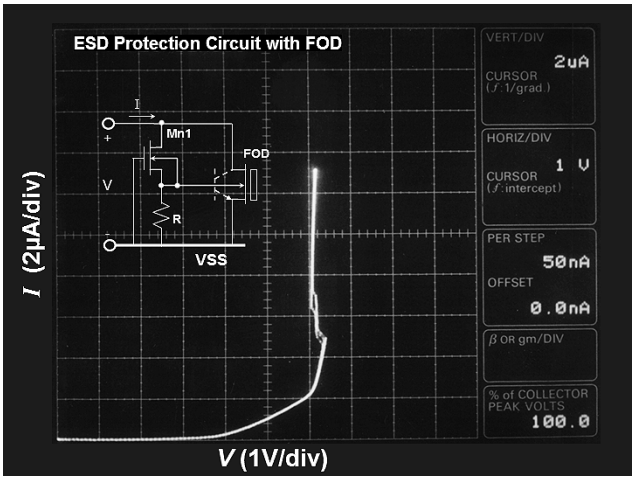


Fig. 7. Overall dc I–V curve around the trigger point of the proposed input ESD protection circuit with the substrate-triggered FOD.

voltage of the FOD is as high as 11.9 V, but the trigger voltage for the FOD entering into its snapback region is significantly reduced if there is a triggering current into its base. The dc I–V curves of the LBJT in nMOS Mn2 with a channel length of 2 μm are measured under different substrate currents I_B and shown in Fig. 6(b). The original snapback breakdown voltage of Mn2 is 8.4 V, but the trigger voltage for Mn2 entering into its snapback region is also significantly reduced if there is a triggering current into its base.

The overall dc I–V curve around the trigger point of the whole substrate-triggered input ESD protection circuit with the FOD in Fig. 2 is measured and shown in Fig. 7, which is the combination of the dc I–V curves of the FOD, the nMOS Mn1, and the substrate resistance. In Fig. 7, the trigger voltage of the input ESD protection circuit has been significantly reduced to only 6.4 V by the substrate current generated from the short-channel-length nMOS Mn1. The turn-on efficiency of the FOD to discharge ESD current is, therefore, enhanced by the substrate-triggered design. This input ESD protection circuit with the substrate-triggered FOD can provide effective voltage-clamping function to protect the thin gate oxide of 50 Å in the 0.25-μm salicided CMOS technology.

B. Transmission-Line Pulsing (TLP) Measurement

To investigate the turn-on behavior of the device during high ESD current stress, the TLP technique has been widely used to measure the second breakdown characteristics of devices [24], [25]. The transmission-line pulse generator (TLPG) with a pulse width of 100 ns is used to find the second breakdown current (It2) of the fabricated FOD and nMOS devices under different substrate biases.

When the human-body-model (HBM) ESD stress zapping on the input pad is greater than the It2 of the input ESD protection circuit, the input ESD protection circuit will be permanently damaged by the overstress current. By adjusting the device dimensions of the FOD (or the nMOS Mn2), the It2 can be proportionally increased and, thus, the ESD robustness of the input ESD protection circuit can be adjusted. Two important device layout parameters, which have a strong effect on the

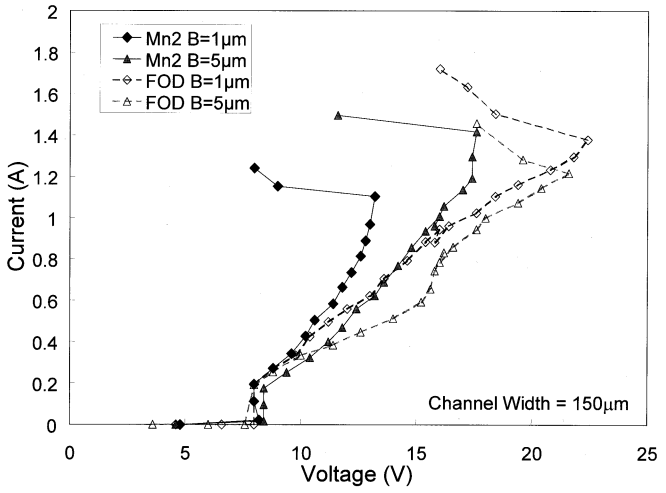


Fig. 8. TLP-measured I–V curves of the proposed input ESD protection circuits with nMOS Mn2 or FOD under different B spacings.

HBM ESD level of the input ESD protection circuit, are the B spacing in Fig. 4 (Fig. 5) and the total channel width of the FOD (or the nMOS Mn2) in the input ESD protection circuits. The TLP-measured I–V curves of the input ESD protection circuits with the FOD in Fig. 4, with Mn2 in Fig. 5, under different B spacings but with the same channel width of 150 μm, are shown in Fig. 8. From the TLP-measured It2 in Fig. 8, the dependences of It2 on the B spacing of the input ESD protection circuits with the FOD or nMOS Mn2 are shown in Fig. 9(a), where the channel width for the FOD and Mn2 is kept at 150 μm. When the B spacing is increased from 1 to 5 μm, the It2 of the input ESD protection circuit with the FOD is slightly decreased from 1.38 to 1.22 A. But the It2 of the input ESD protection circuit with nMOS Mn2 is increased from 1.11 to 1.42 A, when the B spacing is increased from 1 to 5 μm. The dependence of secondary breakdown current on the channel width of the FOD or nMOS Mn2 in the input ESD protection circuits is shown in Fig. 9(b), where the B spacing for the FOD and Mn2 is kept at 2 μm. The FOD or nMOS Mn2 with a longer channel width can sustain a higher secondary breakdown current.

In Fig. 5 with the nMOS Mn2 device, the effective turned-on region of the parasitic LBJT in Mn2 is distributed among the substrate under the gate of Mn2 and the surface channel of Mn2. The B spacing will modify the turn-on characteristics of the parasitic LBJT in the proposed circuit. The parasitic LBJT with different turn-on resistance and turn-on region has different ESD robustness [26]. The nMOS device with a shorter B spacing and LDD structure can strongly affect the electric field distribution near its surface channel during ESD stress. However, the turn-on region of the nMOS with a longer B spacing is more easily distributed far away from its surface channel [26]. Therefore, the nMOS with a longer B spacing has a higher It2, as that shown in Fig. 9(a). But the longer B spacing in Fig. 4 with the FOD can only cause a larger turn-on resistance along the ESD current discharging path, because there is no gate structure to generate the surface channel in the FOD. Therefore, the FOD with a longer B spacing has a slightly lower It2, as shown in Fig. 9(a). Because of the different turn-on characteristics between the FOD and nMOS devices under ESD stress, the proposed ESD protection circuits with the substrate-triggered FOD or Mn2 under different B spacings will have different ESD robustness.

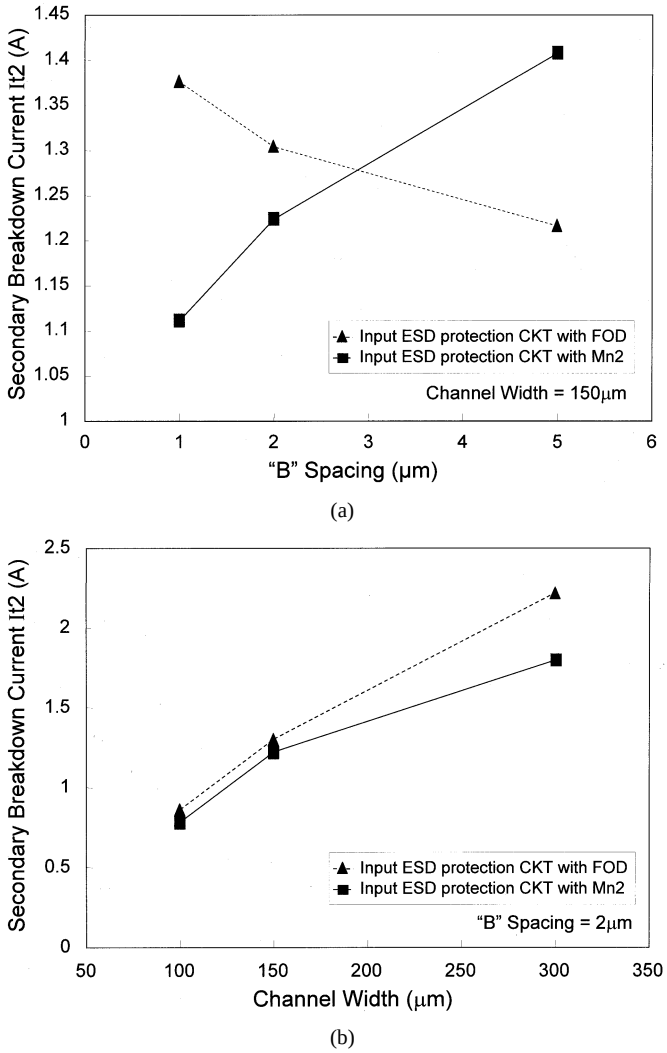


Fig. 9. Comparisons on the TLP-measured It2 of the input ESD protection circuits with the FOD or Mn2 devices under (a) different B spacing but with a fixed channel width of 150 μm and (b) different channel width but with a fixed B spacing of 2 μm.

C. ESD Test

The ZapMaster ESD tester, produced by Keytek Instrument Corporation, is used to investigate the HBM ESD level of the fabricated test chip. The failure threshold is generally defined as the minimum ESD stress to cause the leakage current greater than 1 μA under 1.1 $\times$ $V_{\rm DD}$ bias. In this 0.25-μm CMOS process, the core circuits are operated with 3.3-V $V_{\rm DD}$ bias. So, the failure criterion is defined as 1-μA leakage current under 3.63-V voltage bias. The fabricated input ESD protection circuits with the substrate-triggered FOD or Mn2 are verified by the HBM ESD test. To compare with the traditional design, the input ESD protection circuit with ggnMOS is also tested as a reference. The HBM ESD test results are shown in Fig. 10(a) for the devices with different B spacing but a fixed channel width of 150 μm and in Fig. 10(b) for the devices with different channel width but a fixed B spacing of 2 μm.

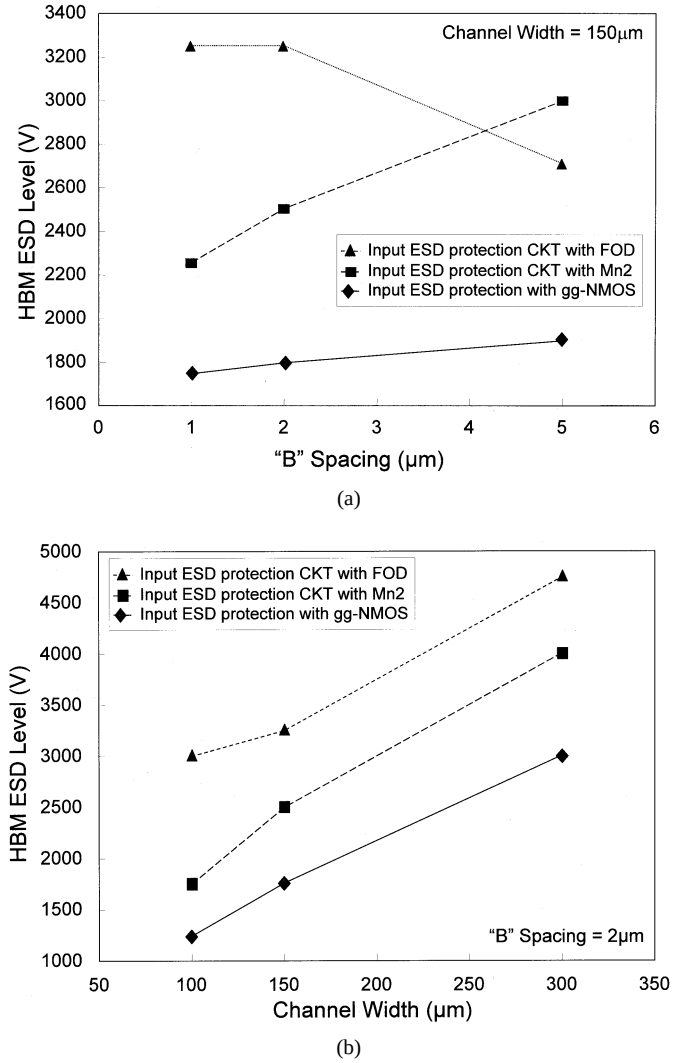


Fig. 10. Comparisons on HBM ESD levels of the input ESD protection circuits with the substrate-triggered FOD, substrate-triggered Mn2, or the traditional ggnMOS, under (a) different B spacing but with a fixed channel width of 150 μm and (b) different channel width but with a fixed B spacing of 2 μm.

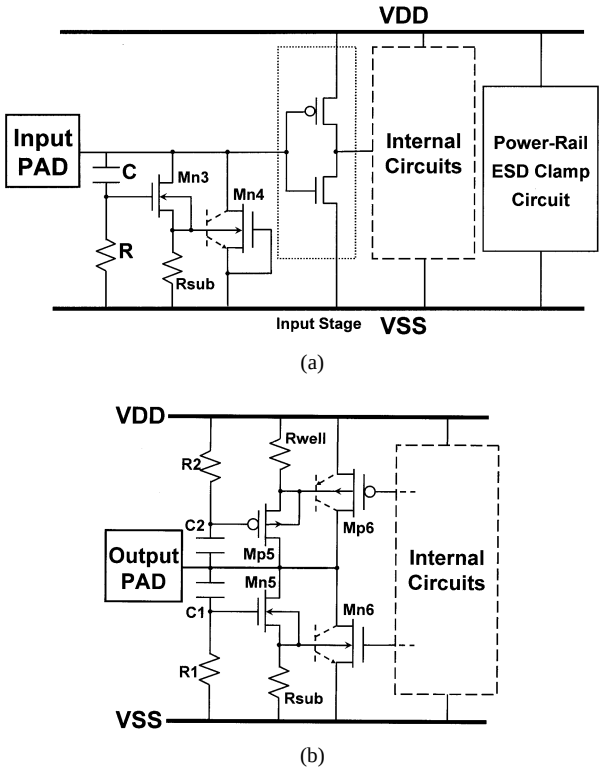


Fig. 11. Modified design of substrate-triggered ESD protection circuits with enhanced turn-on speed for (a) input and (b) output pins of IC products in deep-submicron CMOS process without using extra process modification.

In Fig. 10(a), the HBM ESD levels of the input ESD protection circuit with the FOD ($W = 150$ μm) is decreased from 3250 to 2750 V, when the B spacing in the FOD is increased from 1 to 5 μm. But the HBM ESD level of the input ESD protection circuit with nMOS Mn2 ($W = 150$ μm) is increased from 2250 to 3000 V, when the B spacing in nMOS Mn2 is increased from 1 to 5 μm. This tendency is consistent with that verified by the TLP-measured It2 in Fig. 9(a). With a B spacing of 2 μm, the input ESD protection circuit with the FOD in a silicon area of 1725 μm^2 can sustain an ESD level of 3250 V, but that with Mn2 in the same silicon area can only sustain an ESD level of 2500 V. The ggnMOS with a channel length of 2 μm and the same channel width of 150 μm in a silicon area of 1328 μm^2 can only sustain an HBM ESD level of 1800 V. The proposed ESD protection circuit with the FOD has the highest ESD robustness per unit silicon area of 1.73 V/μm^2, as compared with that of Mn2 with 1.33 V/μm^2 and that of ggnMOS with 1.2 V/μm^2. The HBM ESD level per silicon area of the input ESD protection circuit with the substrate-triggered FOD (Mn2) is increased 44% (11%) more than that with the traditional ggnMOS.

In Fig. 10(b), the ESD robustness of the input ESD protection circuits with the FOD or Mn2 is increased, as the total channel width of the FOD or Mn2 is increased from 100 to 300 μm. The tendency of ESD robustness on the channel width in Fig. 10(b) is also consistent to the TLP-measured It2 in Fig. 9(b).

IV. Modified Design to Enhance Turn-On Speed

To enhance the turn-on speed of the proposed input ESD protection circuit for effective protection of the much thinner gate oxide of the input stage in the sub-0.25-μm CMOS processes, a modified design on the input ESD protection circuit with substrate-triggered nMOS Mn4 (or FOD) is shown in Fig. 11(a). When a positive ESD voltage is zapping on the input pad, the gate of nMOS Mn3 will be coupled with a positive voltage through the *RC* gate-coupled circuit [17]. Because the trigger voltage of nMOS Mn3, which is turned on by gate-coupled circuit, is much smaller than the snapback breakdown voltage of nMOS Mn1 in the input ESD protection circuit of Fig. 3, the nMOS Mn3 in this modified ESD protection circuit can be quickly turned on to conduct a triggering current into the substrate of nMOS Mn4. Therefore, the parasitic LBJT in nMOS Mn4 (or FOD) can be quickly triggered on to discharge ESD current from input pad to V_{SS}. So, this modified design can effectively enhance the turn-on speed of the proposed substrate-triggered input ESD protection circuits.

The proposed substrate-triggered technique can be also used to improve the ESD robustness of the output stage. The substrate-triggered output ESD protection circuit with enhanced turn-on speed is shown in Fig. 11(b). The pMOS Mp6 and nMOS Mn6 of the output buffer in the integrated circuit are also used as ESD protection devices. During positive-to-V_{SS} ESD stress, the circuit with C1–R1 and nMOS Mn5 are used to detect the positive ESD transition and to conduct the triggering current into the substrate of Mn6. The ESD current is discharged from the output pad to grounded V_{SS} through the turned-on output nMOS Mn6. During negative-to-V_{DD} ESD stress, the circuit with C2–R2 and pMOS Mp5 are used to detect the negative ESD transition and to conduct a negative triggering current into the n-well of Mp6. The negative ESD current is discharged from the output pad to grounded V_{DD} through the turned-on output pMOS Mp6. Under negative-to-V_{SS} (positive-to-V_{DD}) ESD stress condition, the p-n junction in the drain region of the output nMOS Mn6 (pMOS Mp6) is operated in forward-biased condition to discharge ESD current. Therefore, the output buffer can sustain a much higher ESD level in the negative-to-V_{SS} and positive-to-V_{DD} ESD stresses. With this substrate-triggered design, the gates of output nMOS Mn6 and output pMOS Mp6 are not interfered by the ESD detection circuit. The gates of output buffer can be fully controlled by the predriver of the internal circuits. So, the proposed substrate-triggered design is more feasible for using to protect the output buffers with complex gate-control circuits, such as the slew-rate-controlled output buffer.

The proposed substrate-triggered ESD protection circuits with gate-coupled technique can provide fast turn-on speed and high ESD robustness for the input and output pins of IC products in deep-submicron CMOS processes without using extra process modification. This substrate-triggered technique can also be applied in the power-rail ESD clamp circuit to further improve ESD robustness and turn-on speed for effective protection of the internal circuits of an IC. Some successful design examples have been reported in [27] and [28].

V. Conclusion

The proposed ESD protection circuit using the substrate-triggered technique has been practically verified in a 0.25-μm salicided STI CMOS process without extra silicide-blocking and ESD-implantation modifications. The trigger voltage of the proposed input ESD protection circuit with the FOD is lowered from the original 11.9 V to only 6.4 V, so it can be quickly turned on to effectively protect the thin gate oxide (50 Å) of the input stage in the 0.25-μm salicided CMOS process. The whole ESD protection circuit can be drawn into a compact layout structure to enhance the substrate-triggered efficiency and to save the occupied silicon area. Comparing to the traditional ESD protection design with ggnMOS, the ESD level per silicon area of the proposed input ESD protection circuits with the FOD (or nMOS Mn2), under the B spacing of 2 μm and the channel width of 150 μm, can be increased 44% (or 11%). To further enhance the turn-on speed of the input or output ESD protection circuits during ESD stress, the gate-coupled technique can be merged into the substrate-triggered ESD protection circuits. So, the proposed substrate-triggered ESD protection design can be still suitable for use in protecting the input and output stages of ICs in future nanoscale CMOS technology.

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