High-Performance P-Channel Schottky-Barrier SOI FinFET Featuring Self-Aligned PtSi Source/Drain and Electrical Junctions

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***Abstract*—A simplified and improved Schottky-barrier metal–oxide–semiconductor device featuring a self-aligned offset channel length, PtSi Schottky junction, and reduced oxide thickness underneath the sub-gate was proposed and demonstrated. To alleviate the drawbacks related to the nonself-aligned offset channel length in the original version, a self-aligned offset channel length is achieved in the new device by forming the silicide source/drain junction self-aligning to the sidewall spacers abutting the gate. This results in not only one mask count saving but also better device performance, as facilitated by the reduced offset channel length of the self-aligned sidewall spacers. Moreover, the adoption of PtSi for the Schottky junction further improves the on-state current of p-channel operation, while a thinner oxide employed underneath the sub-gate effectively reduces the sub-gate bias needed to form the electrical junction to below 5 V. Significant improvement in on-current as well as leakage current reduction is achieved in the new improved device.**

***Index Terms*—Ambipolar, Schottky barrier, silicon-on-insulator (SOI).**

A SCHOTTKY-BARRIER metal–oxide–semiconductor (SB MOS) transistor [1] has been proposed as a potential candidate for future nanoscale device applications [2]. The SB MOS devices are simpler in fabrication and compatible with low-temperature processing, compared with conventional MOS transistors, by using metal silicide, in lieu of the heavily doped region, to serve as the source/drain (S/D). Recently, we reported a novel Schottky-barrier silicon-on-insulator (SOI) FinFET with $CoSi_2$ source/drain and electrical junctions induced by a sub-gate (right side of Fig. 1) [3]–[5]. Excellent ambipolar characteristics with near-ideal subthreshold swing ($\sim$ 60 mV/dec) and high on/off current ratio $(> 10^8)$ have been demonstrated for both n-channel and p-channel operations on a single device for the first time. Nevertheless, the on-state current is compromised by the long offset channel length due to the nonself-aligned nature in the original structure, as well as the large barrier heights for both holes and electrons with the $CoSi_2$ junction. Further, it is also highly desirable to reduce the sub-gate bias of 7.5 $\sim$ 10 V required in the previous work. To alleviate the above shortcomings, we have explored a modified device structure with self-aligned offset channel region. In addition, we have adopted a low-barrier silicide material (e.g., PtSi, barrier height for hole $\sim$ 0.24 eV [6]) in device fabrication, and also incorporated a thinner oxide underlying the sub-gate.

Fig. 1 depicts key process flows for fabricating the new (left side) and original (right side) devices. The starting materials were boron-doped 6-in SOI wafers with background doping of around 5×10^{15} cm^{-2}. The nominal SOI and buried oxide layer thicknesses of the starting wafers were 200 and 330 nm, respectively. For device fabrication, the thickness of SOI layer was first thinned down to 80 nm by thermal oxidation and wet etching. The device island (including S/D contact regions and Si fins [7]) was then formed on the substrate by electron-beam (e-beam) lithography, which was employed extensively for device patterning throughout the fabrication. Next, a 2.2-nm gate oxide and an *in situ* doped n^+ poly-Si (150-nm) films were deposited sequentially on the surface. The polysilicon gate was then patterned and etched by a high-density plasma etcher with an etching selectivity to the underlying oxide layer of larger than 100 [Fig. 1(a)]. A 20-nm tetra-ethyl-ortho-silicate (TEOS) oxide layer was then deposited by low-pressure chemical vapor deposition (LPCVD), and patterned to define the offset channel (i.e., S/D extension) regions. Pt salicide process was subsequently performed to form PtSi in the exposed S/D regions [Fig. 1(b)]. Next, a 20-nm TEOS oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD), followed by contact hole and aluminum pad/sub-gate formation [Fig. 1(c)]. Finally, wafers were annealed in forming gas at 400 °C. Electrical characterizations were performed on the completed devices using an HP4156A semiconductor analyzer.

It is worth noting here that the offset channel length is set by the sidewall spacer with a bottom width of around 15 nm in the new self-aligned structure (Fig. 2 , right side, denoted as SA structure). Compared to the original nonself-aligned (NSA) structure (Fig. 2, left side), the new SA device features a smaller offset length. It also saves one e-beam lithographic step during fabrication. It is also worth noting here that the thickness of the PE-TEOS layer underlying the sub-gate has been reduced to 20 nm [Fig. 1(c)], from 40 nm used in previous study [3]–[5]. The proper sub-gate bias is, thus, reduced from the previous 7.5 $\sim$ 10 V to 5 $\sim$ 6 V in this work. Fig. 2 shows the schematic

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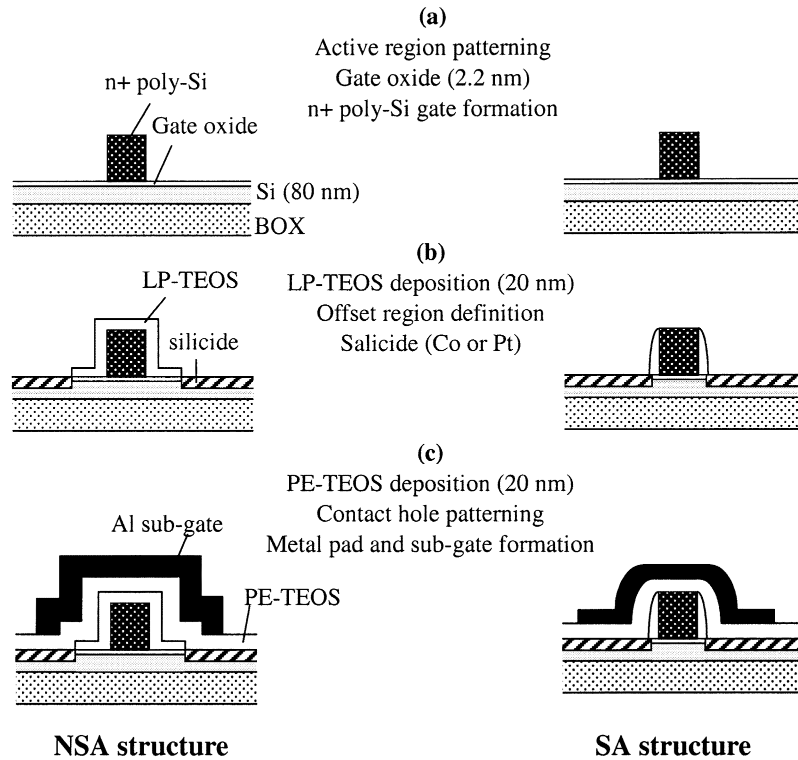

Fig. 1. Key process flows for device fabrication.

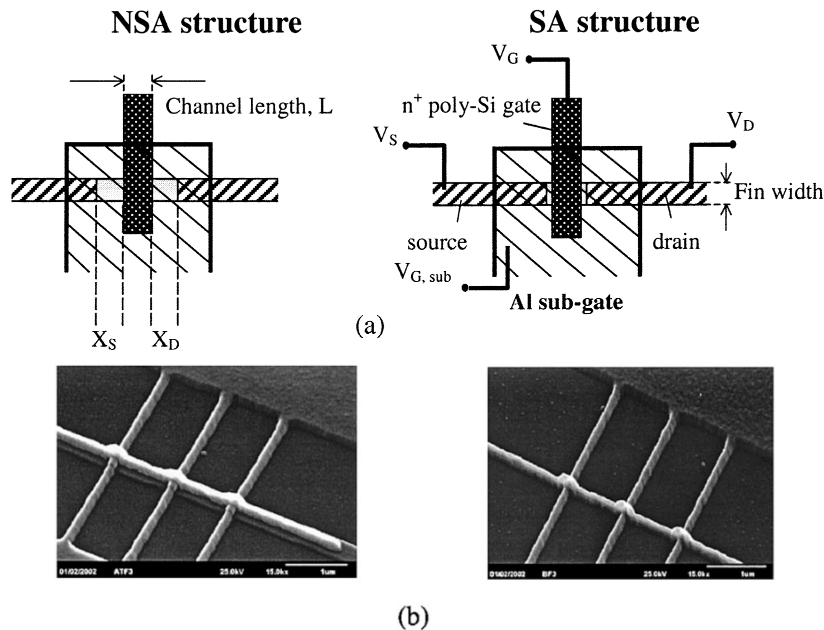

Fig. 2. (a) Schematic top views of the new SA (right) and original NSA (left) devices. (b) SEM pictures for SA (right) and NSA (left) devices before salicide step.

top views and scanning electron microscope (SEM) pictures of the SA and NSA devices. Offset length for the NSA devices (X_D and X_S) characterized in this work is fixed at 100 nm.

Fig. 3(a) and (b) shows the effects of sub-gate bias on the p-channel operation of NSA and SA devices, respectively. It can be seen that the application of a proper sub-gate bias not only greatly improves the on-state current, but also effectively reduces the off-state leakage. Extremely high on/off ratio (up to 10^9) could, thus, be achieved. This trend is basically similar to that for devices with $CoSi_2$ S/D presented in our previous study [3]–[5]. Based on the analysis done in our former work [5], this could be ascribed to the suppression of field emission of electrons from the drain junction, which is the major leakage mechanism at $V_{G,sub} = 0$. It can also be seen that extremely high on/off ratio (up to 10^9) is achieved in this work.

Output characteristics for the NSA and SA devices are shown and compared in Fig. 4. Note that the drain current has been normalized to the effective width, i.e., the sum of the Si fin width

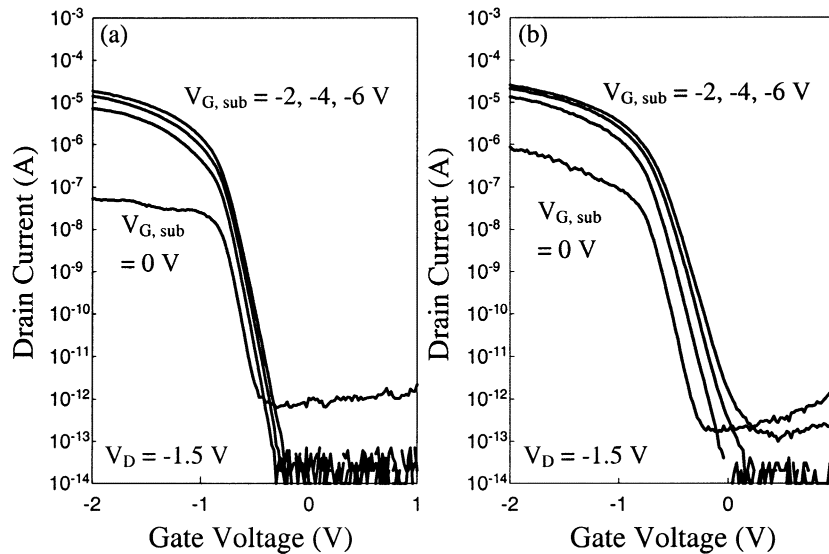

Fig. 3. Effects of sub-gate bias on the p-mode operation of: (a) NSA and (b) SA devices with Pt silicide S/D (L $= 110$ nm; Fin width $= 50$ nm; Fin number $= 1$).

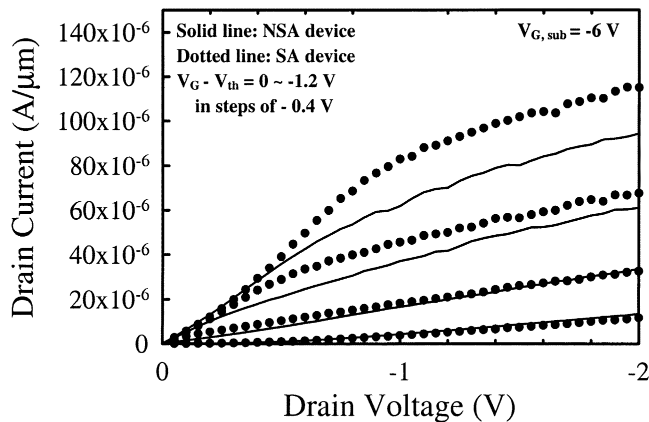

Fig. 4. P-mode output characteristics of NSA and SA devices with Pt silicide S/D. (L $= 110$ nm; Fin width $= 50$ nm).

(Fig. 2) plus twice the Si thickness (80 nm). It is observed that the SA device exhibits drain drive current larger than the NSA device when both V_D and V_G are high. Nevertheless, the drain current becomes nonsensitive to the structure when either V_D or V_G is low. This might be due to the fact that the thermionic emission of holes at the source dominates the conduction in the low-voltage regime, thus, the advantage of using the SA structure to reduce the parasitic resistance of the offset channel is not significant.

When comparing with the NSA device with $CoSi_2$ S/D (data not shown), more than five times increase in on-current (when V_D and V_G are both high) has been achieved for the SA device shown in Fig. 4. These results indicate that the use of SA scheme, combined with the low barrier-height silicide, results in significant improvement in the device performance. It should also be noted that such improvement is not observed in n-channel operation. The performance of n-channel operation for the fabricated devices is significantly degraded compared with those having $CoSi_2$ S/D. This is reasonable because the barrier height of electrons at PtSi–Si junction is high (> 0.8 eV).

In summary, a self-aligned scheme that enhances on-state current and saves one mask count was proposed and demonstrated for SB FinFETs. In addition, PtSi was adopted for the Schottky junction, and shown to further improve the on-state current of p-channel operation. Finally, by thinning the underlying oxide, it was demonstrated that the sub-gate bias can be reduced to 5 V. Further reduction is feasible if a high-k material with the same physical thickness is used.

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REFERENCES

[1] M. P. Lepselter and S. M. Sze, "SB-IGFET: an insulated-gate field-effect transistor using Schottky-barrier contacts for source and drain," *Proc. IEEE*, vol. 56, pp. 1400–1401, Oct. 1968.

[2] J. R. Tucker, C. Wang, and P. A. Carney, "Silicon field-effect transistor based on quantum tunneling," *Appl. Phys. Lett.*, vol. 65, pp. 618–620, 1994.

[3] H. C. Lin, M. F. Wang, F. J. Ho, J. T. Liu, F. H. Ko, H. L. Chen, G. W. Huang, T. Y. Huang, and S. M. Sze, "Nano-scale implantless Schottky-barrier SOI FinFET's with excellent performance," in *Tech. Dig. 60th Annu. Device Research Conf. (DRC)*, Santa Barbara, CA, June 2002, pp. 45–46.

[4] H. C. Lin, M. F. Wang, F. J. Ho, J. T. Liu, T. Y. Huang, and S. M. Sze, "Application of field-induced Schottky MOS to fin-like body FET," *Jpn. J. Appl. Phys.*, vol. 41, pp. L626–L628, June 2002.

[5] H. C. Lin, M. F. Wang, F. J. Ho, J. T. Liu, Y. Li, T. Y. Huang, and S. M. Sze, "Effects of sub-gate bias on the operation of Schottky-barrier SOI MOSFET's having nano-scale channel," in *Proc. IEEE Conf. Nanotechnology (NANO)*, Washington, DC, Aug. 2002, pp. 205–208.

[6] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20-nm gate-length regime," in *Int. Electron Devices Meeting Tech. Dig.*, 2000, pp. 57–60.

[7] D. Hisamoto, W. C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T. J. King, J. Bokor, and C. Hu, "A folded-channel MOSFET foe deep-sub-tenth micron era," in *Int. Electron Devices Meeting Tech. Dig.*, 1998, pp. 1032–1034.