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Room temperature two-terminal characteristics in silicon nanowires

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Abstract

Quantum effects in silicon nanowires due to one-dimensional carrier confinement were observed at room temperature. Electrical transport properties were measured on narrow thin-silicon-on-insulator wires that were defined by e-beam lithography and further narrowed and thinned down by oxidation to a final thickness of around 3 nm, and a width of 29 nm. The room temperature current–voltage characteristics of the resulting silicon nanowires are shown to exhibit a zero current state may be due to the occurrence of Coulomb blockade.

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Keywords: A. Nanostructures; B. Nanofabrications; D. Tunnelling

1. Introduction

When the dimensions of a semiconductor sample are reduced to the nanometer regime, small-dimensional effects involving quantization come into play. These effects, which manifest themselves in the form of conductance oscillations [1], appear at nanometer-scale dimensions at room temperature. To understand the size-quantization effects in semiconducting materials, semiconductor nanostructures have been studied extensively in the past two decades. Single electron and Coulomb blockade effects [1] have been revealed in mesoscopic low-dimensional structures. Yano et al. demonstrated Coulomb blockade effects in polycrystalline silicon structures [2]. In their work, the film thickness was sufficiently thin and nonuniform so a natural potential difference occurs between the individual Si grains. Ng et al. reported the observation of Coulomb blockade effects at no higher than 70 K in hydrogenated amorphous silicon recrystallized by electron beam annealing [3]. In their work, Coulomb blockade effect was modeled as a combination of hopping conduction between a limited number of trapping sites in amorphous regions or at grain boundaries with additional Coulomb blockade effects, as well as confinement due to potential fluctuations arising from dopant distribution. Concurrently, because silicon-on-insulator (SOI) structure is an efficient method for obtaining thin device thickness and can effectively remove the undesirable bulk effect of Si wafer, many works on devices based on SOI wafers made from separation by implanted oxygen (SIMOX) method have recently been reported [4–7]. In this paper, we present our experimental work using electron-beam direct writing combined with oxidation to fabricate narrow thin wires on SIMOX wafer. The final width and thickness of the wires are 29 and 3 nm, respectively. Two-terminal characteristics were demonstrated at room temperature in the conducting silicon quantum wires.

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2. Experimental

The silicon nano wires in this study were fabricated using SIMOX wafers fabricated on ⟨100⟩ p-type Si substrates, with a thin 60 nm silicon layer on top of a 400 nm buried SiO_2. After depositing a 10 nm capping oxide, the top silicon layer was doped by phosphorous ion implantation at a dose of 2×10^{14} ions/cm^2 and with energy of 40 kV. The doping level is sufficiently high so that the layer depicts metallic behavior, as is indicated by a significant drop in silicon sheet resistance to around 965–1118 Ω. The silicon layer was thinned down by a sacrificial oxidation and subsequent oxide strip. E-beam direct writing by a Leica Weprint 200 system with NEB22A electron-beam resist was then employed to define 80 nm-wide lines, with various lengths of 0.5, 1, and 3 μm, respectively. Next, the silicon layer was further thinned and narrowed down again, and a 20 nm gate oxide was then grown at 925 °C for 43 min in oxygen which further reduce the silicon wires' thickness and width. Aluminum metal film was then deposited and patterned to provide electrical contact to the structure. Fig. 1(a) shows a schematic of the fabricated Si wires. The corresponding scanning electron microscope photograph is shown in Fig. 1(b). W, L, and d denote the wire width, length, and thickness, respectively.

To characterize structural aspects of the Si wire, high-resolution transmission electron microscopy (HRTEM) was employed. The HRTEM examination was carried out with a JEOL-4000EX electron microscope operated at 400 kV. A HP4156C precision semiconductor parameter analyzer was used to measure the electrical properties both at 300 and 31 K. The low temperature measurements were performed in liquid He cryogenic probing system (SCT-66 MDC, NAGASE). The current–voltage characteristics were measured with symmetric dc voltage bias V_{ds} varied between −2 and +2 V. Cross-sectional HRTEM image of a narrow silicon wire profile along AA′ (see Fig. 1) after oxidation at 925 °C for 43 min is shown in Fig. 2. An abrupt interface between the oxide and the silicon is observed. The HRTEM image shows a dark, orderly region as well as gray regions in the sample. From the observation of the enlarged TEM image (bottom part of Fig. 2), the dark orderly 'lattice-like' region is mainly composed of nanocrystalline Si regions, which are separated by the gray regions. The gray counterparts are the SiO_2 amorphous phase. The separation between crystalline planes in the images was measured and estimated to be ~5 Å, which is in excellent agreement with the Si lattice constant of 5.43 Å. The lateral crystallite dimensions $d \sim 3$ nm and $W \sim 29$ nm are confirmed by the cross-sectional view in Fig. 2.

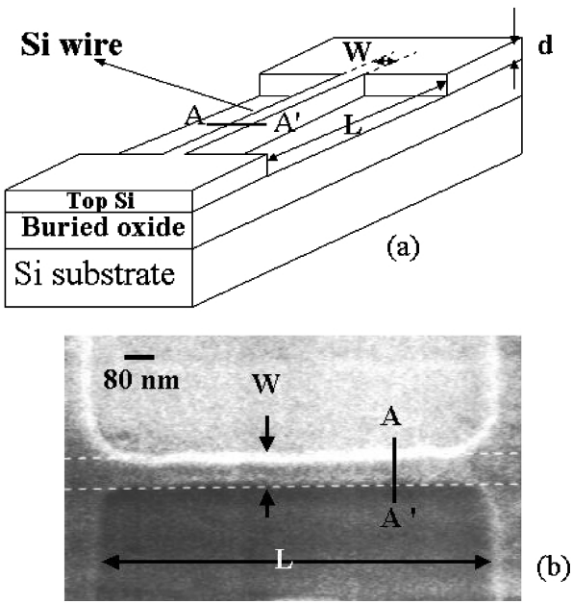

Fig. 1. (a) Schematic diagram of Si quantum wire and (b) the corresponding SEM photograph.

3. Results and discussion

I–V characteristics measured at $T = 31$ K as a function of source–drain bias for narrow wires with various lengths are shown in Fig. 3. All wires have active $W \sim 29$ nm and $d \sim 3$ nm. It can be seen that all wires, irrespective of their length, depict very low current in a considerable voltage range around zero bias. Moreover, the measurements of source–drain current at $T = 300$ K, which are plotted in Fig. 4, also exhibit zero current state around zero bias. This phenomenon observed at 300 K is similar to that at 31 K. Under higher bias conditions the current depict a

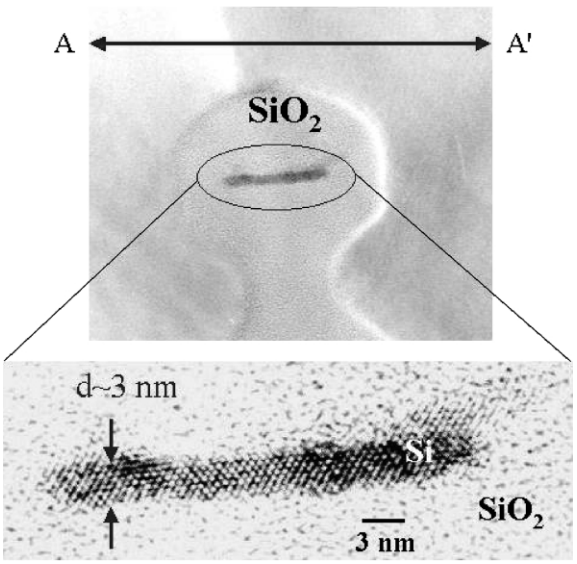

Fig. 2. Cross-sectional views of a HRTEM observation of silicon nano wire profile along AA′ (as shown in Fig. 1). Lateral crystallite dimensions with $d \sim 3$ nm and $W \sim 29$ nm are confirmed.

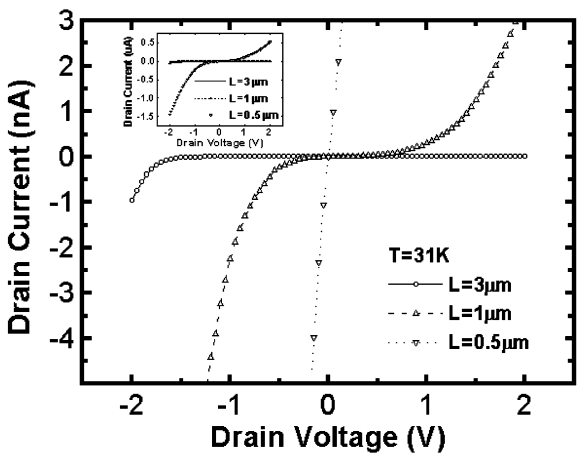

Fig. 3. Current–voltage characteristics measured at 31 K of silicon quantum wires with various lengths of 0.5, 1, and 3 μm. Insert shows the enlarged portion in the region around 0 V for 0.5 μm-long wire, illustrating the value of the offset voltage.

linear function of the applied voltage. A clear tendency is observed that, with the same thickness and width, a longer wire gives rise to a higher low current region. In other words, the size of the zero current state is significantly decreased while the overall conductivity increases for wires with smaller length. Specifically, from the distance between the first conductance peak, zero current state of 0.1, 0.3, and 1.5 V were found for wire length of 0.5, 1, and 3 μm, respectively.

The effects of a capacitively coupled gate on the transport properties of nano wires were also found. The gate electrode was formed by a probe tip, which was placed in direct contact with the oxide on top of the 1 μm-long wire. The drain–source current–voltage characteristics at room temperature of a wire with active width ~29 nm and thickness ~3 nm were measured with different gate voltages $V_G = 0, -5$, and -10 V, respectively. The results are shown in Fig. 5. Due to the relatively thick oxide ~500 nm used in this study, the gate coupling was weak. Nevertheless, it can be seen clearly that a more negative gate bias leads to a wider blockade region. It seems that the effect of the gate is a field effect, perturbing or narrowing the conductance channel. The increase in resistance with length, leading to significant current suppression at low bias, can be due to multiple tunneling between the nanocrystallites along the wire, where each may involve a charge effect. In addition, some peaks were observed in the differential conductance that separates the low current range from the tunneling region. When the drain bias is sufficiently high, the low current range of the current through the wire can be lifted due to the additional energy. Therefore, the electrons can occupy states at higher orbital in the confined quantum wire and opening of a large energy window for tunneling. Fig. 6 shows the corresponding tunneling spectra (dI/dV vs. V). The tunneling spectra appear to be asymmetrical with peaks in the positive and negative bias region. The conductance peaks in the positive bias region as shown in Fig. 6 is much higher and better resolved than the peaks in the negative bias region. It should be noted that the conductance, on the other hand, increases more rapidly at negative bias than at positive bias. Electron transport in Si nanocrystallites is complicated due to the coexistence of amorphous and crystalline phases, dopants, traps, etc. Assuming a complete suppression of the potential fluctuations, the observed low current regime could only be attributed to quantum confinement and unintentional inhomogeneous effects [8–12], as they only depend on the geometry and the exact location of the impurities and are not only affected by the applied gate voltage.

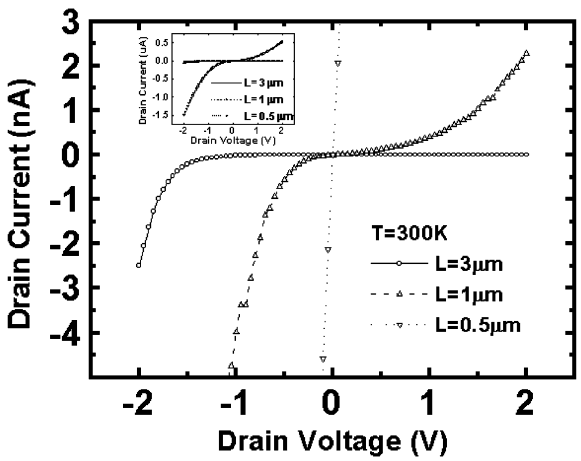

Fig. 4. Current–voltage characteristics measured at room temperature (300 K) of silicon quantum wires with various lengths of 0.5, 1, and 3 μm. Insert shows the enlarged portion in the region around 0 V for 0.5 μm-long wire, illustrating the value of the offset voltage.

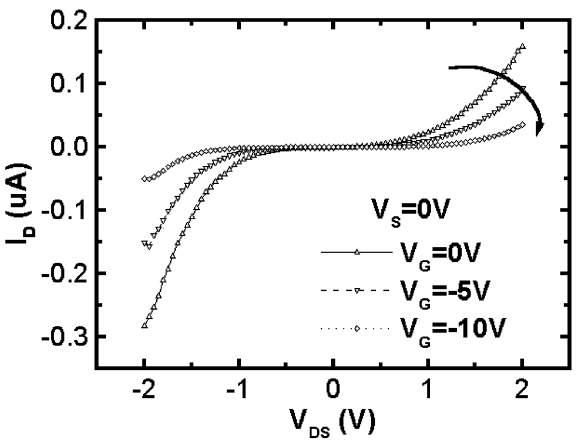

Fig. 5. Current–voltage characteristics measured at room temperature (300 K) of silicon wire with various gate voltage of 0, −5, and −10 V. The wire length is 1 μm.

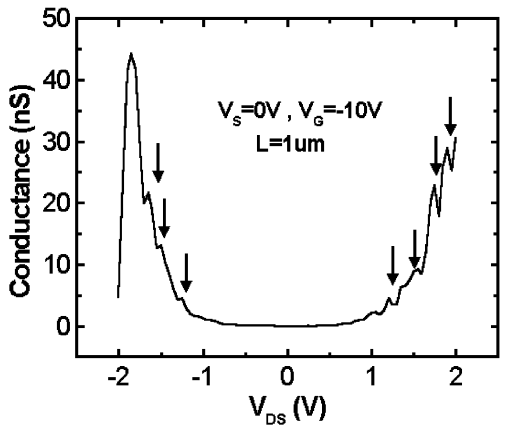

Fig. 6. Conductance (dI_D/dV_D) oscillations plotted as a function of V_{DS} for 1 μm-long wire measured at room temperature. V_G is fixed at −10 V.

4. Conclusions

We have fabricated extremely narrow thin silicon wires on SIMOX wafers. The highly doped Si layer was accomplished using phosphorous ion implantation and annealing. The lateral crystallite dimension, 3 nm × 29 nm, is confirmed by cross-sectional view of HRTEM image. Two-terminal characteristics were observed in the structure not only at 31 K but also at the room temperature.

Acknowledgements

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