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Ambipolar Schottky barrier silicon-on-insulator metal–oxide–semiconductor transistors

Horng-Chih Lin [a,*], Meng-Fan Wang [b], Chia-Yu Lu [b], Tiao-Yuan Huang [a,b]

[a] National Nano Device Laboratories, 1001-1 Ta Hsueh Road, Hsin-Chu 300, Taiwan
[b] Institute of Electronics, National Chiao Tung University, Taiwan

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Abstract

A novel Schottky barrier silicon-on-insulator metal–oxide–semiconductor field-effect transistor featuring metallic source/drain and an electrical drain junction has been fabricated and characterized. The formation of electrical drain junction, or the field-induced drain (FID), is controlled by a metal field-plate overlying the passivation oxide. Excellent ambipolar operation is demonstrated on the device. Specifically, on/off current ratios up to 10^8 and 10^7 are observed for p- and n-channel operations, respectively. Meanwhile, the off-state leakage current shows very weak dependence on the voltage difference between the main-gate and the drain, highlighting the effectiveness of FID. Finally, negative differential conductance effect is observed for n-channel operation, which is identified as due to dynamic hot electron trapping during device characterization.

Keywords: Schottky barrier; Silicon-on-insulator; Field-induced drain; Negative differential conductance

1. Introduction

Schottky barrier (SB) metal–oxide–semiconductor (MOS) transistor is an interesting and potentially useful device. First proposed by Lepselter and Sze in 1968 [1], the device employs a metallic source and drain (S/D) [1–5] to eliminate the source/drain implantation and subsequent annealing steps altogether. It is therefore much simpler in processing and inherently suitable for low temperature processing. Moreover, it is also capable of ambipolar (or bi-channel) operation [5]. With these advantages, it appears to be quite attractive for applications to nano-scale devices as well as large-area electronics.

Conventionally, SB MOS devices employ a self-aligned silicidation (salicide) process to form the silicided S/D. Oxide sidewall spacers abutting the gate are required to prevent bridging between the gate electrode and the silicided S/D [1–5]. However, the resultant SB MOS transistors generally suffer from severe leakage current and poor on/off current ratio. This is due to the much larger junction leakage current inherent in Schottky diodes compared to p–n junction diodes.

Recently, we proposed and demonstrated a novel SB poly-Si thin-film transistor (TFT) that exhibits excellent ambipolar operation performance [6–8]. The new device employs a field-plate (or sub-gate) to induce an electrical drain extension in the active layer. The unique field-induced drain (FID) feature reduces effectively the off-state leakage current, while maintaining a reasonable on-current, resulting in significant improvement in the device performance. On/off current ratios of around 10^6 were achieved for both n- and p-channel operations in our previous work. Device performance could be further improved by using silicon-on-insulator (SOI) wafers, since mono-crystalline Si substrates have better material properties than poly-Si substrates. Thus we carried out this study to fabricate and evaluate the performance of SB SOI devices with a FID structure.

* Corresponding author. Tel.: +886-3-572-6100.
E-mail address: hclin@ndl.gov.tw (H.-C. Lin).

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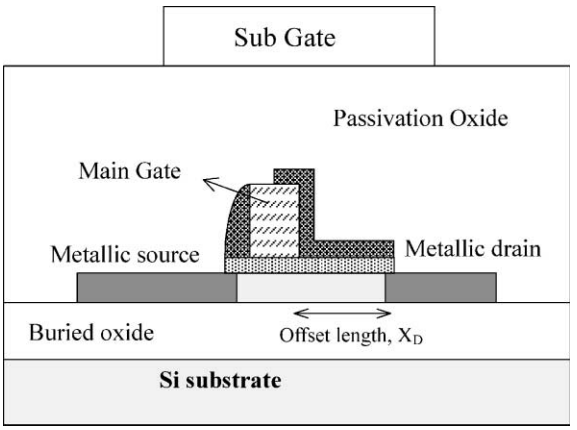

Fig. 1. Structure of the SOI SB MOS device.

2. Device structure and fabrication

The structure of the proposed SB SOI MOS transistor is illustrated in Fig. 1. For device operation, a fixed bias is applied to the sub-gate to form a FID extension under the sub-gate region. So, depending on the sub-gate bias polarity, the device can function both as n-channel and p-channel transistors with positive and negative sub-gate biases, respectively.

Fig. 2 shows key processing steps in the device fabrication. SIMOX wafers with 50-nm p-Si layer on 400 nm buried oxide (BOX) are used as the starting substrates. After patterning the active device region, a 6-nm thermal gate oxide and an n^+ poly-Si (200 nm) layer is deposited (Fig. 2(a)). The n^+ poly-Si gate layer is delineated to form the main-gate. Next, a 200-nm CVD oxide layer is deposited, followed by lithographic step to define the offset regions for SOI devices with FID (Fig. 2(b)). Then, the silicided source/drain is formed by a self-aligned silicidation (salicidation) treatment, by first depositing a thin Ni layer (30 nm), followed by a rapid-thermal annealing (550 °C, 30 s) step and a wet etching step in H_2SO_4:H_2O_2 = 3:1 to remove the non-reacted metals. It should be noted that neither the channel nor the source/drain region receives any deliberate doping, so no post-implant annealing step is necessary. Wafers then follows a standard back-end processing to completion. The metal sub-gate in the new structure is formed simultaneously with the regular metal patterning (Fig. 2(c)), so no extra processing step is required. A post-metal annealing at 400 °C in forming gas for 30 min is performed before electrical measurements.

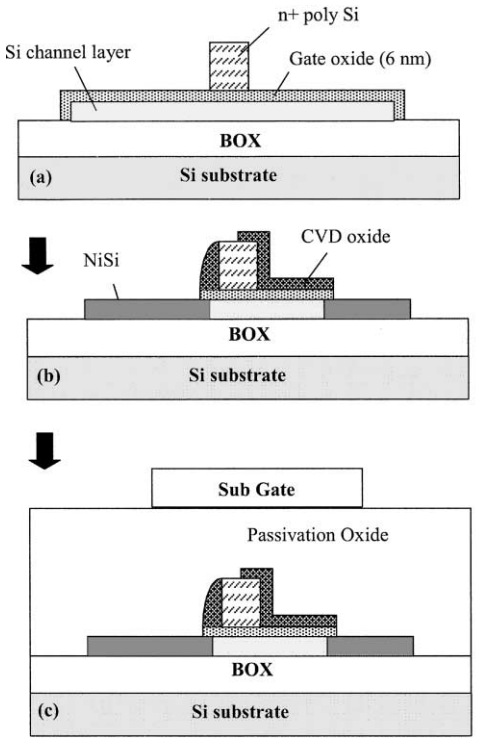

Fig. 2. Key device fabrication flow.

3. Results and discussion

Fig. 3 shows typical ambipolar sub-threshold characteristics of the FID SB SOI devices. High on/off current ratios of up to 10^7 and 10^8 are achieved for n- and

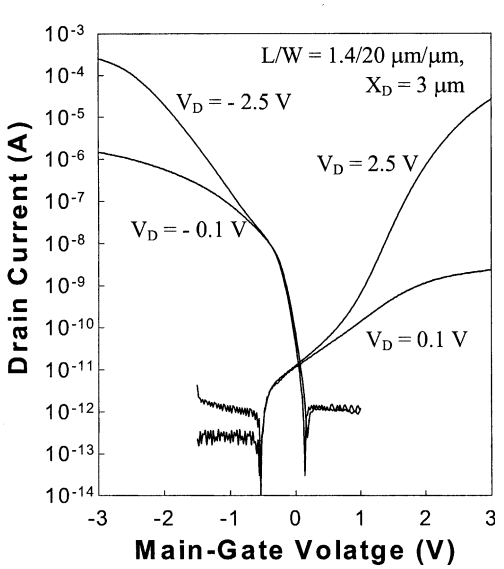

Fig. 3. Ambipolar sub-threshold characteristics of a SB MOS transistor. Sub-gate voltages are 30 and −30 V for n- and p-channel operations, respectively.

p-channel operations, respectively. In addition, the off-state leakage current shows only weak dependence on the gate bias, highlighting the effectiveness of FID. We also find that the drive capability is better for p-channel operation, which is reasonable since the barrier height for holes (~0.4 eV) is lower than that for electrons (~0.7 eV) [9] for the NiSi silicide used in this study.

Figs. 4 and 5 depict the effects of sub-gate bias on the drain current for n-($V_D = V_{G,main} = +2.5$ V) and p-channel ($V_D = V_{G,main} = -2.5$ V) operations, respectively. Since a large $|V_{G,main}|$ is applied, the channel region underneath the main-gate acts simply as a "pseudo-source", and the results can be regarded as the operation of a FET with the metal field-plate (or the sub-gate) serving as the transistor gate, while X_D becomes the transistor channel length. The transfer characteristics shown in these figures are, however, in strong contrast to the results shown in Fig. 3. The off-state leakage current is high, especially for n-channel operation, and shows strong dependence on the sub-gate bias in the off-state regime.

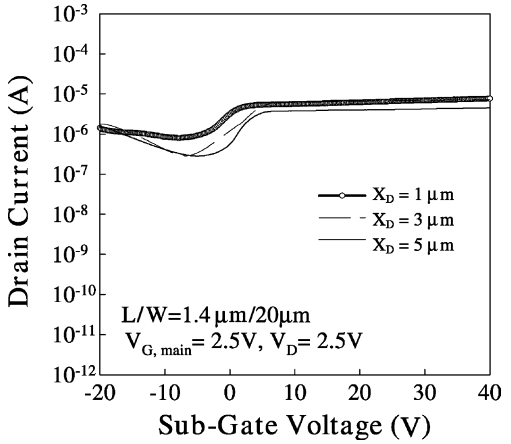

Fig. 4. Drain current as a function of sub-gate bias for n-channel operation. Main-gate and drain voltages are both 2.5 V.

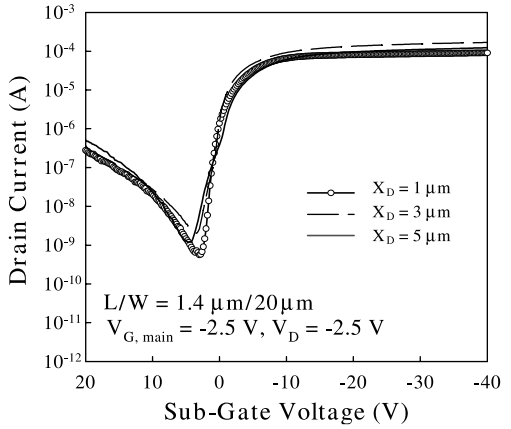

Fig. 5. Drain current as a function of sub-gate bias for p-channel operation. Main-gate and drain voltages are both −2.5 V.

The above characteristics may be explained using the band diagrams shown in Fig. 6 for four different n-channel operation ($V_D = +2.5$ V) conditions. The high off-state leakage in Fig. 4 ($V_{G,main} = +2.5$ V, $V_{G,sub} \ll 0$) is ascribed to the field emission of holes from the drain junction (Fig. 6(a)), which is reduced when $V_{G,sub}$ is increased to 0 V (Fig. 6(b)). When $V_{G,sub}$ is further increased to a high positive value corresponding to a normal on-state condition ($V_{G,main} = +2.5$ V, Fig. 6(c)), field emission of electrons from the source junction contributes to the drain output current instead [2–5]. On the other hand, when $V_{G,main}$ is switched to the off-sate (i.e., $V_{G,main} \sim 0$) while maintaining $V_{G,sub}$ at a high positive value, the FID in the offset channel region impedes the drain leakage (i.e., hole field emission) [6], as shown

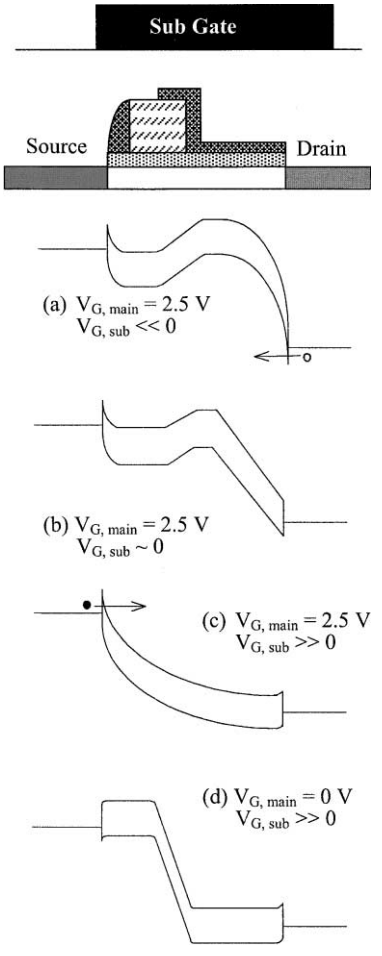

Fig. 6. Band diagrams along the channel for different n-channel operation conditions ($V_D = 2.5$ V).

in Fig. 6(d). As a result, extremely low off-state leakage (Fig. 3) is achieved.

Note that Fig. 6 illustrates the situation under n-channel operation, though similar mechanisms may be used for the case of p-channel operation. The major difference in the two channel modes arises from the difference in barrier height between holes and electrons, which explains why the on-current in Fig. 3 is lower for n-channel operation and the off-state leakage is higher in Fig. 4 than that in Fig. 5.

Drain output characteristics are shown in Figs. 7 and 8 for n- and p-channel operations, respectively. Contrary to the normal p-channel output characteristics, a negative differential conductance (NDC) behavior is clearly observed under n-channel operation when $V_{G,main}$ is higher than 4 V. This anomalous phenomenon may be ascribed to the dynamic electron trapping during device characterization. Supportive evidence is shown in Fig. 9, in which significant gate leakage contributed by the electron injection is indeed detected when $V_{G,main}$ is higher than 4 V. A similar observation has also been reported by Uchida et al. [10], who showed that electron injection occurs at the source side if the source is a Schottky junction. This phenomenon is explained with the band diagrams shown in Fig. 10, which is similar to that shown in Fig. 6(c). The diagram corresponds to the on-state operation of the SB MOS devices. Note that most of the voltage drop along the channel occurs at the region near the source side [11], which is very different

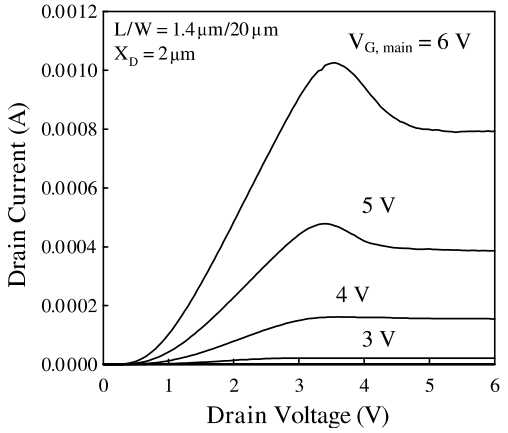

Fig. 7. Drain output characteristics of a SB MOS transistor in n-channel operation. Sub-gate bias is 30 V.

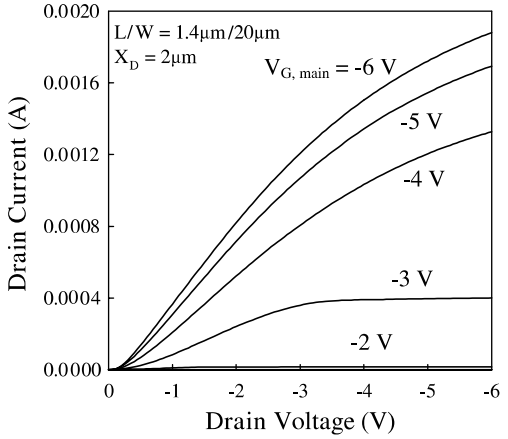

Fig. 8. Drain output characteristics of a SB MOS transistor in p-channel operation. Sub-gate bias is −30 V.

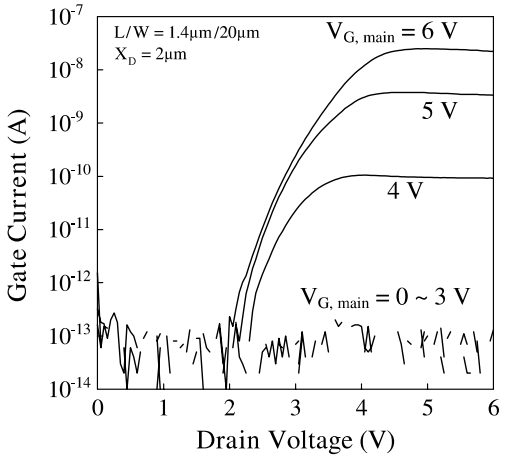

Fig. 9. Gate current as a function of drain and main-gate voltages. Sub-gate bias is 30 V.

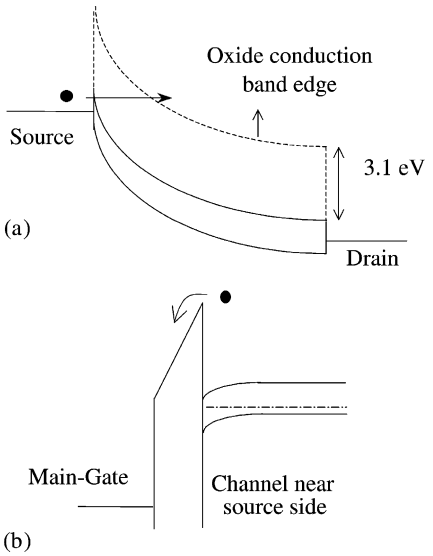

Fig. 10. The band diagrams of (a) source-side hot electron, and (b) hot electron injection into gate.

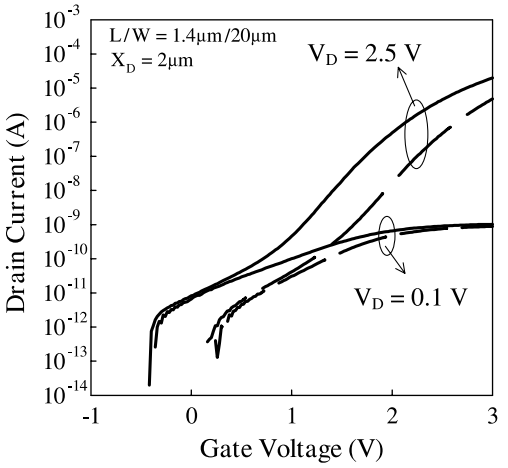

Fig. 11. Sub-threshold characteristics of a SB SOI device before (solid line) and after (dashed line) NDC occurrence.

from conventional MOS transistors. Therefore, the injected electrons from the source may become hot enough to surmount the barrier height of oxide (3.1 eV) if a high drain voltage is applied.

When the main-gate bias is also high, significant electron injection occurs and leads to severe electron trapping, resulting in threshold voltage increase. Since this process proceeds during the device characterization, the drain current is decreased simultaneously, causing the NDC effect. Fig. 11 compares the sub-threshold characteristics of a device before and after the NDC occurrence. Significant shift in *V*th observed after NDC is in agreement with the aforementioned model.

NDC is not observed for p-channel operation, presumably due to the higher barrier height (4.7 eV) and heavier effective mass of holes. The NDC phenomenon may be eliminated if the operation voltage is scaled down, which is in line with the scaling of device dimensions. The electron injection mechanism may, on the other hand, be useful for some floating-gate non-volatile memory applications.

4. Conclusions

In this work, we have fabricated and characterized a new SB SOI MOS transistor device featuring a FID structure. Ambipolar operation with high on/off current ratios of up to 10^7 and 10^8 for n- and p-channel operations, respectively, has been demonstrated. Moreover, the off-state leakage is low and shows very weak dependence on the voltage difference between the drain and the main-gate, in strong contrast to that with conventional structure. These results indicate that the new structure may indeed significantly improve the performance of the SB MOS devices.

We have also found that the NDC phenomenon occurs for n-channel operation if both gate and drain applied voltages are high enough. Such phenomenon may be ascribed to the dynamic electron trapping mechanism induced during the measurements. It may be avoided by lowering the applied voltage, which is in line with future scaled-down device applications. On the other hand, the electron injection mechanism may be useful for some floating-gate non-volatile memory applications.

Acknowledgements

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References

[1] Lepselter MP, Sze M. Proc IEEE 1968;56:1400–1.
[2] Tucker JR, Wang C, Carney PA. Appl Phys Lett 1994; 65:618–20.
[3] Saitoh W, Itoh A, Yamagami S, Asada M. Jpn J Appl Phys 1999;38:6226–31.
[4] Kedzierski J, Xuan P, Bokor J, King T-J, Hu C. Tech Dig IEDM 2000:57–60.
[5] Nishisaka M, Ochiai Y, Asano T. Proc Dev Res Conf (DRC) 1998;98:74–5.
[6] Lin H-C, Lin C-Y, Yeh K-L, Huang R-G, Huang T-Y, Sze M. Tech Dig IEDM 2000:857–9.
[7] Lin H-C, Yeh K-L, Huang R-G, Huang T-Y. IEEE Electron Dev Lett 2001;22:179–81.
[8] Lin H-C, Yeh K-L, Huang R-G, Huang T-Y. Tech Dig AMLCD 2001;1:247–50.
[9] Sze M. Physics of semiconductor devices. 2nd ed.;1982. p. 292.
[10] Uchida T, Matsuzawa K, Koga J, Toriumi A. Appl Phys Lett 2000;76:3992–4.
[11] Winstead B, Bavailio U. IEEE Trans Electron Dev 2000; 47:1241–6.