Figure 3 Measured axial ratio in the broadside direction of the proposed antenna

Figure 5 Measured antenna gain for the proposed antenna

bands I, II, and III, the measured axial ratios are less than 1.2, 1.8, and 2.3 dB, respectively (see Table I). Measured radiation patterns at the center frequencies of bands I, II, and III are also plotted in Figure 4, and good CP radiation has been obtained. Figure 5 shows the measured antenna gain for the proposed antenna. For band I, the measured antenna gain is about 3.2–4.3 dBic. For bands II and III, the measured antenna gain is about 4.0–5.5 dBic and 3.3–4.0 dBic, respectively.

4. CONCLUSION

A low-profile broadband PQHA with good CP radiation characteristics has been proposed and successfully implemented. The proposed antenna shows a very wide CP bandwidth of larger than
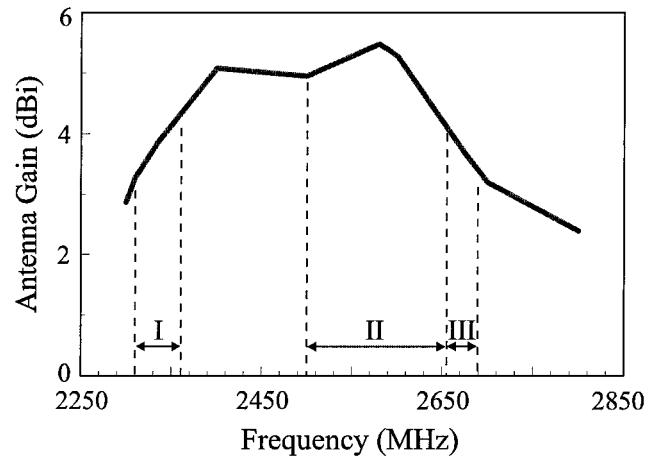
27%, which covers the frequency bands of 2310–2360 MHz, 2500–2655 MHz, and 2655–2690 MHz for broadcasting satellite applications. In addition, the proposed antenna has a low profile of only 27.2 mm, and good antenna gain has also been obtained.

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(a) f = 2335 MHz

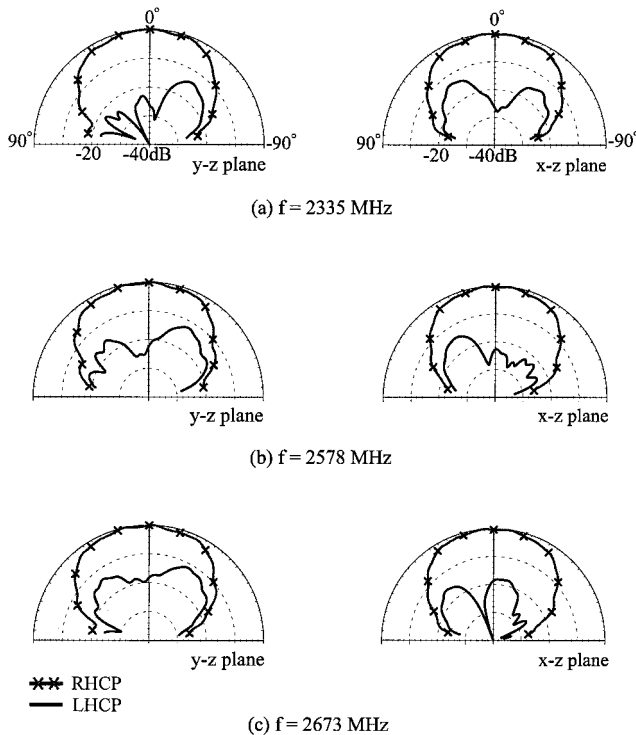(b) f = 2578 MHz

✳✳ RHCP
— LHCP

(c) f = 2673 MHz

Figure 4 Measured radiation patterns at the center frequencies of (a) band I (2310–2360 MHz), (b) band II (2500–2655 MHz), and (c) band III (2655–2690 MHz) for the proposed antenna

A 1.2-V FULLY INTEGRATED 2.4-GHz LOW-NOISE AMPLIFIER IN 0.35-μm CMOS TECHNOLOGY

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ABSTRACT: *A 1.2-V fully integrated 0.35-μm inductively degenerated common source CMOS low-noise amplifier has been demonstrated at 2.4 GHz in this paper. A simple common source configuration can be operated at lower voltage and has lower output impedance when compared with a conventional high output impedance cascode LNA circuit topology. The input matching inductance, output matching inductance, and source degeneration inductance are integrated on a single chip. The fully integrated 2.4-GHz CMOS LNA has 5.27-dB power gain, 17-dB input return loss, 15-dB output return loss, 4-dB noise figure, and -1-dBm IIP_{1dB} and 8-dBm IIP_3 at $V_{dd} = 1.2$ V and $I_{dd} = 10$ mA, respectively. © 2003 Wiley Periodicals, Inc. Microwave Opt Technol Lett 36: 136–139, 2003; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10699*

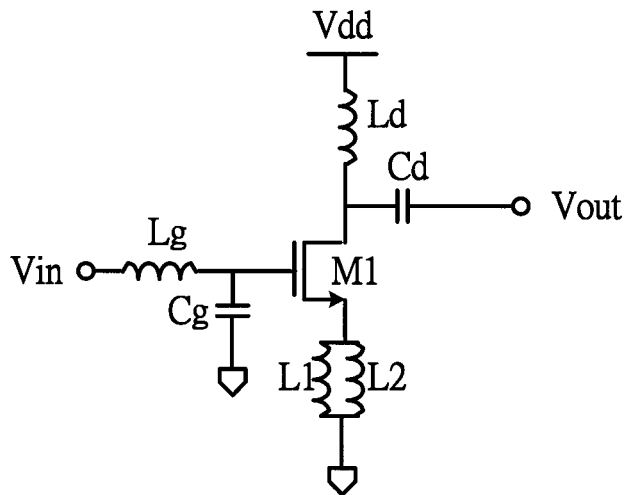**Key words:** *CMOS; LNA; MOSFET amplifier*

Figure 1 Schematic of the inductively degenerated CMOS LNA.

INTRODUCTION

A low-noise amplifier is the key element of an RF receiver. There is a strong effort toward highly integrated, and thus low-cost, radio frequency integrated circuits in wireless communication systems. CMOS apparently has the lowest cost among all the semiconductor technologies for wireless communication. The 0.35-μm CMOS process is fabricated by the inexpensive I-line photolithography techniques instead of expensive deep-UV, and even phase-shift, mask photolithography techniques which are used for gate length 0.25 μm and below. Generally speaking, inductors, resistors, and capacitors limit the size of an RFIC, and thus smaller-gate-length CMOS technology does not improve RFIC chip size. Recently, a highly integrated CMOS transceiver for Bluetooth applications has been implemented in a digital 0.35-mm CMOS process [1]. However, most of the CMOS LNAs implemented still use off-chip matching elements to reduce chip size and provide tuning flexibility [1–3]. There are some works on fully integrated CMOS cascode LNAs [4–7]. A cascode CMOS LNA has better isolation and is the most popular LNA topology. On the other hand, a simple inductively degenerated common source LNA can operate at lower voltage and could have smaller on-chip inductances. The larger input capacitance caused by the Miller effect and the lower output impedance of a simple inductively degenerated common-source LNA require smaller input gate resonant inductance and smaller drain inductance for impedance transformation to 50Ω. In this paper, a 1.2-V fully integrated inductively degenerated common-source CMOS LNA is demonstrated at 2.4 GHz by using 0.35-μm digital CMOS technology. The experimental results show that the CMOS LNA has 5.27 dB gain and 4 dB noise figure at $V_{dd} = 1.2$ V and $I_{dd} = 10$ mA. On the other hand, the CMOS LNA has 6.12-dB gain and 4-dB noise figure at $V_{dd} = 3.3$ V and $I_{dd} = 10$ mA.

CIRCUIT DESIGN

A simple common-source CMOS LNA schematic is illustrated in Figure 1. L_g and L_d are the input matching inductance and the output matching inductance, respectively, while the two parallel L_1 and L_2 shown in Figure 1 are the source degenerated inductances. L-type matching networks are used at both input and output. The design approach for this CMOS LNA is a measurement-based
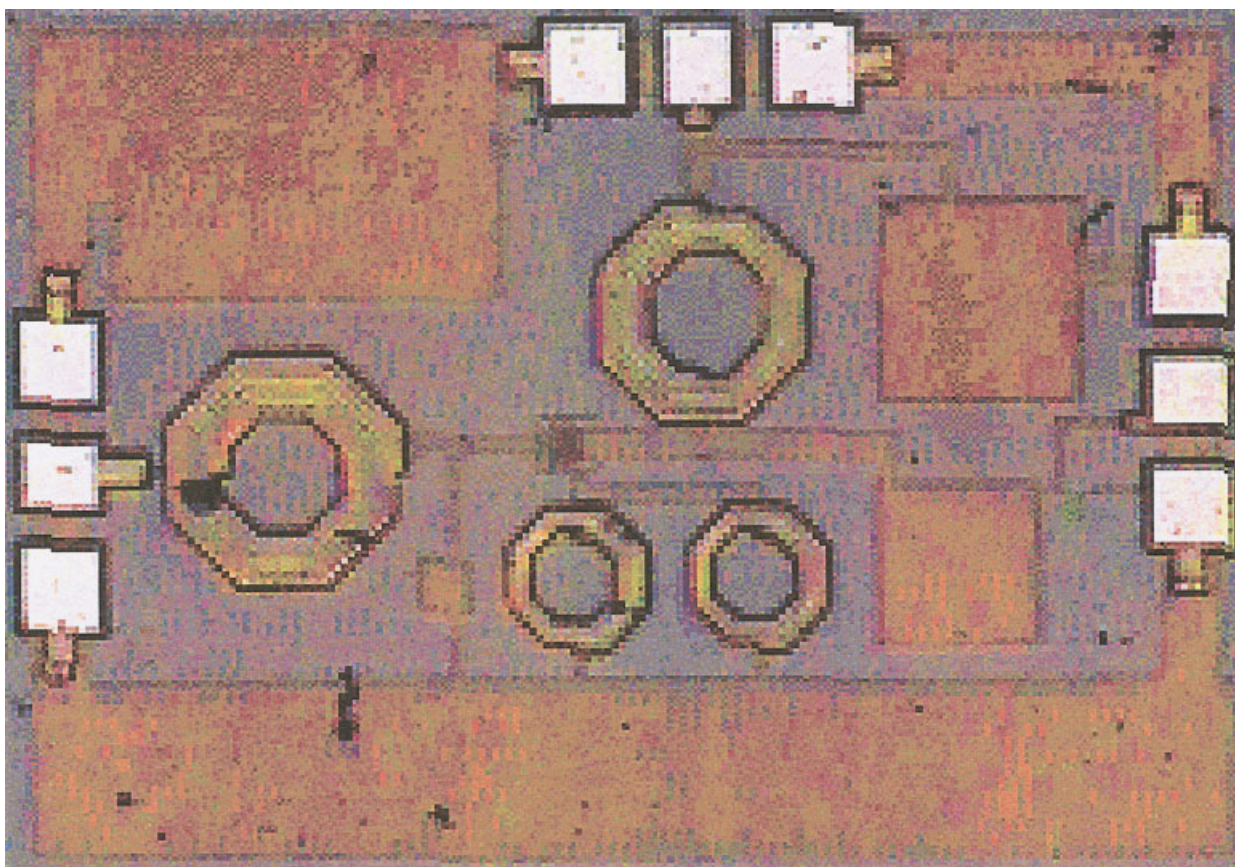

Figure 2 Photo of the fabricated CMOS LNA. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com.]
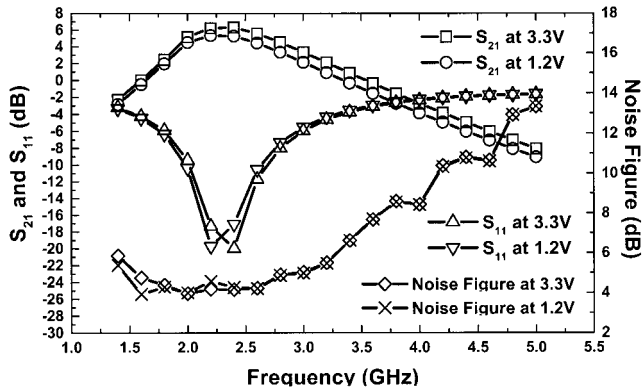
Figure 3 Measured S_{21}, S_{11} and noise figure of the 0.35 μm CMOS LNA at both 1.2 V and 3.3 V supply voltage when $I_{dd} = 10$ mA.

Figure 5 Measured IP_{1dB} and IIP_3 of the 0.35 μm CMOS LNA at both 1.2 V and 3.3 V supply voltage when $I_{dd} = 10$ mA.

design, which is very accurate but requires a test run to generate a circuit-element database. High frequency measurements were performed on different device sizes and various inductors after the test run was made. The low-noise amplifier is then simulated by the measured S-parameters. The inductors used in the CMOS LNA design are 5 turns (260 μm $\times$ 280 μm) for L_g, 4 turns (235 μm $\times$ 250 μm) for L_d, and 2 turns (150 μm $\times$ 175 μm) for L_1 and L_2, respectively. A multi-finger CMOS device is used to reduce the gate resistance for better power gain and noise figure. The CMOS device has 0.35-μm gate length and eight fingers with 25-μm-unit gate width. The photo of the fabricated CMOS LNA is shown in Figure 2. The low noise amplifier is implemented with a 0.35-μm digital CMOS technology.

EXPERIMENTAL RESULTS

The measurement-based design approach is indeed a useful RFIC design method. Simulation results and measured results of the CMOS LNA agree very well. Because the CMOS LNA can be operated at 1.2 V supply voltage and thus rf performance are measured at both 1.2 V and 3.3 V supply voltages when $I_{dd} = 10$ mA. The measured small signal rf results are illustrated in Figures 3 and 4. Figure 3 illustrates S_{21} (forward transmission), S_{11} (input return loss), and noise figure; while Figure 4 illustrates S_{22} (output return loss) and S_{12} (reversed transmission). S_{21} is 6.31 dB, S_{11} is -20 dB, S_{12} is -29 dB, S_{22} is -17 dB and NF = 4 dB at 2.4 GHz when $V_{dd} = 3.3$ V. The noise figure shown here indicates that the noise figure is at its best around 2.4 GHz. Large signal gain
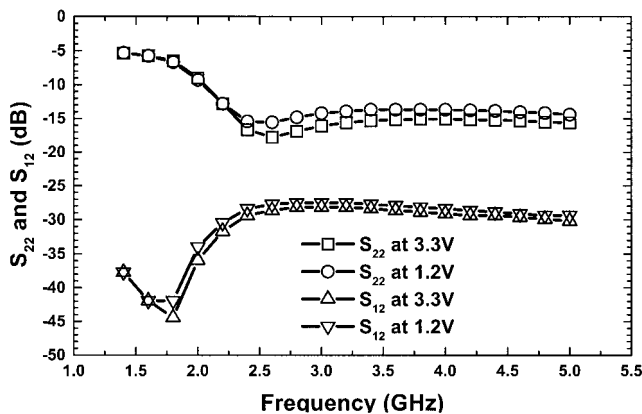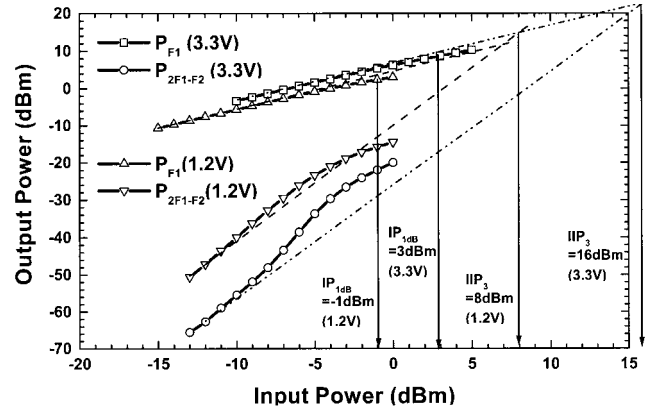
compression and two tone intermodulation were also measured and shown in Figure 5. As shown in Figure 5, IP_{1dB} is 3 dBm and IIP_3 is 16 dBm at 3.3 V. When the CMOS LNA is operated at 1.2 V, S_{21} is 5.27 dB, S_{11} is -17 dB, S_{12} is -28 dB, S_{22} is -15 dB, and NF = 4 dB at 2.4 GHz. IP_{1dB} is -1 dBm and IIP_3 is 8 dBm at 1.2 supply voltage.

DISCUSSION AND CONCLUSION

A low-voltage (1.2 V) truly fully integrated CMOS LNA was demonstrated in a simple common source configuration. Power gain can be increased by cascading two identical common-source CMOS LNAs. The noise figure of a cascaded amplifier is calculated by the well-known equation $NF = NF_1 + (NF_2 - 1)/G_1$. If the LNA in this letter is in cascade, the total noise figure is 4.71 (or 4.57) dB and gain is 10.54 (or 12.62) dB at $V_{dd} = 1.2$ (or 3.3) V and $I_{dd} = 20$ mA. A cascading common source LNA can be a fair comparison to a cascode LNA, because a cascode LNA is a two-stage amplifier (CS-CG configuration). The noise figure of the LNA is not very good and is probably due to the inadequate gate finger number and unit gate width. Power gain can possibly be improved by using smaller a unit-gate width and more gate fingers [7]. In conclusion, a fully integrated 2.4-GHz CMOS LNA with 5.27-dB power gain, 17-dB input return loss, 15-dB output return loss, 4-dB noise figure, and -1-dBm IIP_{1dB} and 8-dBm IIP_3 is demonstrated at $V_{dd} = 1.2$ V and $I_{dd} = 10$ mA.

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Figure 4 Measured S_{22} and S_{12} of the 0.35 μm CMOS LNA at both 1.2 V and 3.3 V supply voltage when $I_{dd} = 10$ mA.

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ANALYSIS OF CONFORMAL ANTENNAS ON A COMPLEX PLATFORM

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ABSTRACT: *A numerical technique is presented for characterizing the radiation patterns and mutual coupling of conformal antennas mounted on a complex platform. This technique uses the higher-order finite element method (FEM) to model the antennas and the platform and employs the boundary integral equation to terminate the FEM computational domain. The resulting numerical system is solved using a novel preconditioner in conjunction with the multilevel fast multipole algorithm for the fast evaluation of boundary integrals.* © 2003 Wiley Periodicals, Inc. Microwave Opt Technol Lett 36: 139–142, 2003; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10700

1. INTRODUCTION

Modern aircraft are usually equipped with many antennas for a variety of communication, detection, tracking, and surveillance purposes. To reduce the radar signature and adverse effects on the aerodynamic design, antennas are often conformal to the surface of the vehicle and sometimes embedded in a layered dielectric medium. Placing these antennas on aircraft inevitably introduces distortion in their radiation patterns and causes mutual coupling. The distortion in the radiation patterns may reduce the desired coverage for effective communications and compromise accuracy of isolating and locating targets. The
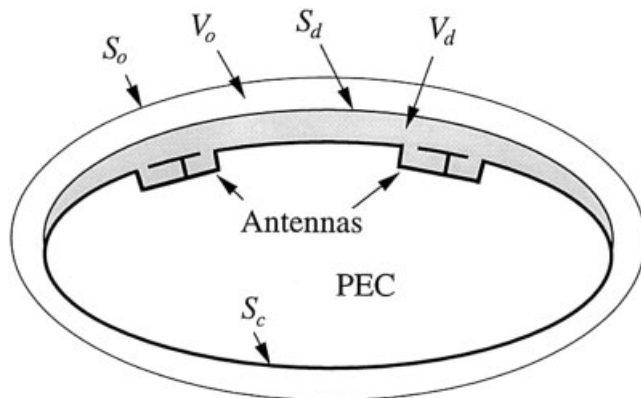

Figure 1 Conformal antennas embedded in a dielectric medium situated on a large platform
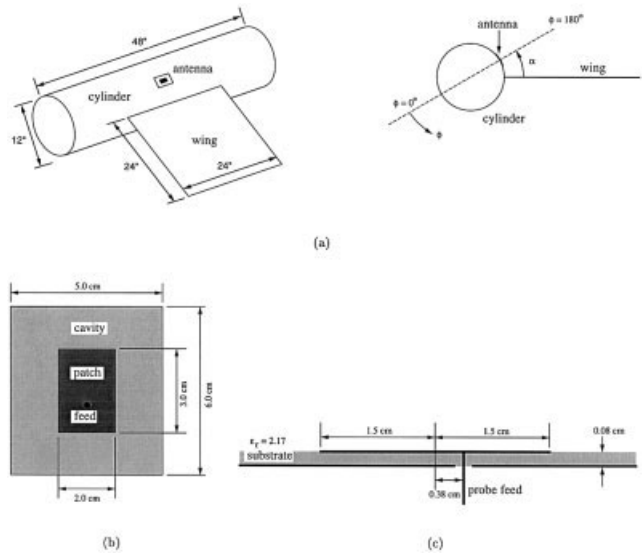

Figure 2 (a) Patch antenna mounted on a cylinder with a wing; (b) top view of the patch antenna; (c) longitudinal section view of the patch antenna

existence of mutual coupling, caused by space waves, surface waves, and scattering by the platform, reduces the electromagnetic isolation between the antennas and consequently makes it difficult to operate the antennas simultaneously. Therefore, it is important to develop accurate numerical prediction tools to characterize the radiation patterns and mutual coupling of the antennas mounted on a complex, often large, platform.

Because of the high complexity of the problem, limited work has been carried out in the past. In [1], a technique is presented for calculating the radiation pattern of a microstrip patch antenna on a cylindrical body using a three-dimensional (3D) finite element method (FEM) to analyze the patch antenna and a two-dimensional (2D) method of moments (MoM) to characterize the effect of the cylindrical body. Its application is limited to predicting the radiation patterns of patch antennas on 2D bodies. In [2] and [3], the FEM is combined with a high-frequency asymptotic method to predict the radiation patterns of conformal antennas on a 3D platform. Again, the FEM is used to analyze the antennas and the asymptotic method is employed to characterize the effect of the platform on the radiation patterns. Since the asymptotic methods are not capable of modeling surface waves and near-field scattering accurately, this hybrid method cannot accurately simulate the mutual coupling of the antennas. To accurately predict the radiation patterns and simulate the mutual coupling of the antennas on a platform, it is necessary to use a first principle method, such as the FEM and MoM or their hybridization, to carry out the analysis. Such an analysis is, however, very difficult because of the complexity of the structures and the large size of the platform.

In this paper, we present a novel hybrid technique, which is our first attempt to deal with this complex problem. This technique is based on a recently developed finite element–boundary integral (FE–BI) method [4]. It employs higher-order vector elements to accurately model complex geometries and reduce the number of unknowns for large-size problems and incorporates a highly effective preconditioner [5] to accelerate the convergence of the iteration solution of the FE–BI system and the multilevel fast multipole algorithm (MLFMA) [6] to speed up the evaluation of boundary integrals.