Device Modeling of Ferroelectric Memory Field-Effect Transistor for the Application of Ferroelectric Random Access Memory

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***Abstract*—An improved theoretical analysis on the electrical characteristics of ferroelectric memory field-effect transistor (FeMFET) is given. First, we propose a new analytical expression for the polarization versus electric field (*P*-*E*) for the ferroelectric material. It is determined by one parameter and explicitly includes both the saturated and nonsaturated hysteresis loops. Using this expression, we then examine the operational properties for two practical devices such as the metal-ferroelectric-insulator-semiconductor field-effect transistor (MFIS-FET) and metal-ferroelectric-metal-insulator-semiconductor field-effect transistor (MFMIS-FET) as well. A double integral also has been used, in order to include the possible effects due to the nonuniform field and charge distribution along the channel of the device, to calculate the drain current of FeMFET. By using the relevant material parameters close to the (Bi, La)$_4$Ti$_3$O$_{12}$ (BLT) system, accurate analyses on the capacitors and FeMFET's at various applied biases are made. We also address the issues of depolarization field and retention time about such a device.**

I. Introduction

With some decisive and superior features such as nonvolatile, low power consumption, short programming time, and high endurance of over 10^{12} read/write cycles, the ferroelectric random access memory (FeRAM) has become a potential high performance nonvolatile memory [1]. Essentially two types of FeRAM have been evaluated based on the practical use. One type is made of transistors connected with capacitors, such as 1T1C [1] or chain FeRAM [2] structures. The other is a field-effect transistor and is referred to as the ferroelectric memory field-effect transistor (FeMFET) [3]. The FeMFET has special potential for technical use as a nondestructive read out (NDRO) and high-density nonvolatile memory [3]–[9]. The structure of FeMFET is similar to the common metal-oxide-semiconductor field-effect transistor (MOSFET); only the gate material is a ferroelectric rather than the usual oxide. With writing at a gate voltage, $+V_w$ or $-V_w$, the dipole moments are stored, and the direction of polarization is set in the ferroelectric material. This results in the threshold voltage difference of the two states of the FeMFET and can be identified as two logic states in a memory. However, the direct deposition of the ferroelectric material on a silicon (Si) substrate may cause serious interdiffusion near the interface, which in turn will degrade the device performance. Thus, an insulating buffer layer must be inserted between the Si and ferroelectric layer in order to give better interfacial properties. Such device structure is referred to as the metal-ferroelectric-insulator-semiconductor field-effect transistor (MFIS-FET) [3]–[9]. The MFIS-FET, however, has a small memory window under the low operation voltages. In order to overcome this problem, metal-ferroelectric-metal-insulator-semiconductor field-effect transistor (MFMIS-FET) with a floating metal gate sandwiched by the ferroelectric and insulating buffer layer has been reported [4], [5]. The main merit of this device is that the area of a metal-ferroelectric-metal (MFM) capacitor can be changed to be smaller than that of metal-insulator-semiconductor (MIS). This would make the capacitance of MIS comparable to that of MFM, such that the voltage drop across the ferroelectric layer can be strongly enhanced. As a result, the applied voltage becomes more efficient in driving the ferroelectric layer into the state of saturated polarization. Therefore, the operation voltage for an MFMIS-FET can be much lower than MFIS-FET.

So far, the reported retention times of various FeMFET and the associated capacitors are usually shorter than 10^5 seconds, which are still much lower than the industrial standard for the nonvolatile memory in which 10 years is required. The reason for the small retention time of FeMFET is due to the depolarization fields that cause charge injection and reduction of the remanent polarization. These effects lead to threshold voltage shifts that could reduce the memory window. Although the problem of short data retention time is not overcome until now, recently Kim *et al.* [10] and Ma and Han [11] proposed that the FeMFET can be used as a dynamic random access memory (DRAM) if the FeMFET can be refreshed. This new kind of device, called FeDRAM, triggers a new application of FeMFET.

In order to optimize the design and fabrication parameters of FeMFET, a theoretical understanding of the depen-

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dence of the electrical properties on material parameters thus is needed. However, there are only a few theoretical reports of such device thus far in spite of its great importance. The first complete theoretical study on the operational properties for an FeMFET was made by Miller and McWhorter [3]. Their treatment is based on the Brews' charge sheet model [12], [13] together with a mathematical model [14], [15] of describing the switching polarization of ferroelectric capacitor. The validity of their model, however, is rather limited because Brew's charge sheet model is not suitable for the device operated in the subthreshold and saturation region (after pinch-off). In addition, they have assumed, in order to simplify the formulation, the polarization interior the ferroelectric along the channel position to be constant, which is the case of very low drain voltage. Miller and McWhorter's model [3] recently was modified by Kamei *et al.* [16], who have treated the polarization of the ferroelectric material in an MFSFET to be inhomogeneous along the channel. However, the method still cannot be applied to the saturation and subthreshold region due to the limitation of charge sheet model. In addition, they have assumed the polarization of the ferroelectric material is saturated hysteresis, which is not suitable for MFIS and MFMIS-FET. The purpose of this paper is to give an improved analysis of the electric characteristics for the FeMFETs. The analysis is made based on a new analytical expression for nonsaturated polarization of the ferroelectric material together with inclusion of nonuniform field distributions along the channel position. Pao and Sah's double integral [12], [13] is first used to investigate the effect of this inhomogeneous field in the FeMFET's. Systematic numerical results will be presented for two practical devices, MFIS-FET and MFMIS-FET (along with the associated capacitors). The results allow one to gain some physical insight into the operation of FeMFETs that are of practical use in the device design.

The material and device parameters used for the analyses in this paper are listed in Table I, unless otherwise specified. The parameters of the ferroelectric and insulator are chosen to be close to the reported data [17] of (Bi, La)$_4$Ti$_3$O$_{12}$ (BLT) MFMIS capacitors. The BLT has nearly fatigue-free properties [18] and moderate saturated polarization in addition to a high coercive field ($E_c = 100$ kV/cm). Although the FeMFET is commonly fabricated as n-channel devices, we analyze the p-channel devices with n-type substrate (or n-well) for consistency with the experimental condition [17].

II. Theory

A. Phenomenological Model of Dipole Polarization

Let us first develop a new analytical expression for the dipole polarization for the ferroelectric layer used in the gate of FeMFET. This will be done on the basis of mathematical model reported by Miller *et al.* [14]. In this model, the saturated P-E hysteresis loop for a ferroelectric is described as:

$$P_{sat}^{+}(E) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right), \tag{1}$$

$$P_{sat}^{-}(E) = -P_{sat}^{+}(-E) \tag{2}$$

where

$$\delta \equiv E_c\left(\ln\left(\frac{1 + P_r/P_s}{1 - P_r/P_s}\right)\right)^{-1}. \tag{3}$$

Here $P^{+}(E)$ stands for the lower (positive-going) branch, and $P^{-}(E)$ is the upper (negative-going) branch. P_s is the spontaneous polarization, P_r is the remanent polarization, and E_c is the coercive field. To fit well with experimental data, (1) should be modified as [20]:

$$P_{sat}^{+}(E) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) + \varepsilon_F\varepsilon_0 E, \tag{4}$$

where ε_F is the dielectric constant of the ferroelectric material and ε_0 is the free space permittivity. The negative-going branch still follows (2).

As mentioned previously, the above equations are suitable only for the saturated hysteresis loop. With these in hand, we can develop a new expression for the unsaturated hysteresis loop in a simple way. We assume that the unsaturated hysteresis loop can be uniquely determined by a parameter, E_m, which is defined as the maximum electric field that the ferroelectric layer may undergo. The unsaturated hysteresis loop is composed of two branches, $P^{+}(E, E_m)$ and $P^{-}(E, E_m)$, where $P^{+}(E, E_m)$ is, as usual, the positive-going branch and $P^{-}(E, E_m)$ is the negative-going one. These two branches must intersect at $E = E_m$:

$$P^{+}(E = E_m, E_m) = P^{-}(E = E_m, E_m). \tag{5}$$

By making use of the fact stated in [14], "existing data indicate that the derivative of the polarization with respect to the electric field, evaluated at a constant field, is independent of the amplitude of the applied signal, at least to first order," we have:

$$\left.\frac{dP^{+}(E, E_m)}{dE}\right|_E = \left.\frac{dP_{sat}^{+}(E)}{dE}\right|_E, \tag{6}$$

and

$$\left.\frac{dP^{-}(E, E_m)}{dE}\right|_E = \left.\frac{dP_{sat}^{-}(E)}{dE}\right|_E. \tag{7}$$

It is then easy to get two branches of the unsaturated hysteresis loop, namely:

$$P^{+}(E, E_m) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) + \varepsilon_F\varepsilon_0 E + \frac{1}{2}\left(P_s \tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s \tanh\left(\frac{E_m - E_c}{2\delta}\right)\right), \tag{8}$$

TABLE I
DEVICE PARAMETERS FOR THE SIMULATION IN FEMFET IN THE TEXT.

Parameters	Definitions	Values used in calculation
P_r	Remanent polarization	15 μC/cm^2
P_s	Spontaneous polarization	17 μC/cm^2
E_c	Coercive field	100 KV/cm
ε_F	Dielectric constant of ferroelectric	200
ε_I	Dielectric constant of insulator	3.9
t_F	Thickness of ferroelectric film	150 nm
t_I	Thickness of insulator film	2 nm
A_F	Area of ferroelectric film	1 cm^2 (For MFIS capacitor)
A_I	Area of the insulator film	1 cm^2
μ	Electron mobility	500 cm^2/s-Volt
N_a	Substrate doping concentration (p-type)	10^{16} cm^{-3}
L	Channel length	1 μm (for FEMFET)
W	Channel width	1 μm (for FEMFET)

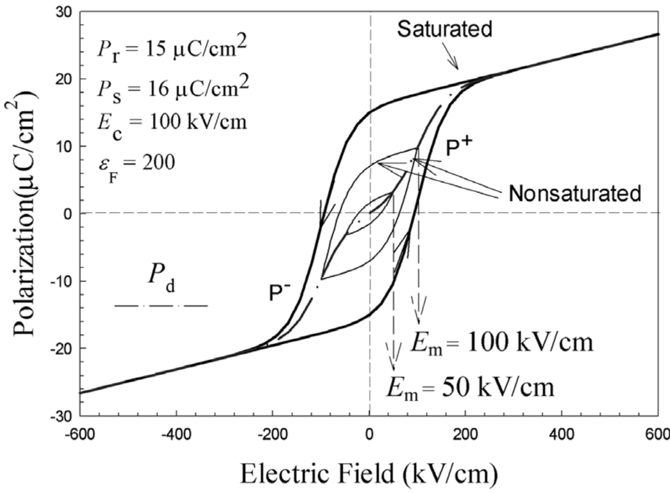

Fig. 1. The modeled polarization, based on (8)–(10) as a function of the electric field (P-E) for the ferroelectric material at different maximum electric field. The model parameters used are $P_r = 15\ \mu$C/cm^2, $P_s = 16\ \mu$C/cm^2, $E_C = 100$ kV/cm, and $\varepsilon_F = 200$.

and

$$P^{=}(E, E_m) = P_s \tanh\left(\frac{E + E_c}{2\delta}\right) + \varepsilon_F \varepsilon_0 E - \frac{1}{2}\left(P_s \tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s \tanh\left(\frac{E_m - E_c}{2\delta}\right)\right). \quad (9)$$

The dependence of the dipole polarization on the maximum electric field is given by:

$$P_d(E_m) = \varepsilon_F \varepsilon_0 E_m + \frac{1}{2}\left(P_s \tanh\left(\frac{E_m + E_c}{2\delta}\right) + P_s \tanh\left(\frac{E_m - E_c}{2\delta}\right)\right). \quad (10)$$

Two calculated nonsaturated loops of P-E based on (8)–(10) are displayed in Fig. 1. The unpolarized ferroelectric material is first at the origin ($P = 0$, $E = 0$). By increasing the applied field, the polarization will follow the curve of $P_d(E_m)$ until the maximum field E_m is attained. The polarization will follow branch $P^+(E, E_m)$ and then $P^-(E, E_m)$. Therefore, the overall hysteresis loop is constructed in the counterclockwise direction. Eq. (8)–(10) will be used later to investigate the electric characteristics of the FeMFETs.

B. Capacitor Equations

In this paper, we consider two important structures of FeMFET, the MFIS-FET and MFMIS-FET shown, respectively, in Fig. 2(a) and (b), in which the sign conventions also are given.

1. MFIS Capacitance-Voltage Relation: For an MFIS capacitor shown in Fig. 2(a), the boundary condition gives:

$$D = \varepsilon_0 E_F + P(E_F) = \varepsilon_I \varepsilon_0 E_I = \varepsilon_{Si} \varepsilon_0 E_{Si}, \quad (11)$$

where E_F, E_I, and E_{Si} stand for the electric fields in the ferroelectric, insulator, and near the interface of semiconductor (Si), respectively. And ε_I and ε_{si} are the dielectric constants of insulator and semiconductor, respectively. The term $\varepsilon_0 E_F$ can be neglected because it is much less than $P(E_F)$. And Gauss's law gives $\varepsilon_{Si}\varepsilon_0 E_{Si} = -Q_s(\psi_s)$, where $Q_s(\psi_s)$ is the space charge (per unit area) in the semiconductor and ψ_s denotes the surface potential. Eq. (11) is rewritten as:

$$-Q_s(\psi_s) = P\left(\frac{V_F}{t_F}\right) = \frac{\varepsilon_I \varepsilon_0}{t_I} V_I, \quad (12)$$

where the voltage drops in the ferroelectric layer and the insulator is $V_F = E_F t_F$ and $V_I = E_I t_I$, respectively. The semiconductor charge density $Q_s(\psi_s)$ for n-type substrate is given by [12]:

$$Q_s(\psi_s) = \mathrm{m}\frac{\sqrt{2}\varepsilon_{Si}\varepsilon_0}{\beta L_D} \left(\frac{n_i^2}{N_D^2}\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right) + \left(e^{\beta\psi_s} - \beta\psi_s - 1\right)\right)^{1/2}, \quad (13)$$

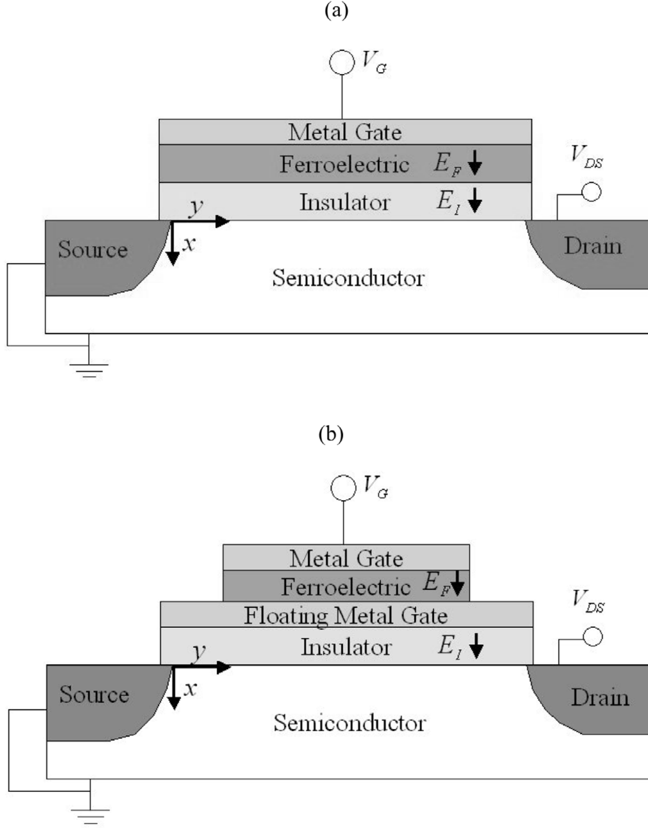

Fig. 2. Diagram of two typical FeMFETs. (a) The MFIS-FET, and (b) MFMIS-FET. The coordinate and sign convention are shown here.

where the leading minus (−) sign is for $\psi_s > 0$ (accumulation), the plus sign (+) is for $\psi_s < 0$ (inversion), and the Debye length is $L_D = \sqrt{\varepsilon_{Si}\varepsilon_0/qN_D\beta}$, where N_D is the majority carrier concentration (for an n-type semiconductor here), n is the intrinsic carrier concentration equal to 9.65×10^9, and $\beta \equiv q/kT$, where k is the Boltzmann constant and q the electronic charge.

The total gate voltage is:

$$V_G = \psi_s + V_I + V_F. \tag{14}$$

Assuming that the unpolarized ferroelectric film is first at the origin ($E = 0$, $P = 0$), the polarization then traces $P_d(E_m)$. Given the maximum writing gate voltage, $+V_W$ or $-V_W$, (12) and (14) can be used to numerically determine the surface potential ψ_s and the maximum electric field E_m in the ferroelectric layer. Therefore, two branches, $P^+(E, E_m)$ and $P^+(E, E_m)$, in (8) and (9) are readily determined. Then by repeatedly solving (12) and (14) by varying the gate voltage, from $+V_W$ to $-V_W$ with $P^-(E, E_m)$ and $-V_W$ to $+V_W$ with $P^+(E, E_m)$, one is able to obtain ψ_s, V_I, and V_F as a function of gate voltage in a closed loop. The reason for the direction will be discussed in Section III.

The total capacitance in this stacked structure is:

$$C_{total} = \left(\frac{1}{C_I} + \frac{1}{C_F} + \frac{1}{C_D}\right)^{-1}, \tag{15}$$

where

$$C_I = \frac{\varepsilon_0\varepsilon_I A_I}{t_I}, \tag{16}$$

$$C_F = \frac{\varepsilon_0\varepsilon_F A_F}{t_F}, \tag{17}$$

and the capacitance of semiconductor depletion layer is given by [12]:

$$C_D = \frac{A_I\varepsilon_{Si}\varepsilon_0}{\sqrt{2}L_D} \frac{\left(\frac{n_i^2}{N_D^2}\left(-e^{-\beta\,\psi_s} + 1\right) + \left(e^{\beta\,\psi_s} - 1\right)\right)}{\left(\frac{n_i^2}{N_D^2}\left(e^{-\beta\,\psi_s} + \beta\,\psi_s - 1\right) + \left(e^{\beta\,\psi_s} - \beta\,\psi_s - 1\right)\right)^{1/2}}. \tag{18}$$

With the aid of the calculated surface potential as a function of gate voltage together with (15)–(18), we can finally establish the relationship of capacitance versus gate voltage. Black and Welser [19] have pointed out that there can be voltage drops across the metal electrodes due to the finite Thomas-Fermi screening length in the metal. This phenomenon can be effectively treated by adding more insulators in the MFIS or MFMIS structures. The present simulation method also can model this effect by simply increasing the equivalent oxide thickness (EOT) of the insulator slightly, which can be estimated to be around 1 to 2 Å based on [19].

2. MFMIS Capacitance-Voltage Relation: For an MFMIS capacitor shown in Fig. 2(b), the area of ferroelectric is obviously not the same as the insulator. In this case, the only distinction lies in (12), which now should be read as:

$$A_F P\left(\frac{V_F}{t_F}\right) = A_I\frac{\varepsilon_I\varepsilon_0}{t_I}V_I, \tag{19}$$

according to the charge conservation. Other equations remain the same as MFIS capacitor. Thus, the capacitance-voltage (CV) curve can be determined by the same procedures as in an MFIS capacitor.

It should be noted that (18) is a low-frequency result. The high-frequency capacitance, however, does not follow it at strong inversion. At high frequency, the generation rate of the charge carriers from the depletion region cannot follow the rapid change of the applied signal, and the capacitance remains at the minimum value, C_{min}. Because the ordinary CV is measured at high frequency, we therefore constraint the capacitance to C_{min} at the strong inversion condition.

C. FeMFET Drain Current Equations

The drawback of Miller and McWhorter's model [3] was mentioned earlier. Therefore, we resort to another approach to calculate the drain current of the FeMFET. An improved and elegant method of calculating the drain cur-

rent for MOSFET is available, namely Pao and Sah's double integral [13]:

$$I_D = q\mu \frac{W}{L} \int_0^{V_{DS}} \int_{\psi_B}^{\psi_s} \frac{\left(n_i^2/N_D\right) e^{-\beta(\psi - V)}}{\xi(\psi, V)} d\psi\, dV, \tag{20}$$

where $\psi_B = -(kT/q)\ln(N_D/n_i)$. Here $\xi(\psi, V)$ is the electric field given by:

$$\xi(\psi, V) = \sqrt{\frac{2N_D kT}{\varepsilon_{Si}\varepsilon_0}} \left[\left(e^{\beta\psi} - \beta\psi - 1\right) + \frac{n_i^2}{N_D^2} e^{\beta V}\left(e^{-\beta\psi} + \beta\psi e^{-\beta V} - 1\right)\right]^{1/2}. \tag{21}$$

This current equation includes the drift as well as the diffusion currents, and it is suitable for the simulation of an FeMFET operated in subthreshold, triode, and saturation regions.

1. MFIS-FET Current: For an MFIS-FET, the gate voltage is:

$$V_G = \psi_s + \frac{Q_s(\psi_s, V)}{\varepsilon_I/t_I} + E_F t_F, \tag{22}$$

where

$$Q_s(\psi_s, V) = P(E_F, E_m). \tag{23}$$

Here the dependence of surface charge density on the surface potential ψ_s and channel potential V is given by [12]:

$$Q_S(\psi_S, V) = \mathrm{m}\frac{\sqrt{2}\varepsilon_{Si}\varepsilon_0 kT}{qL_D} \left(\left(e^{\beta\,\psi_s} - \beta\,\psi_s - 1\right) + \frac{n_i^2}{N_D^2} e^{\beta\,V} \left(e^{-\beta\,\psi_s} + \beta\,\psi_s e^{-\beta\,V} - 1\right)\right)^{1/2}, \tag{24}$$

and $P(E_F, E_m) = P^+(E_F, E_m)$ or $P^-(E_F, E_m)$ for $-V_W \to +V_W$ or $+V_W \to -V_W$, respectively. E_m is the same as obtained by the MFIS capacitor. Eq. (22) and (23) then can be used to numerically solve for ψ_s and E_F for a given channel potential V. The surface potentials are controlled by the polarization of ferroelectric material according to (22) and (23). Consequently, the drain current will in turn change as a function of polarization from (20). The current-voltage relationship can then be determined at any desired drain voltage V_{DS} and gate voltage V_G. Note that the gate voltage V_G should be negatively large enough to ensure $\psi_s < \psi_B$ (inversion). The case of $\psi_s > \psi_B$ (accumulation) where the FeMFET operating in the cut-off region is of no interest to us here.

Then, (20) can be rewritten, with change of variable, as [13]:

$$I_D \frac{y}{L} = \frac{1}{L}\int_0^y I_D\, dy = q\mu \frac{W}{L}\int_0^{V(y)} \int_{\psi_B}^{\psi_S} \frac{\left(n_i^2/N_D\right) e^{-\beta(\psi - V)}}{\xi(\psi, V)} d\psi\, dV. \tag{25}$$

where the drain voltage now runs to $V(y)$ rather than to V_{DS}. Given V_G and V_{DS}, (20) gives the drain current I_D, which then is used in (25). This integral equation enables one to numerically determine the channel potential, $V(y)$. However, there is a simpler way to directly obtain $V(y)$ from $I_D - V_{DS}$ plot. As seen from (25), channel position y can be solved easily for a given channel potential because the right side is simply the drain current for a value of drain voltage $V(y)$. Therefore, if we can first determine the $I_D - V_{DS}$ by changing the drain voltage V from 0 to V_{DS}, the ratio $I_D(V)/I_D(V_{DS})$ can be converted simply to y/L, and V just corresponds to $V(y)$ for this bias condition. With $V(y)$ in hand, ψ_s, V_I, and V_F as functions of channel position are readily obtainable based on (22), (23), and (24).

2. MFMIS-FET Current: The above-mentioned calculation procedures for MFIS-FET generally are valid for MFMIS-FET only with some different ones. In this case, the floating metal gate would cause ferroelectric voltage, V_F, to be uniform in the lateral direction. The structure of MFMIS-FET is depicted in Fig. 2(b), in which itself can be effectively regarded as an MOSFET in series with an MFM capacitor. Thus, by individually investigating the behaviors for two devices, the characteristics of an MFMIS-FET can be obtained. At a low drain voltage, the charges stored in the MOSFET are closely equal to the MOS capacitor. Eq. (12) and (19) determine the gate voltage of MOSFET, and the drain current also could be found from (20).

III. Discussion of the Simulation Results

The behaviors of the FeMFETs and the associated capacitors are now investigated using the equations derived in the preceding section. The material parameters used for the analyses in all the figures are listed in Table I, unless otherwise specified. Fig. 1 shows the calculated P-E results, in which it is seen that a larger value of E_m gives rise to a larger unsaturated hysteresis loop. The central dot-dashed line denotes, $P_d(E_m)$ described in (10).

A. Capacitors

The simulation result of the CV relation for an MFMIS capacitor with various area ratios of A_f/A_I = 1/6, 1/9, 1/12, and 1/15 at the writing voltages of ±5 V is plotted in Fig. 3. The simulation results of the CV curves are close to the experimental results reported by Tokumitsu *et al.* [17]. In their work, the observed CV curves are slightly shifted in the cases of small area ratios; they explained that this phenomenon was due to the fixed charge occasionally introduced in the sample. Our simulation results also show a similar behavior for the sample with small area ratios. However, our simulation does not incorporate the effect of fixed charge. We provide the possible explanation as the following instead of the fixed charge introduced. Because the accumulation capacitances with small area ratios are reduced, the flat band capacitances, consequently,

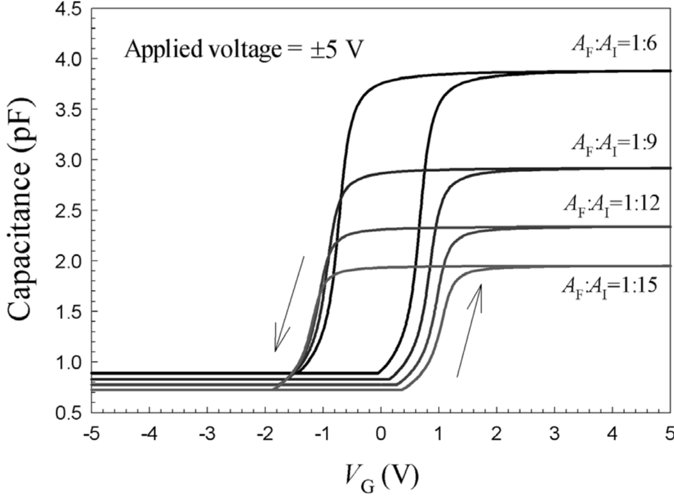

Fig. 3. Calculated capacitance versus gate voltage (CV) for the MFIS capacitors at various area ratios. The device parameters used are given in Table I.

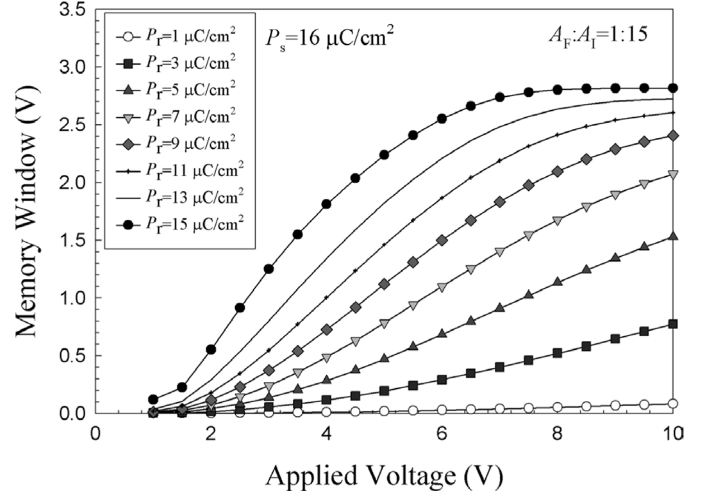

Fig. 5. Calculated memory window as a function of applied bias at different values of P_r with a fixed value of P_s for the MFMIS capacitor. Large P_r/P_s is required to obtain large memory window.

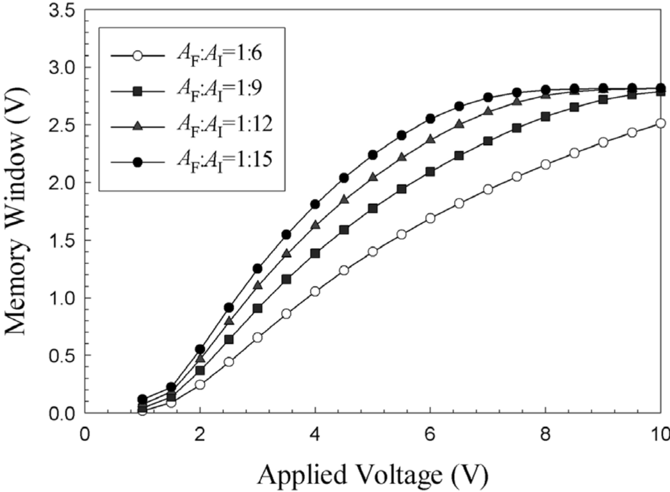

Fig. 4. Calculated memory window as a function of applied bias for the MFMIS capacitors at various area ratios.

are reduced and become close to the accumulation capacitances. The flat band voltages of the two branches of the CV curves are still symmetrical with respect to the origin ($V_G = 0$). However, this will result in an illusion of the slightly shift of the CV curves.

Fig. 4 shows the memory windows as functions of applied biases for the above MFMIS capacitors. For a small value of A_F/A_I, the memory window increases with increasing applied bias and attains the maximum value more rapidly. The calculated results are in good agreement with the reported experimental results [17]. The memory window is defined as the flat-band voltage shift of the two directions of CV curves. At the condition of flat-band where $\psi_s = 0$, both V_I and the polarization are equal to zero according to (12) and, therefore, the flat-band gate voltage is simply the voltage in ferroelectric, V_F. As a result, the maximum memory window corresponding to the saturation loop is given by $2E'_c t_F$, where E'_c is the electric field at which $P^+_{sat} = 0$, namely, from (4):

$$0 = P_s \tanh\left(\frac{E'_c - E_c}{2\delta}\right) + \varepsilon_F \varepsilon_0 E'_c. \tag{26}$$

If we first neglect the linear term $\varepsilon_F \varepsilon_0 E'_c$, $E'_c = E_c$, and the memory window equals $2E_c t_F$ [20]. If we incorporate this linear term, then the first order approximation of (26) gives:

$$E'_c = E_c \left(1 - 2\delta\, \varepsilon_F / P_s\right), \tag{27}$$

indicating that E'_c is a bit less than E_c. The maximum memory window is slightly reduced to:

$$\Delta V_{FB}(\max.) = 2E'_c t_F \approx 2E_c t_F \left(1 - 2\delta \varepsilon_F / P_s\right). \tag{28}$$

Eq. (28) is consistent with the result in Fig. 4.

Fig. 3 also illustrates the direction (counterclockwise) that hysteresis CV curve would follow. We now give a simple argument about the reason of this direction. If we start from a positive writing (gate) voltage ($V_W > 0$), the directions of electric field in the ferroelectric and the insulator are downward ($+x$ direction) based on the sign convention in Fig. 2. Consequently, the electric field is positive-valued, indicating the polarization should go along the upper-going branch P^-. At flat-band condition, $P^- = 0$, giving a negative value of electric field, $-E'_c$. Thus, the flat-band gate voltage, $-E'_c t_F$, is negative. Likewise, the flat-band gate voltage is $+E'_c t_F$ for negative writing voltage ($V_W < 0$). As a result, the hysteresis CV loop goes in a counterclockwise direction as shown in Fig. 3.

The MFMIS capacitor's memory windows as a function of bias voltage are further investigated at various material parameters, in Figs. 5–7. In Fig. 5, the dependence of memory window on the ratio of P_r/P_s is given. For a small value of P_r/P_s, the corresponding P-E curve becomes linear-like, leading the ferroelectric to behave like

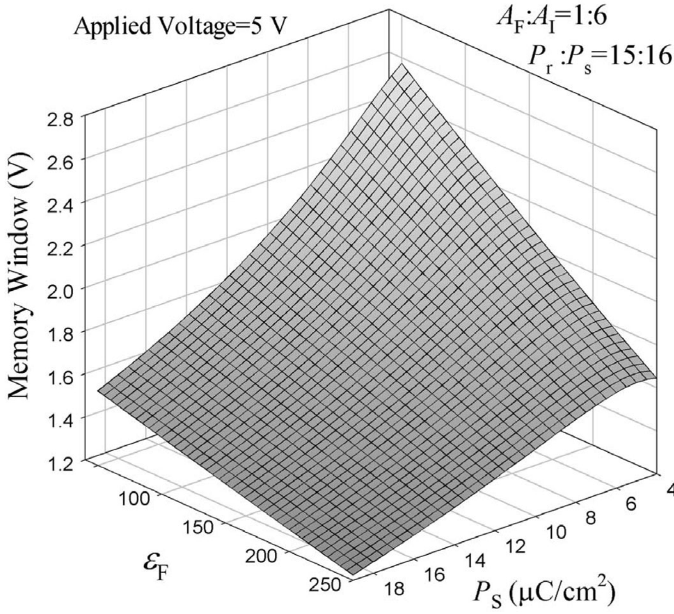

Fig. 6. Calculated memory window as a function of ε_F and P_s at a constant applied voltage of 5 V for the MFMIS capacitor with $A_F : A_I = 1 : 6$. The ratio of P_r/P_s is fixed at 15/16.

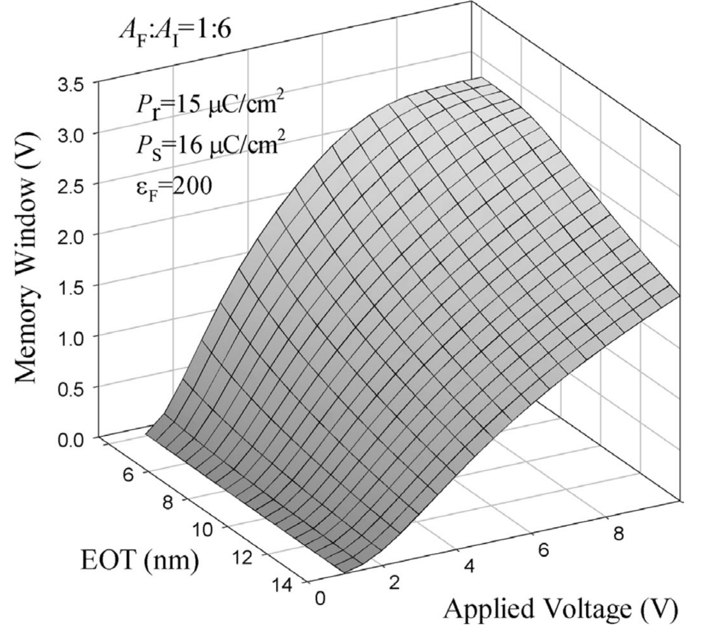

Fig. 7. Calculated memory window as a function of the applied voltage and EOT of the insulator for an MFMIS capacitor with $A_F : A_I = 1 : 6$.

paraelectric. Therefore, the memory window is expected to be small for a small value of P_r/P_s. The window, in general, increases with increasing applied bias and eventually attains a maximum value given by (28). Fig. 6 illustrates the effect of P_s and ε_F on the memory window at a constant applied voltage, ±5 V, while fixing the ratio of P_r and P_s. The memory window increases with decreasing P_s and ε_F. This can be understood in a simple way. In the case of the saturation situation, the polarization would be larger than P_s. The P_s is proportional to the amount of charges induced in the capacitor. Therefore, a larger value in P_s indicates that we need a higher gate voltage to induce the corresponding charges for the saturation. Conversely, it may imply that the memory window will decrease with increasing P_s at a constant applied voltage. However, decreasing ε_F also increases the memory window. But the effect of ε_F is less important than P_s because the ferroelectric layer itself is a nonlinear dielectric material in which the electric displacement D is contributed primarily by the nonlinear polarization rather than the linear one.

For most MFIS and MFMIS devices, high-k gate dielectrics often are used to increase the gate capacitances. Larger gate capacitances will provide better matching of the capacitances of MFM and MIS, giving rise to a better memory window. The insulators often are characterized by EOT ($EOT = t_I \varepsilon_{SiO_2}/\varepsilon_I$). The effect of EOT on the memory window is plotted in Fig. 7. It is seen that a small EOT of only several nanometers can obtain a better memory window at a low operation voltage.

B. FeMFET

Let us now start to investigate the current-voltage relation for the FeMFET. We begin with the study of the

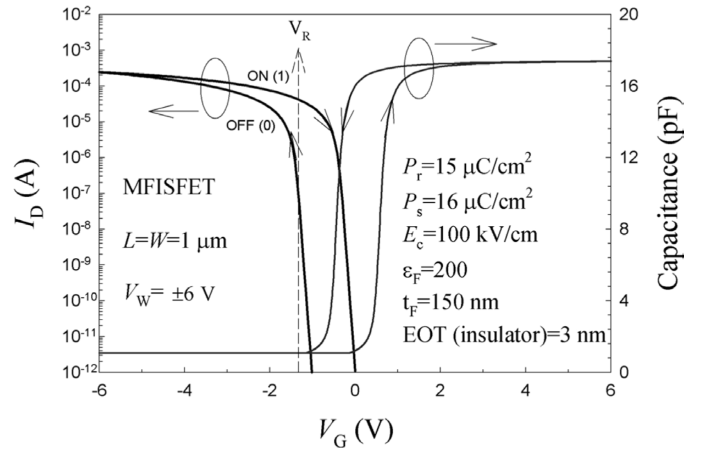

Fig. 8. The calculated CV and $I_D - V_G$ results for the MFIS capacitor and MFIS-FET. The ON state and OFF state are specified, and the direction of the memory window also is shown here. For better memory window, the EOT of the insulator is changed to 3 nm, and the applied voltage is 6 V.

MFIS-FET. The EOT is adjusted to 3 nm for the purpose of a suitable memory window. If the insulator is taken as a high-k gate dielectric such as $SrTiO_3$ (STO) with $\varepsilon_F \approx 39$ as compared with the experimental result (21), the physical thickness of the insulator is about 30 nm or so. The insulator with a large thickness can reduce the leakage current and then can prevent the dielectric breakdown. Fig. 8 illustrates the $I_D - V_G$ curve of an MFIS-FET, in which we also have included, in order for the convenience of comparison, CV relation of the associated MFIS capacitor. Here the voltage is swept from +6 V to −6 V, and vice versa. The memory window of the drain current is 1 V, equal to

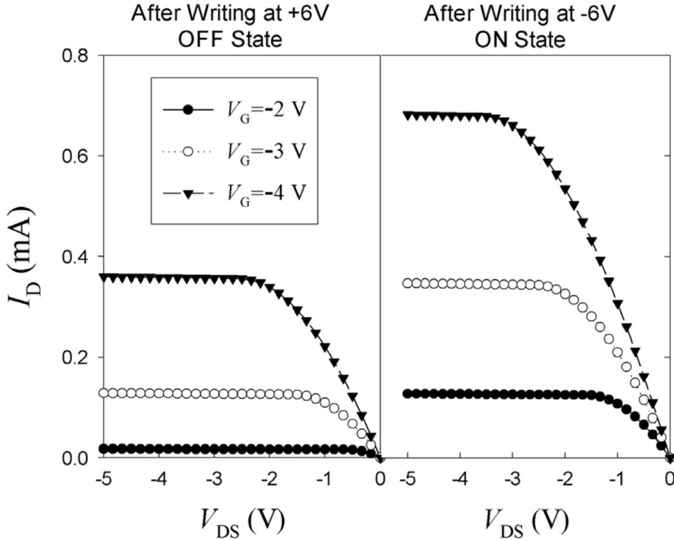

Fig. 9. The calculated $I_D - V_{DS}$ for the ON and OFF states at various gate voltages for an MFIS-FET. The device parameters are the same with Fig. 8.

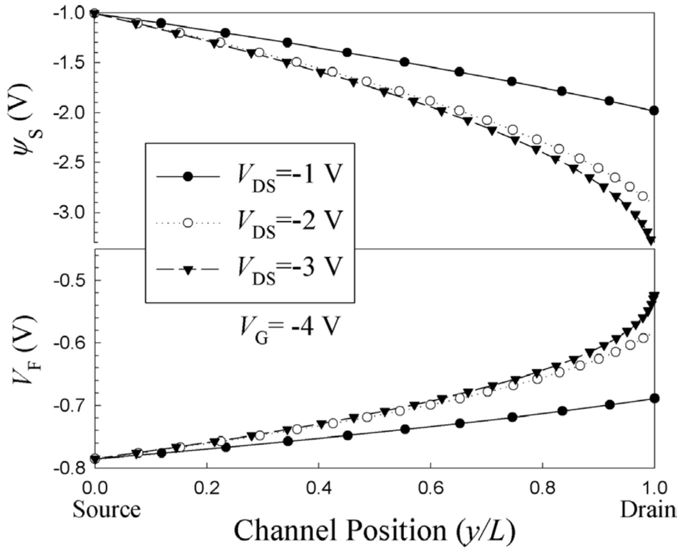

Fig. 10. Calculated surface band bending, ψ_3, and voltage across the ferroelectric, V_F, as functions of the channel position at various drain voltages for an MFIS-FET.

that of the CV curve. Smaller threshold voltage is defined as the ON state (or logic "1"); larger threshold voltage is denoted as the OFF state (Logic "0"). To get a better discrimination, the reading voltage, V_R, must be chosen to yield a large drain current in the ON state and low drain current in the OFF state. A suitable choice of V_R for an FeMFET is shown in Fig. 9 in which the drain current ratio $I_D(ON)/I_D(OFF)$ is larger than 10^3, which is suitable for the memory operation.

The dependence of the drain current on the drain voltage for both ON and OFF states at different gate voltages is plotted in Fig. 9. The drain current in the OFF state is smaller than that in the ON state at the same bias voltages. A simple insight can be obtained from Fig. 9. The

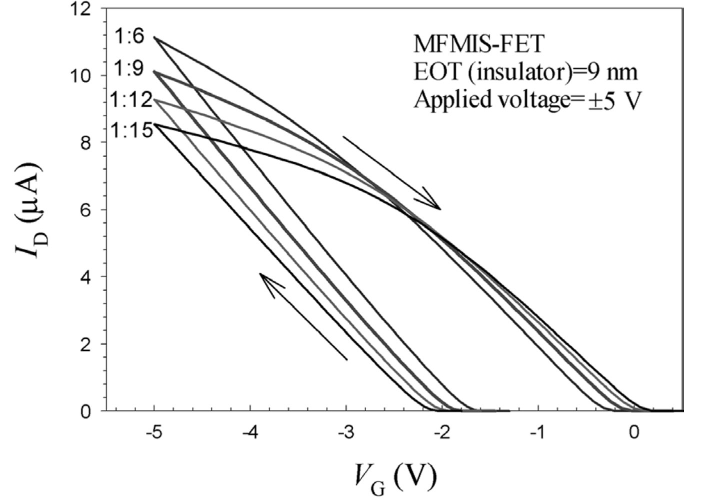

Fig. 11. Calculated $I_D - V_G$ for an MFMIS-FET at various area ratios of A_F/A_I. The material parameters are the same with Fig. 3.

threshold voltage in the OFF state is less than the ON state by about 1 V, namely the drain current of the ON state at $V_G = -3$ V is close to that of the OFF state with $V_G = -4$ V. Likewise, the drain current at $V_G = -2$ V (ON) is close to that at $V_G = -3$ V (OFF).

The voltages across the ferroelectric V_F and the surface band bending potential ψ_s as functions of the channel position for the FeMFET operated at $V_G = -4$ V of the OFF state are shown in Fig. 10. The calculation is based on (22)–(25). The band bending increases from the source to drain, and V_F decreases from source to drain. In the model of Miller and McWhorter [3], the voltages in the insulator and the ferroelectric are assumed to be constant for convenience of calculation. This assumption would lead to a large deviation at a large drain voltage according to results shown here. Accordingly, our model here appears to be more relevant and accurate because we have removed this limitation and, furthermore, the distributions of voltages also have been incorporated.

Fig. 11 displays the $I_D - V_G$ of the MFMIS-FET at various area ratios of $A_F/A_I = 1/6$, 1/9, 1/12, and 1/15 for the writing voltages of ±5 V. The EOT of the insulator is reset to 9 nm. The other parameters are the same as those of the MFMIS capacitors shown in Fig. 3. The memory window increases from 1.4 V to 2.3 V as A_F/A_I changes from 1/6 to 1/15. However, the drain currents decrease. This is due to the decrease in total gate capacitance of the MFMIS structure in which the area of MFM is decreased, as indicated by Fig. 3. The decreasing drain current is an obvious handicap that may limit the device performances, for example, the circuit speed and sensing margin. In addition, the reduced total gate capacitance may generate some serious short channel effects when devices are scaled down under submicron regimes. Therefore, certain trade-offs should be made between the memory window and the drain current.

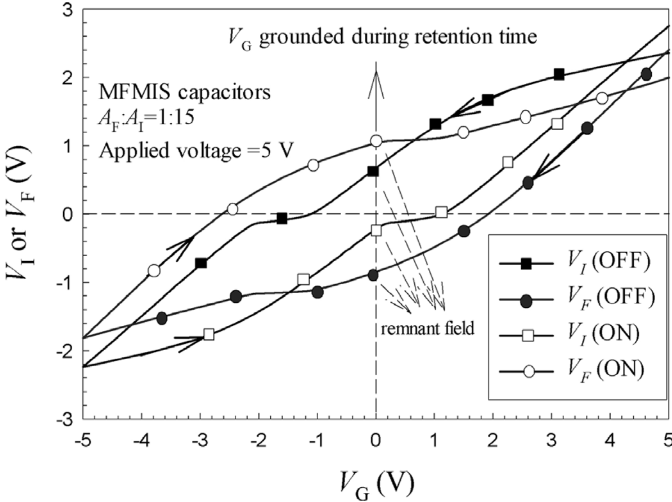

Fig. 12. The voltages across the ferroelectric and insulator of both ON and OFF states for MFMIS capacitor with $A_F/A_I = 1:15$.

C. Depolarization Field and Retention Time

Let us address the important issues on the depolarization field and retention time. Fig. 12 shows the voltages, including both the ON and OFF states, in the ferroelectric and insulator film as a function of gate voltage for the MFMIS capacitor with an area ration of 1:15. These voltages are obtained from the CV simulation in Fig. 3. The depolarization field is the remanant electric field in the ferroelectric thin film when the gate voltage is grounded during data retention time. This field may cause charge injection [22] and reduction of the remanent polarization. The charge injection will reduce the memory window as well as the current ON/OFF ratio after the retention time. According to Fig. 12, the remanant voltage in the ferroelectric thin film for the OFF state is -0.8 V, which is opposite to the direction of the initial state. Because the direction of the remanant electric field in the ferroelectric film is reverse relative to the original applied field, we called this electric field the depolarization field. The depolarization fields in the ferroelectric film for the OFF and ON states are calculated to be -50 kV/cm and 70 kV/cm, respectively. Similarly, the remanant fields in the insulator for the OFF and ON states are calculated to be 700 kV/cm and -200 kV/cm, respectively. We found that the remanant fields in the insulators are much larger than the depolarization fields in the ferroelectric films because of the relatively small dielectric constants of insulators compared with the ferroelectrics. Therefore, we suggest that the retention times are primarily limited by the leakage currents of insulators rather than the ferroelectric layers for most FeMFET's. This situation is quite similar to that of the floating gate devices that compose the flash memory. In order to sustain the retention time of the flash memory, there is a limit of the shortest thickness of the tunneling oxide (about 7 nm SiO_2) [23]. In an analogous manner, we expect that there also exists scaling limit of the film thickness for the FeMFETs if data retention time should be maintained. In case the data retention time is not satisfactory for the nonvolatile memory application, refreshable operation of FeMFETs such as FeDRAM [10], [11] may be a better choice.

IV. Conclusions

A systematical theoretical approach for the analyses of electrical characteristics for the ferroelectric-based capacitor and field-effect transistor has been given. We have proposed a new analytical expression for the unsaturated hysteresis loop for the ferroelectric material. Based on this model, we have successfully analyzed the operational properties for the FeMFET's and capacitors. In the analysis of drain current for the FeMFET, we have used Pao and Sah's [13] double integral to account for the inhomogeneous electric field along the channel. The simulation results agree well with the reported data. The present model enables one to accurately model the FeMFETs for the device design.

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