Effects of Process Temperature on Polysilicon Thin Film Transistors with Liquid-Phase Deposited Oxides as Gate Insulators

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ABSTRACT

Liquid-phase deposited (LPD) oxide has previously been successfully applied to low temperature processed polysilicon thin film transistors (poly-Si TFTs) as a gate insulator. This paper shows the feasibility of applying room temperature deposited LPD oxide to high temperature processed devices. The thermal effects of high temperature processing on poly-Si TFTs including postoxide annealing and dopant activation have been investigated. These high temperature treatments show excellent improvement in device characteristics. In addition, the novel devices also show considerably more efficient hydrogenation during NH_3-plasma treatment, and their reliability under dc electrical stress appears similar to that of conventional poly-Si TFTs.

Introduction

To develop active matrix liquid crystal displays (AMLCDs), polysilicon thin film transistors (poly-Si TFTs) in peripheral device circuits must be fabricated either on quartz or on large area glass substrates.[1] In addition, in the application of three-dimensional integrated circuits, particularly to static random access memories (SRAMs), poly-Si TFTs are stacked on the top of active elements.[2] To date, several gate insulator growth methods have been developed to obtain high performance poly-Si TFTs using either high temperature or low temperature processes.[3-6] Recently, great interest has been shown in liquid phase deposited (LPD) oxide films because of their excellent film properties and successful application as gate insulators to low temperature processed (LTP) poly-Si TFTs.[6-8]

In the application of high temperature-processed (HTP) poly-Si TFTs to SRAMs and quartz based LCDs, thermal oxidation is one of key technologies and can grow high quality gate oxides to bring excellent device characteristics. However, thermal oxidation at high temperature (>850°C) has been found to degrade the mobility of poly-Si TFTs.[9-11] The low temperature deposited oxide is an alternative method for forming gate insulator. Various chemical vapor deposition (CVD) methods have been used to fabricate the gate oxide.[3,4] But all of these CVD methods require expensive equipment and the processes involved are very complex. Therefore, we have developed the LPD method to fabricate gate oxide at room temperature. The LPD apparatus used is simple and inexpensive.[6-8] LPD oxide technology is thus an economical candidate for replacing high cost CVD technologies. To assess the feasibility of applying LPD oxide to HTP poly-Si TFTs, the thermal effects of high temperature processing on TFT performance have to be clarified. In this paper, we focus on the thermal effects of gate oxide annealing and dopant activation of poly-Si TFTs with LPD oxide gate insulators.

In addition, in the poly-Si film there still exists lots of grain boundary defects as well as intragrain defects. It is generally necessary to passivate these defects with hydrogen plasma to improve poly-Si TFT performance.[12,13] In this paper, investigation into the effects of NH_3-plasma passivation[6] on high temperature treated poly-Si TFTs is reported. Moreover, the stability of the novel poly-Si TFTs is of significant importance from the standpoint of long-term operation, so the effects of dc electrical stress on TFT performance are also clarified.

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Experimental

The four groups of conventional top gate N-channel poly-Si TFTs shown in Table I were prepared at different temperatures for gate oxide annealing and dopant activation. They are labeled group L-L, group H-L, group L-H, and control. L-L means low gate oxide annealing temperature (600°C) and low dopant activation temperature (600°C). H-L means high gate oxide annealing temperature (900°C) and low dopant activation temperature (600°C). L-H means low gate oxide annealing temperature (600°C) and high dopant activation temperature (900°C). Group L-L was the conventional LTP poly-Si TFT. Group H-L evaluated the thermal effects of gate oxide annealing on TFTs, while group L-H evaluated the thermal effects of dopant activation. The control sample was the conventional HTP poly-Si TFT. The inset in Fig. 1 shows the cross-sectional structure of poly-Si TFTs.

Group L-L, group H-L, and group L-H were prepared according to the following procedures. A 100 nm thick LPCVD amorphous Si layer was deposited on thermal oxide using SiH_4 gas at 550°C, and recrystallized at 600°C for 24 h using the solid-phase crystallization (SPC) method. After the SPC poly-Si layer was patterned to the active region, a 47 nm thick gate oxide layer was grown on the active layer using the LPD method at 18°C.[14] For groups L-L and L-H, gate oxide annealing was performed at 600°C for 1 h in N_2 ambient. For groups H-L, gate oxide annealing was performed at 900°C for 1 h in N_2 ambient. Then, the 300 nm thick poly-Si gates were deposited using the LPCVD method at 620°C. After the poly-Si gates were patterned, the source/drain and gate regions were doped using phosphorus self-aligned ion implantation with an energy of 40 keV and a dose of 5×10^{15} cm^{-2}. The LPD oxide upon source/drain regions was not removed, and

Table I. Processing conditions for four TFT samples labeled groups L-L, H-L, L-H, and control.

Samples	Gate insulator	Gate-oxide annealing	Dopant activation	NH_3-Plasma treatment
Group L-L	LPD oxide ((18°C)	600°C, 1 h (L)	600°C, 24 h (L)	
Group H-L	LPD oxide (18°C)	900°C, 1 h (H)	600°C, 24 h (L)	300°C,
Group L-H	LPD oxide (18°C)	600°C, 1 h (L)	900°C, 30 min (H)	0 ~ 5 h
Control	Dry O_2 (900°C)	None	900°C, 30 min (H)	

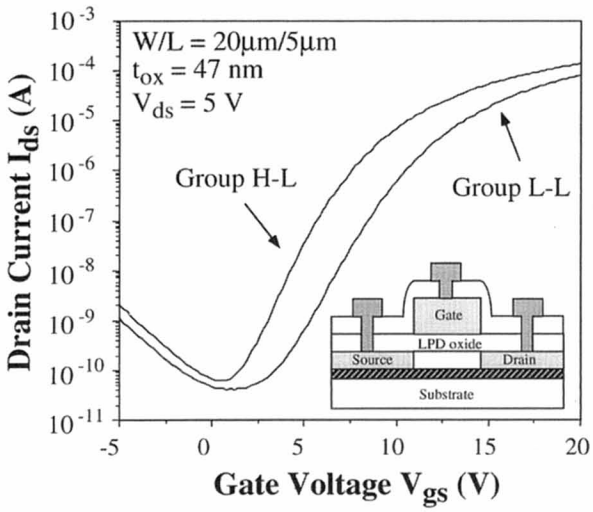

Fig. 1. Transfer characteristics ($I_{ds} - V_{gs}$) of poly-Si TFTs (W/L = 20 μm/5 μm) at V_{ds} = 5 V for groups L-L and H-L without hydrogenation. The inset shows the cross-sectional structure of poly-Si TFTs.

then acts as the screen oxide for ion implantation. For groups L-L and H-L, dopant activation was performed at 600°C for 24 h in N_2 ambient. For group L-H, dopant activation was performed at 900°C for 30 min in N_2 ambient. Then, the 500 nm thick oxide interlayer was formed using the PECVD method at 300°C. After the contact holes were opened, 500 nm thick aluminum electrodes were deposited and patterned. Finally, sintering was performed at 400°C for 30 min in N_2 ambient.

For the control poly-Si TFTs, 47 nm thick gate oxides were prepared using dry oxidation at 900°C without postoxidation annealing, while dopant activation was performed at 900°C for 30 min in N_2 ambient. Other procedures are the same as those of group L-L, group H-L, and group L-H.

To passivate the trap states in the poly-Si channel, NH_3-plasma hydrogenation was performed for all four groups in a parallel plate reactor at 300°C with a power density of 0.7 W/cm^2.

Results and Discussion

Effects of processing temperature.—Figure 1 shows the typical transfer characteristics at V_{ds} = 5 V for groups L-L and H-L without NH_3-plasma treatment. The detailed key device characteristic parameters including threshold voltage (V_{th}), subthreshold swing (S.S.), field-effect mobility (μ_{FE}), and ON/OFF current ratio (I_{on}/I_{off}) are shown and analyzed in Table II. We can see that the characteristics of TFTs with high temperature annealed gate oxides (group H-L) are superior to those of conventional LTP devices (group L-L). These improved characteristics, especially their V_{th} and S.S., can be attributed to restructuring in the LPD gate oxide and reduction in trap states in the poly-Si film due to postoxide high temperature annealing.

As previously reported,[15] essential Si-OH and Si-F bonds exist in as-deposited LPD oxides and greatly affect oxide properties and device characteristics. In the case of gate oxide annealing at 600°C, SiO-H bonds can break, forming large numbers of negatively charged SiO^-. These charges may be the main cause of the high V_{th} in group L-L. While annealing at 900°C, in addition to SiO^- generation, the Si-F bonds even break. The resulting positive Si^+ charges will electrically neutralize many of the negatively charged SiO^-; this is shown by the low V_{th} in group H-L. A decrease in Si-F bonds in LPD oxide film during high temperature annealing was observed in FTIR spectra. Figure 2 shows typical FTIR spectra in the region of 700 ~ 1500 cm^{-1} for the as-deposited and the annealed LPD oxides. In samples annealed at 900°C, the Si-F stretching vibration band (located at 930 cm^{-1}) has completely disappeared, and the annealed LPD oxide has come to resemble thermal oxide.[15] Changes in oxide charges due to annealing were also confirmed by the flatband voltage (V_{FB}) shifts in MOS capacitors made from them. MOS capacitors with aluminum gates are not sintered. MOS capacitors made from LPD oxide annealed at 600°C show a V_{FB} of −0.19 V, while those made from LPD oxide annealed at 900°C show a V_{FB} of −1.05 V. The significant negative shift in V_{FB} implies that lots of positive charges are generated in LPD oxides due to annealing at 900°C.

In addition, the difference in S.S. between group L-L and group H-L is also correlative with fluorine (F) concentrations in LPD oxides. After 900°C annealing, the diminution in F concentrations causes increases in the dielectric constant of LPD oxide and resultantly in the capacitance.[16,17] This is also a reason for the lower S.S. in group H-L samples.[18]

As shown above, high temperature postoxide annealing is effective in enhancing the quality of LPD oxide and in improving the characteristics of poly-Si TFTs. However, in fabricating HTP poly-Si TFTs, dopant activation also needs high temperature annealing. Whether the high temperature annealing for dopant activation can availably replace postoxide annealing to improve oxide quality is an interesting issue. We next discuss the effects of annealing for dopant activation on TFT performance.

Figure 3 shows a comparison of typical transfer characteristics at V_{ds} = 5 V for groups H-L, L-H, and control samples without NH_3-plasma treatment. The key device characteristic parameters are also presented and analyzed in Table II. As shown in Fig. 3 and in Table II, group L-H samples showed excellent characteristics including a low V_{th} of 7.34 V, a low S.S. of 1.15 V/dec, a high μ_{FE} of 21.48 cm^2/V s and a high ON-current (I_{on}) of 215 μA. The increases in μ_{FE} and I_{on} can be attributed to the decrease in drain/source sheet resistance,[19,20] which was 238 Ω/□, but 478 Ω/□ for group H-L samples. Distinguishing features can be seen more clearly in the output characteristics ($I_{ds} - V_{ds}$). Figure 4 shows the typical output characteristics ($I_{ds} - V_{ds}$) of poly-Si TFTs for groups H-L and L-H with V_{gs} as a parameter. High temperature dopant activation indeed achieves a lower sheet resistance and overwhelmingly enhances the on-state performance. In addition, compared with group L-L, group L-H also exhibits a lower V_{th}. This indicates that high temperature annealing for dopant activation can also restructure the LPD gate oxide. In total, for group L-H the high temperature treatment effectively acts not only as a dopant activator, but also as a gate oxide annealant.

In comparison with the control HTP TFTs, all performance indexes for group L-H appear favorable; especially the μ_{FE} of 21.48 cm^2/V s is excellent. It appears that TFTs with LPD gate oxides can have perfect SiO_2/poly-Si inter-

Table II. Device characteristic parameters before hydrogenation for groups L-L, H-L, L-H, and control.

Sample \ Parameter	V_{th} (V)	S.S. (V/dec)	μ_{FE} (cm^2/V s)	I_{on}/I_{off}	I_{on} (μA)	I_{off} (pA)
Group L-L	9.60	1.53	13.49	2.0×10^6	83.8	41.85
Group H-L	6.73	1.24	14.80	2.2×10^6	142	63.10
Group L-H	7.34	1.15	21.48	4.2×10^6	215	51.60
Control	6.05	1.13	10.86	1.9×10^6	136	70.55

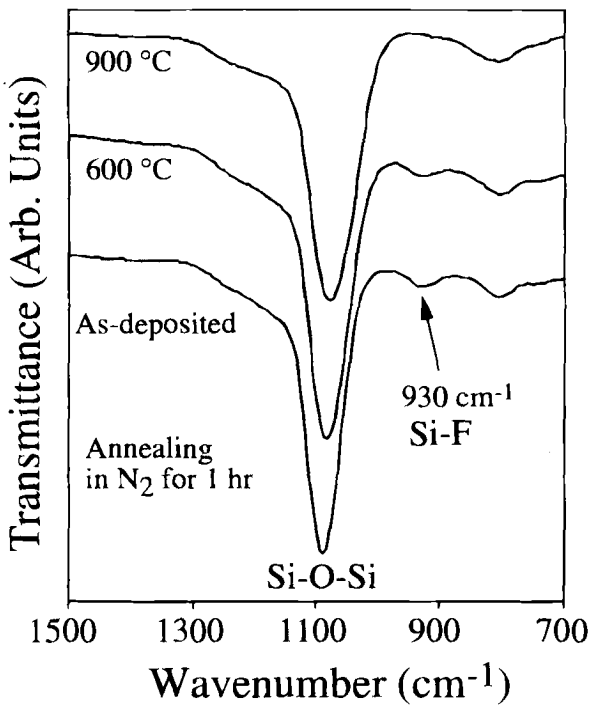

Fig. 2. Changes in FTIR spectra in the range of 700 ~ 1500 cm^{-1} for as-deposited and annealed LPD oxides.

faces, while the control TFTs are quite prone to serious roughness problems at SiO_2/poly-Si interfaces owing to thermal oxidation.[9-11]

From the above comparisons among all samples, it can be concluded that as long as high temperature annealing for dopant activation is performed for poly-Si TFTs with LPD gate oxides, more satisfactory device characteristics can be achieved as compared to those exhibited by conventional HTP TFTs with thermal gate oxides.

Effects of NH_3-plasma treatment.—Figure 5 shows the typical transfer characteristics of groups L-L and L-H at V_{ds} = 5 V before and after 5 h NH_3-plasma treatment. NH_3-plasma treatment improved the performance of both groups. However, the improvement in group L-H is more evident. To further investigate the effects of NH_3-plasma passivation, the device characteristics were evaluated as a function of NH_3-plasma treatment time. Figures 6 and 7

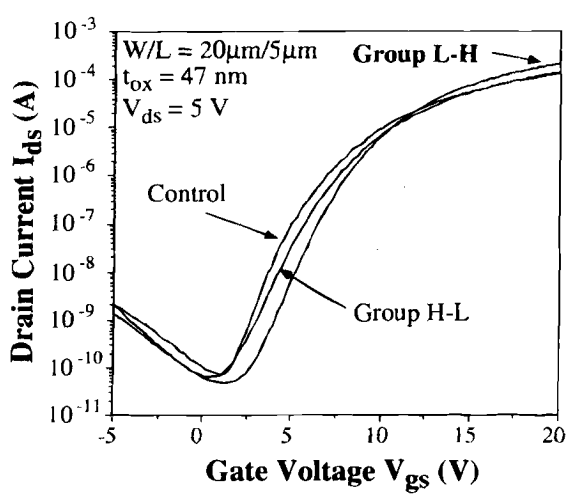

Fig. 3. Transfer characteristics (I_{ds} – V_{gs}) of poly-Si TFTs (W/L = 20 μm/5 μm), at V_{ds} = 5 V for groups H-L, L-H, and control without hydrogenation.

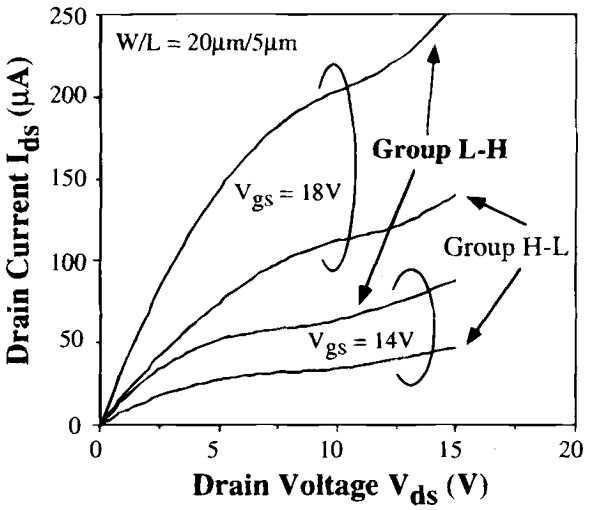

Fig. 4. Output characteristics (I_{ds} – V_{ds}) of poly-Si TFTs (W/L = 20 μm/5 μm) with V_{gs} as a parameter for groups H-L and L-H without hydrogenation.

show the variations in V_{th} and μ_{FE} with NH_3-plasma treatment time, respectively, for groups L-L, H-L, L-H, and control. For group L-L, the improvement in V_{th} and μ_{FE} was slight compared with that of the other groups. It has been reported that V_{th} is mainly influenced by dangling bond midgap states, while μ_{FE} is influenced by band tail states in poly-Si TFTs.[21] In other words, in high temperature treated devices, the two kinds of trap states are efficiently passivated by NH_3-plasma treatment. The variations in trap state density (N_t) with NH_3-plasma treatment time for four groups are shown in Fig. 8. The trap state density (N_t) existed in the poly-Si channel is calculated by extracting a straight line on the plot of ln $[I_{ds}/(V_{gs} - V_{FB})]$ *vs.* $1/(V_{gs} - V_{FB})^2$ at low V_{ds} and high V_{gs} based on the following equation[22]

$$I_{ds} = \left(\frac{W}{L}\right) C_{ox} V_{ds} \mu_{FE} V_{gs} \exp\left(\frac{-q^3 N_t^2 L_c}{8\epsilon_{Si} kTC_{ox} V_{gs}}\right) \quad [1]$$

where C_{ox} is the gate oxide capacitance, q is the electron charge, k is Boltzmann's constant, ϵ_{Si} is the silicon dielectric constant, and T is the temperature. L_c is the channel thickness[23]

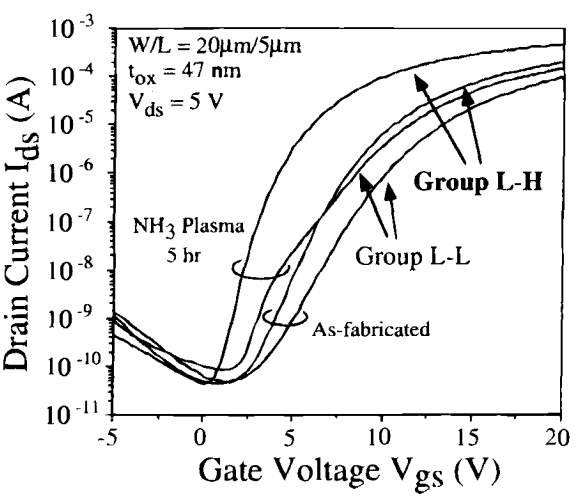

Fig. 5. Transfer characteristics (I_{ds} – V_{gs}) of poly-Si TFTs (W/L = 20 μm/5 μm) at V_{ds} = 5 V for groups L-L and L-H before and after 5 h NH_3-plasma treatment.

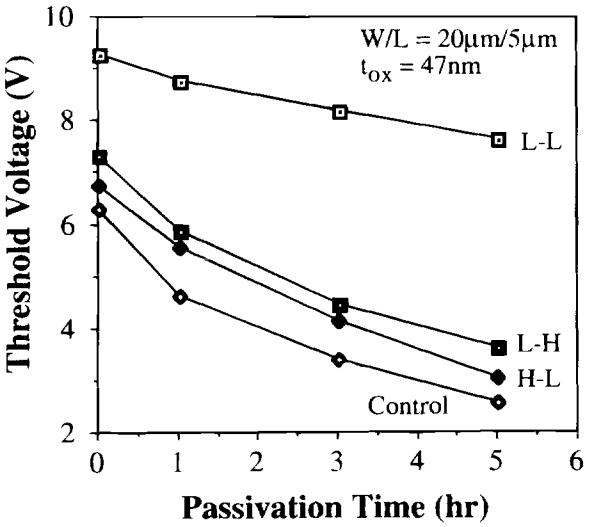

Fig. 6. Variations in threshold voltage with NH_3-plasma passivation time for groups L-L, H-L, L-H, and control (W/L = 20 μm/5 μm).

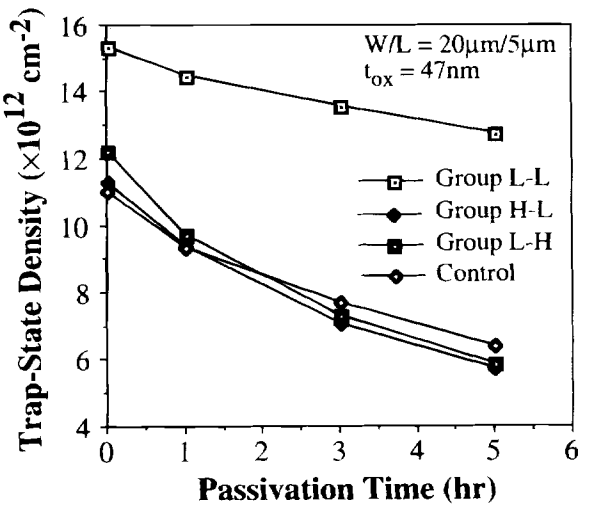

Fig. 8. Variations in trap-state density with NH_3-plasma passivation time for groups L-L, H-L, L-H, and control (W/L = 20 μm/5 μm).

$$L_c = \frac{8kTt_{ox}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{SiO_2}}}}{q(V_{gs} - V_{FB})} \quad [2]$$

where t_{ox} is the gate oxide thickness, ϵ_{SiO_2} is the dielectric constant of gate oxide, and V_{FB} is the gate voltage at which minimum leakage current occurs. For groups H-L, L-H, and control, the N_t reduction rate caused by NH_3 plasma was considerable, while that in group L-L was slight. This is consistent with the results shown in Fig. 6 and Fig. 7, and indicates that the passivation rates for both tail trap states and midgap trap states were significantly increased for high temperature treated poly-Si TFTs.

In our previous report, the shrinkage of LPD oxide after 300, 600, 900, and 1000°C annealing for 1 h in N_2 is about 0.07, 1.58, 2.43, and 3.22%, respectively.[24, 25] The quality of LPD oxide after 1000°C annealing is nearly the same as that of thermal oxide, and nearly unchanged under the subsequent annealing. Hence, the differences of LPD gate oxide thickness between LTP and HTP TFTs are small. We can also find that the change from thickness of LPD gate oxide has a small influence on mobility in the comparison between group L-L and group H-L as shown in Table II. Therefore, for high temperature treated TFTs, the fast changes in mobility during hydrogenation are not due to the changes in LPD oxide thickness. In addition, the gate oxides of the control TFTs are different from those of group H-L and L-H. However, group H-L, group L-H, and control TFTs exhibit the same hydrogenation efficiency. We can neglect the influence of LPD gate oxide on mobility during NH_3-plasma treatment.

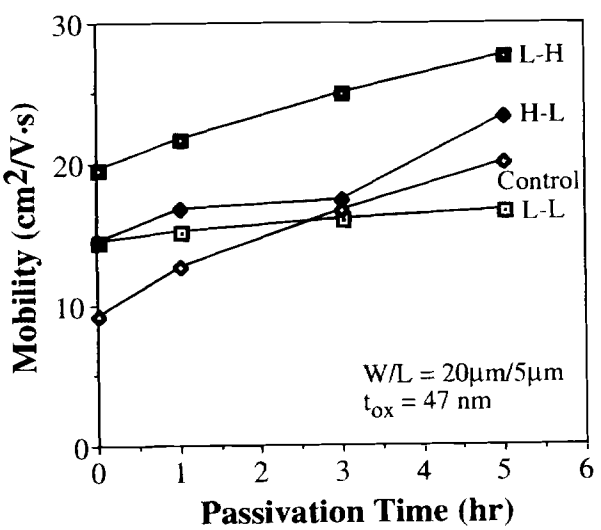

Fig. 7. Variations in field-effect mobility with NH_3-plasma passivation time for groups L-L, H-L, L-H, and control (W/L = 20 μm/5 μm).

In general, the effects of thermal annealing on poly-Si TFT characteristics are densification in gate oxide, reduction in N_t of poly-Si channel, and efficient dopant activation. Drain/source sheet resistance does not correlate with the hydrogenation efficiency,[26] which can be found in the comparison between group H-L and group L-H. Densification in gate oxide will reduce the defects in oxide, which may slow the hydrogen diffusion. Hence, we believe that the higher hydrogenation efficiency is related to the reduction in N_t of poly-Si channel for high temperature treated TFTs. It has been reported that midgap states have a faster response to hydrogenation, while tail states respond slower to hydrogenation. Only when the hydrogenation concentration is so large as to fill both the midgap states and the tail states will a significant fraction of the tail states be passivated. Moreover, if the interior of grains contains a large number of tail states, the passivation rate will be slow for this type of defects.[27] For high temperature treated TFTs in this research, both densities of the midgap states and the tail states were reduced by the high temperature annealing. Since the density of midgap states was lowered by annealing, this type of defects can be fast filled at the beginning of hydrogenation. Hence, other excess hydrogen atoms can then fast passivate the tail states. The tail states can also have a fast response to hydrogenation. Therefore, at the same hydrogenation condition, both the midgap states and the tail states can be passivated faster then those in group L-L.

Reliability.—The reliability of high temperature treated poly-Si TFTs with LPD oxide gate insulators was investigated under dc electrical stress. Figure 9 shows the changes in V_{th} and S.S. for group L-H as a function of stress time during ON-state stressing with $V_{gs} = V_{ds}$ = 15 V. Both the changes in ΔV_{th} and ΔS.S. are defined as Δ(%)=(after stress-before stress)/(before stress) × 100%. Devices with W/L = 5/5 μm had been treated in NH_3 plasma for 7 h before stressing. Both V_{th} and S.S. increased with stress time. However, the changes in μ_{FE} and minimum OFF-current after stressing were slight. The stress results for the forward and reverse modes are nearly the same. Hence, the

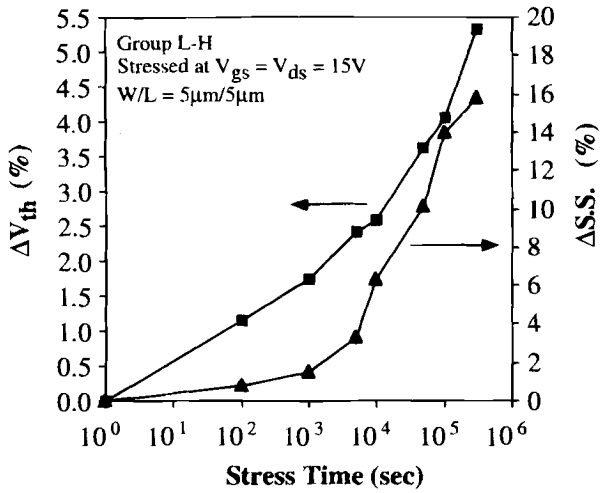

Fig. 9. Degradation rates of threshold voltage (V_{th}) and subthreshold swing (S.S.) for group L-H as a function of stress time under the stress with $V_{gs} = V_{ds} = 15$ V ($W/L = 5/5$ μm).

degradation in group L-H is accounted for by the increase in midgap defects within the poly-Si channel caused by channel carriers.[28] Since the LPD oxide was restructured by high temperature annealing and came to resemble thermal oxide, interface and bulk dielectric charge-trapping were not the dominant degradation mechanisms as they are in conventional HTP poly-Si TFTs.[28]

Conclusions

The thermal effects of high temperature processing, including postoxide annealing and dopant activation, on poly-Si TFTs with LPD gate insulators were investigated. The characteristics of TFTs with 900°C annealed LPD gate oxides were superior to those of conventional LTP devices because of densification in the LPD gate oxide and reduction in trap state density. Poly-Si TFTs with only a high temperature dopant activation processing even exhibited more excellent characteristics than conventional HTP poly-Si TFTs with thermal gate oxides due to their perfect SiO_2/poly-Si interfaces, as well as their restructured LPD gate oxides and efficient dopant activation. For these high temperature treated devices, both the dangling bond midgap states and the band tail trap states were more efficiently passivated during NH_3-plasma treatment. The instability mechanism of high temperature treated TFTs with LPD gate oxides is accounted for by the generation of carrier induced midgap states within the channel. In conclusion, it has been shown feasible to apply the novel LPD gate oxides as gate insulators to HTP poly-Si TFTs.

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