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Current gains of AlAs/GaAs tunnelling emitter bipolar transistors with 25–500Å barrier thickness

H.R. Chen, C.P. Lee, C.Y. Chang, K.L. Tsai and J.S. Tsang

Indexing terms: Semiconductor devices, Heterojunction bipolar transistors, Tunnelling structures

The current gain of an AlAs/GaS tunnelling emitter bipolar transistor (TEBT) is found to increase monotonically with barrier thickness in the range 25–200Å and fall off for barrier thickness increasing from 200 to 500Å. It is found that a thicker barrier can suppress the base-to-emitter hole injection better and increase the current gain, but a barrier which is too thick decreases the current gain due to the suppression of the electron current.

In the last few years, there has been an increasing interest in applying the tunnelling barrier as an effective mass filter [1]. Xu and Shur proposed a new AlGaAs/GaAs bipolar transistor structure [2], the TEBT, in which an AlGaAs tunnelling barrier was inserted between the emitter and base of a GaAs bipolar transistors to increase the emitter injection efficiency due to the very large difference in the tunnelling probabilities for electrons and holes. One major advantage of the TEBT over the conventional HBT is its reduction in the emitter size effect [3,4] caused by non-equilibrium electron transport. Many experimental results including the the DC [5] and AC [3] characteristics of the TEBT have been demonstrated. In this Letter, the AlAs/GaAs TEBT with barrier thicknesses ranging from 25 to 500Å were characterised.

The films were grown by molecular beam epitaxy (MBE) in a Varian Gen II system on (100) oriented n^+-GaAs substrate. The growth rate was 1μm/h and the substrate temperature was 580°C. Si and Be were used as n- and p-type dopant, respectively. The layers, beginning from the substrate, consisted of an n^+-GaAs buffer layer (2000Å, 3×10^{18}cm^{-3}), n^--GaAs collector (5000Å, 5×10^{16} cm^{-3}), p^+-GaAs base (700Å, 5×10^{18}cm^{-3}), i-AlAs barrier (25–500Å), and n^+-GaAs cap layer (2000Å, 3×10^{18}cm^{-3}). A 100Å undoped GaAs spacer was inserted between the base and barrier. Five samples with barrier thicknesses of 25, 50, 100, 200, and 500Å were studied. The wafers were then fabricated by conventional liftoff and wet etching procedures. The emitter had a 120μm diameter.

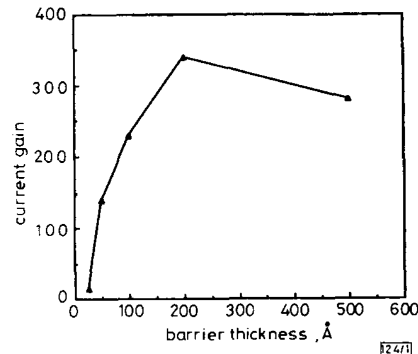

Fig. 1 *Common-emitter current gain as a function of barrier thickness*

Fig. 1 shows the results of the measured current gain as a function of barrier thickness. The current gains of these devices are 3, 140, 230, 340, and 280 for the TEBT with 25, 50, 100, 200 and 500Å barrier thickness, respectively. The current gain increases rapidly for barrier thicknesses less than 50Å and this increment slows down in the range 50–200Å. The current gain, on the other hand, decreases as the barrier thickness increases from 200 to 500Å. Fig. 2 shows the base transfer characteristics of these device at V_{CE} = 2.75V. The base current decreases with barrier thickness and this reduction is more apparent for thin barriers. This base current reduction, resulting from the better hole confinement of the thicker barrier, gives rise to the current gain increment for barrier thicknesses increasing from 25 to 200Å. The hole injection from the base to emitter can be accomplished either by tunnelling or by thermionic emission. The tunnelling probability P across a flat barrier can be expressed as

$$P = \exp\left(-\frac{4\pi L_B}{h}\sqrt{2m_{lh}(\Delta E_V - E)}\right) \qquad (1)$$

where L_B, ΔE_V, and m_{lh} are the barrier thickness, valance band discontinuity and light hole effective mass, respectively. The thermionic emission current density is given by

$$J = A^{**}T^2\exp(-qL_B/kT)[\exp(qv/kT) - 1] \qquad (2)$$

where A^{**} is the effective Richardson constant for thermionic emission, and V is the applied voltage.

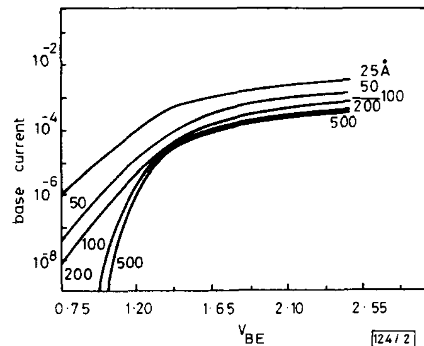

Fig. 2 *Base transfer characteristics of the TEBTs studied at VCE = 2.75 V*

From eqn. 1, the tunnelling probability can be dramatically reduced by increasing the barrier thickness L_B while the thermionic emission current, from eqn. 2, is independent of barrier thickness and is dependent on valence band discontinuity only. For a very thin barrier, the tunnelling component dominates and the base

current can be reduced significantly by increasing the barrier thickness. However, for a thicker barrier, the thermionic emission current becomes important and the base current is less sensitive to the barrier thickness, as can be seen in Fig. 2. This base current behaviour makes the current gain increase rapidly with barrier thickness for thin barriers and this rate of increase reduces for a thicker barrier, as shown in Fig. 1.

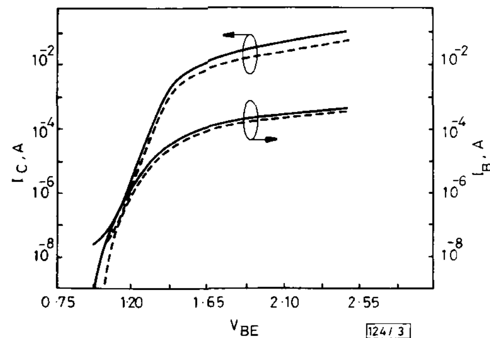

Fig. 3 *Collector and base transfer characteristics of TEBT with 200 and 500Å barrier thickness at V_{CE} = 2.75 V*

—— 200Å
- - - - 500Å

Fig. 3 shows the base and collector transfer characteristics of the TEBT with 200 and 500Å barrier thickness. Both the base and collector current of the TEBT with 500Å barrier are less than those of the TEBT with 200Å barrier. However, the discrepancy of base current is smaller because thermionic emission dominates the base current. The barrier thickness of 500Å severely retards the tunnelling electrons and the collector current apparently reduces. As a consequence, the current gain falls off for barrier thickness increasing from 200 to 500Å.

In summary, we have studied the current gain characteristics of TEBTs with barrier thickness varying from 25 to 500Å. The current gain increases rapidly with barrier thickness in the range 25–50Å and this increment slows down in the range 50–200Å. On the other hand, the current gain decreases as the barrier thickness increases from 200 to 500Å.

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H. R. Chen, C. P. Lee, C. Y. Chang, K. L. Tsai and J. S. Tsang (*Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, Republic of China*)

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Current-injection ECL/CML for AlGaAs/GaAs HBTs

T.Y.K. Wong

Indexing terms: Heterojunction bipolar transistors, Emitter-coupled logic

A novel 'current-injection' circuit topology is presentec that requires lower supply voltage, and demonstrates smaller propagation delay and outperforms classical 2-level emitter-coupled logic/current-mode logic (ECL/CML) in AlGaAs/GaAs heterojunction bipolar transistor (HBT) technology. Test circuits were wafer-probed at 10Gbit/s with full functionality, and operating clock frequency up to 20GHz is recorded.

Introduction: An ECL/CML structure is commonly used in high speed digital circuits [1, 2]. Fig. 1 shows an input stage of a classical 2-level logic. A level 1 (LV1) differential pair Q1-Q2 or Q3-Q4 can be enabled, by switching on cascaded level 2 (LV2) transistor Q5 or Q6. The propagation delay from LV2 inputs (IN2/NIN2) to LV1 outputs (OUTA/NOUTA and OUTB/NOUTB) is the sum of the delays through transistors LV1 and LV2. The output current is I1 less two base currents.

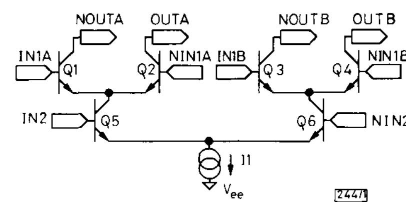

Fig. 1 *Input stage of classical two-level ECL/CML*

Fig. 2 shows an alternative method to implement 2-level ECL/CML. It comprises LV1 differential pairs Q1-Q2 and Q3-Q4, LV2 current-injection transistors Q5-Q6, and constant-current sources I1 and I2. In order for Q5 or Q6 to inject current into I1 or I2 to

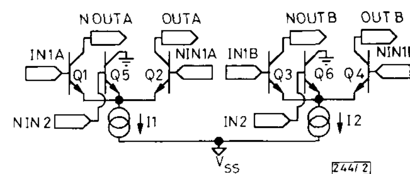

Fig. 2 *Input stage of current-injection two-level ECL/CML*

disable Q1-Q2 or Q3-Q4, the base voltage of Q5 or Q6 needs to be higher than the logic high applied to the bases of Q1-Q2 or Q3-Q4 by a few times the thermal voltage V_t. To enable Q1-Q2 or Q3-Q4, the base voltage of Q5 or Q6 needs to be lower than the logic high applied to the bases of Q1-Q2 or Q3-Q4 by a few times V_t. Because LV1 and LV2 transistors are not in cascade, Fig. 2 requires ~1 V_{BEon} less voltage headroom than Fig. 1. Owing to differential switching between LV1 and LV2 transistors, the propagation delay from LV2 inputs to LV1 outputs is only one transistor delay, as against two transistor delays in Fig. 1. The output current is I1 less one base current, which is less sensitive to the forward current gain β_F.

Experiment: Two test circuits incorporating current injection have been fabricated using the BNR HBT process [3]. Test circuit 1 is a decision circuit comprising three buffers, one master–slave flip-flop (FF) with current injection and one output cell. A die photograph is shown in Fig. 3. Test circuit 2 is an *f*/2 frequency divider comprising one FF with current injection, one buffer and one output cell. The external clock is unbuffered, allowing clock amplitude and offset to be adjusted externally. Both test circuits use a standard pad-out, with predefined positions for power, ground and low- and high-speed signals. High-speed signals are