Characteristics of Polysilicon Contacted Shallow Junction Diode Formed with a Stacked-Amorphous-Silicon Film

Shye-Lin Wu, *Member, IEEE,* Chung-Len Lee, *Senior Member, IEEE,* Tan Fu Lei, and Hue-Chen Chang

***Abstract*—A high-performance shallow junction diode formed with a stacked-amorphous-silicon (SAS) film is presented. Since the boundaries of stacked silicon layers and the poly/mono silicon interface act as a diffusion barrier for implanted dopants, the junction depth of SAS emitter contacted diode is about 500 Å shallower than that of the as-deposited polysilicon (ADP) emitter contacted diode. The fabricated SAS emitter contacted diodes exhibited a very low reverse leakage current (≤ 1 nA/cm^2 at -5 V) and a forward ideality factor $m \approx 1.001$ over 7 decades on a log scale. The reverse *I-V* characteristics were found to be nearly independent of the reverse voltage from the room temperature to 200°C, and it was also found that the leakage current was due almost completely to the diffusion current. The plots of the diode leakage current versus the perimeter to area ratio showed that the periphery generation current only contributed a small portion to the total leakage. The processing temperature for the SAS emitter contacted p$^+$-n diode can be as low as 600°C.**

I. Introduction

To use a highly doped polysilicon film as the diffusion source to form a shallow junction and the contact has been widely investigated [1]–[21]. There are many advantages in using the polysilicon film to form the shallow junction and the contact for bipolar transistors. They are 1) it can avoid the metal spiking through the shallow p-n junction [3]; 2) it significantly increases the switching speed and the packing density resulting from the self-aligned structure [4]; and 3) the polysilicon emitter transistor (PET) exhibits a higher dc current gain than conventional transistors [4]–[7].

Some theories have been proposed to explain the origin of the enhanced current gain of PET's [5]–[10]. For example, Graul *et al.* suggested that the larger current gain was attributed to the bandgap narrowing effect in the polysilicon emitter [5]. DeGraaff and deGroot proposed that the inevitable interfacial oxide between the poly/mono silicon interface in the emitter region would act as a barrier for base minority carriers to tunnel into the polysilicon emitter region [6]. Ning and Isaac proposed a two-region model to attribute the small base current to a low mobility of holes in the polysilicon [7]. Neugroschel *et al.* experimentally demonstrated that the dopant segregation at the poly/mono silicon interface played a dominant role in reducing the base current [8]. Recently, based on the impurity segregation at the poly/mono silicon interface, Ng and Yang [9] and Jalali and Yang [10] proposed a thermionic-diffusion mode, which includes a low-high-low junction that acts as a potential barrier to minority carriers to transport across the interface. The base current was thus reduced and resulted in a higher current gain. Although much research has been devoted to the studies of the physics and the metallurgical structures of the polysilicon contacted devices, the exact nature of the poly/mono silicon interface is not fully understood [4]–[15].

It is generally recognized that the as-deposited polysilicon (ADP) film has an anisotropic structure with its columnar grains perpendicular to the substrate [16]. Since the diffusivity of dopant along the grain boundaries within polysilicon are 3 to 4 orders of magnitude higher than in single-crystal silicon, dopants diffuse anisotropically and rapidly through the vertical grain boundaries, producing irregular morphologies at the polysilicon/oxide and the poly/mono silicon interfaces [16]. This will cause a non-uniform junction and an unstable electrical characteristics of the ADP device [12]. In contrast, the amorphous silicon (α-Si) is of a random structure and has no preferential grain orientation. It has no preferential path for impurity diffusion; hence a smoother α-Si/SiO$_2$ or α-Si/Si interface and a shallower junction may be obtained [16]. It has also been reported that the polysilicon film made from α-Si offers better device characteristics [13], [16]. However, recently, it has been reported that the α-Si film gives less uniform junctions and larger junction leakage currents than does the ADP film [17].

In the authors' recent paper [18], it was reported that a

Manuscript received December 21, 1992; revised April 23, 1993. This work was supported by the National Science Council of R.O.C. through Research Contract 81-0404-E009-134. The review of this paper was arranged by

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IEEE Log Number 9211105.

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high-performance polysilicon contacted n^+-p shallow junction diode formed with a stacked-amorphous-silicon (SAS) film. Since the boundaries of stacked silicon layers and the poly/mono silicon interface act as a diffusion barrier for dopants, the junction depth of SAS emitter contacted n^+-p diode is shallower than that of the ADP emitter contacted n^+-p diode. The stacked boundaries can also serve as the natural grain boundaries of grains between polysilicon layers and limit the grain growth [19]; the average grain size of the SAS film is much smaller than that of the ADP film [18], [19]. Therefore, by referencing Park *et al.* [17], a much more uniform junction can be obtained for the SAS emitter contacted diode. Moreover, due to the stacked emitter structure, implanted dopants would segregate at the stacked boundaries during the diffusion process. The segregated dopants at each interface could create potential barriers to block the minority carrier transport [9], [10], [18]. The segregated dopants are also expected to saturate the boundary dangling bonds and improve the minority-carrier lifetime [14], [20]. The base current is therefore reduced. The fabricated diode exhibited a very low reverse leakage current (≤ 5 nA/cm^2 at -100 V, and ≤ 1 nA/cm^2 at -5 V), a very high breakdown voltage (≥ 100 V), and a forward ideality factor m $\leq$ 1.05 over 7 decades on a log scale [18]. In this paper, a systematic study of the characteristics of both the SAS emitter contacted n^+-p and p^+-n diodes has been done. To make comparisons, the ADP emitter contacted diode, the as-deposited amorphous silicon (ADA) emitter contacted diode, and the stacked-polycrystalline-silicon (SPS) emitter contacted diode were also fabricated during the study.

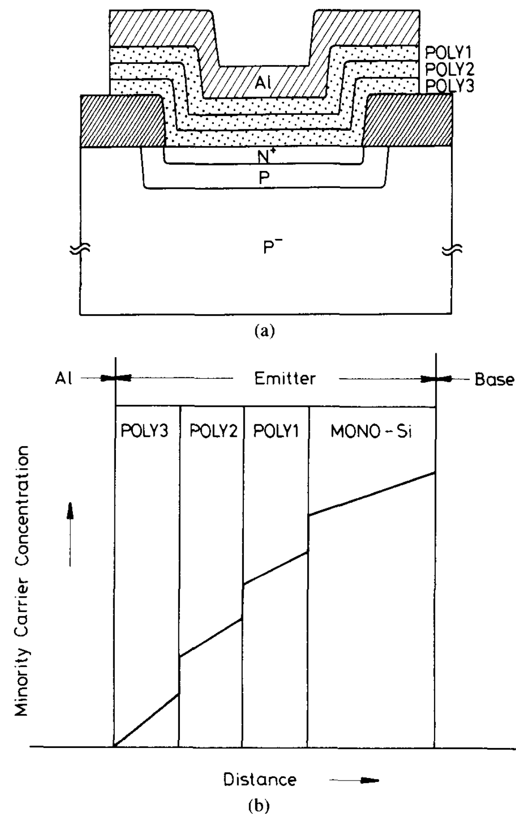


Fig. 1. (a) Cross-sectional view of the SAS emitter contacted n^+-p diode. (b) Emitter minority-carrier distribution.

II. Device Structure and Principle

The SAS emitter contacted n^+-p diode is shown in Fig. 1(a), where the stacked α-Si emitter is of three layers. The device was formed by depositing α-Si film in three consecutive steps with a low pressure chemical vapor deposition (LPCVD) system onto a p-type silicon wafer. The device was then arsenic ion implanted and annealed. During the annealing stage, the amorphous films were crystallized into polysilicon, and at the same time, arsenic atoms diffused through the polysilicon layers and into the substrate to form the n^+-p junction. Because of the stacked layers, arsenic atoms also segregated at the grain boundaries and at the interface of each α-Si layer, in addition to the poly/mono silicon interface [20], [21]. These segregated arsenic atoms produced potential barriers for injected minority carriers transport from the base into the polysilicon emitter region [9], [10], [20]. As a result, the emitter minority carrier distribution would be the one shown in Fig. 1(b) and the base injection current was reduced [10]. In Fig. 1(b), the discontinuities at each boundary are due to the segregated-dopant induced potential barrier for minority-carrier injection at each layer boundary [10].

III. Experimental Procedure

In this study, the SAS emitter contacted n^+-p diodes were fabricated on p-type, (100), 4–11.5 $\Omega \cdot$ cm wafers. The wafers were first thermally oxidized and patterned. On some of the SAS n^+-p diodes, BF_2 ion implantation was performed at 50 keV with a dose of 5×10^{13} cm^{-2} to simulate the base doping level of a bipolar transistor. Prior to the α-Si film deposition, all wafers were dipped in a HF : H_2O (1 : 50) solution to remove the surface native oxide. The α-Si films with total thickness ranging from 2000 Å to 4000 Å were then deposited in several steps on the wafers by using an LPCVD system at 550°C to form the stacked structure. The deposition pressure and deposition rate were controlled at about 140 mtorr and 20 Å/min, respectively. The thickness of each α-Si layer was about 500 Å to 1000 Å. During the stacked-layer deposition, the chamber of the LPCVD system was not interrupted. After the first α-Si layer deposition, the SiH_4 gas was removed and replaced by an N_2 gas to purge the LPCVD system for about a period of about 30 min. By using the same steps, the second and the third α-Si layers were deposited on the wafers. Since a little O_2 may be existed in the N_2 ambient, a layer boundary is formed be-

tween two adjacent α-Si layers. The arsenic implantation was performed at 120 keV with doses ranging from 8×10^{14} to 1×10^{16} cm^{-2}. To make comparisons, the ADP emitter contacted diodes were also fabricated in the same procedures except that the polysilicon film was deposited at 625°C in one step. The deposition pressure and deposition rate were about 200 mtorr and 100 Å/min, respectively.

The SAS emitter contacted p^+-n diodes were fabricated on n-type, (100), 1.97–1.99 $\Omega \cdot$ cm wafers. The wafers were implanted with BF_2 at 120 keV with a dose of 1×10^{16} cm^{-2}. For comparisons, the ADP, ADA, and SPS emitter contacted p^+-n diodes were also fabricated. After implantation, various annealing conditions were performed. Then the surface oxide was removed and a 1-μm-thick aluminum film was evaporated and patterned into circular dots to provide the contact to diodes. Finally, all devices were sintered in an N_2 ambient for 30 min at 400°C.

The *I–V* characteristics were measured by using an HP4145B semiconductor parameter analyzer. The temperature dependence of the diode current was measured from room temperature to approximately 200°C on a thermal chuck to study the mechanisms of the junction leakage. The impurity profiles were analyzed with a VG Ionex SIMS (secondary ion mass spectrometry) tool using an O_2^+ beam for boron and fluorine and a C_s^+ beam for boron, arsenic, and oxygen.

IV. Results and Discussions

A. SIMS Profiles of Dopant Segregation

In the authors' recent papers [18], [19], it was found that the boundaries between the stacked α-Si layers provided not only a segregation sink but also served as a barrier to retard the diffusion of implanted arsenic atoms; multiarsenic segregation peaks could be observed in the SAS emitter contacted n^+-p diode, while only one peak could be observed for the ADP emitter contacted n^+-p diode. Moreover, the junction depth of the SAS emitter contacted diode was shallower than that of the ADP emitter contacted diode. Along with arsenic, the fluorine atoms also segregated at each interface between various layers. These atoms are expected to saturate the boundary dangling bonds and improve the boundary surface states and the minority carrier lifetime [14], [20]. In this study, the dopant profiles of the SAS, SPS, ADA, and ADP emitter contact p^+-n diodes will be analyzed as follows.

Figure 2(a) shows the SIMS profiles of boron of the SAS (solid line), the SPS (dashed line), and the ADP (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 35 min, respectively. The boron profile was analyzed by Cs^+ primary beam. Figure 2(b) shows the SIMS profiles of boron of the SAS (solid line), the ADP (dashed line), and the ADA (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 25 min, respectively. The boron profile was analyzed by an O_2^+ primary beam. Three boron segregation peaks could be observed in both the SAS and SPS diodes, while only one peak could be observed for the ADP and ADA diodes. The junction depth of the SAS diodes are about 500 Å shallower than that of the ADA and ADP diodes, but only slightly shallower than that of the SPS diode. This suggests that the stacked boundaries for the SAS and SPS

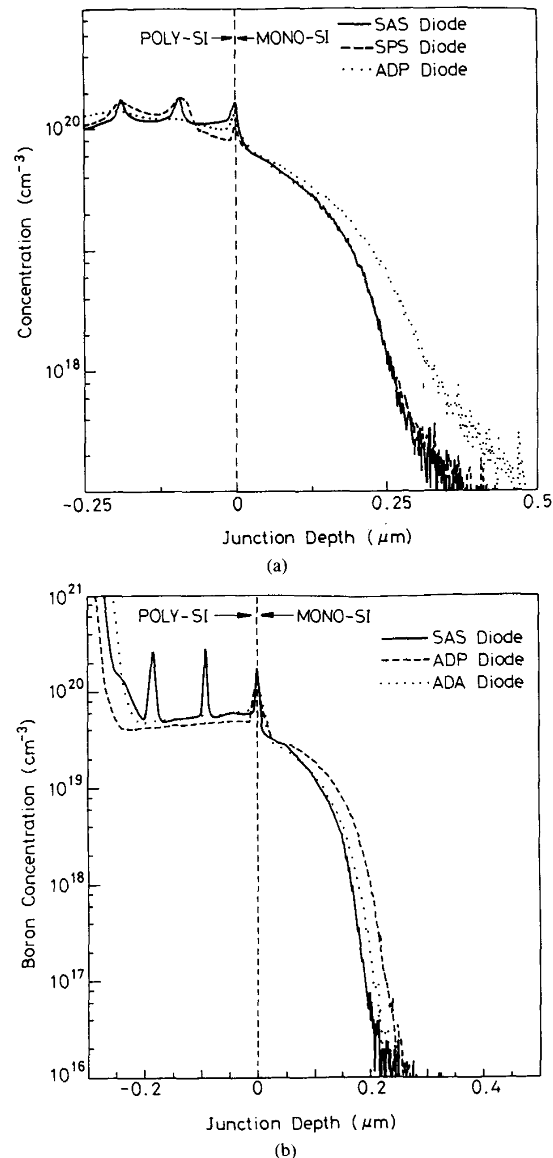


Fig. 2. (a) SIMS profiles of boron of the SAS (solid line), the SPS (dashed line), and the ADP (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 35 min, respectively. The boron profiles were analyzed by an Cs^+ primary beam. (b) SIMS profiles of boron of the SAS (solid line), the ADP (dashed line), and ADA (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 25 min, respectively. The boron profiles were analyzed by an O_2^+ primary beam.

diodes provided not only a segregation sink but also served as a diffusion barrier of boron atoms.

B. I–V Characteristics

Figure 3(a) shows the typical forward (solid line) and reverse (dashed line) *I–V* characteristics of the SAS emitter contacted p^+-n diode. Although the dopant was only driven in at 600°C for 3 h, the diode exhibits an ideal forward characteristics with ideality factor $m \leq 1.01$ over 7 decades on a log scale and a very low reverse current of approximately 0.8 nA/cm^2 at -5 V. Figure 3(b) shows the plots of the reverse leakage current density (*JR*) at -5 V and the forward ideality factor *m* versus the annealing time for the SAS emitter contacted p^+-n diodes annealed at 600°C. It is seen that almost all diodes have a very low leakage current ($JR \leq 1$ nA/cm^2) and a nearly ideal forward characteristics ($m \leq 1.02$).

Figure 4(a) shows the forward and reverse *I–V* characteristics of the SAS (solid line), ADP (dashed line), and SPS (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 35 min in an N_2 ambient. Although all diodes exhibit nearly ideal forward characteristics ($m \leq 1.005$), the ADP diode has the largest forward current. This implies that the current gain of the pnp PET's formed with the SAS and SPS films is larger than those formed with an ADP film. Moreover, both the SAS and SPS emitter contacted p^+-n diodes have a very low reverse leakage current (≤ 0.5 nA/cm^2 at -5V), while that of the ADP emitter contacted p^+-n diode is about 5 nA/cm^2. Figure 4(b) shows the plots of the reverse leakage current at -5 V versus the annealing temperature of the SAS, ADP, and ADA emitter contacted p^+-n diodes respectively. It is seen that the leakage current of the SAS emitter contacted p^+-n diode is less than that of the ADP and ADA emitter contacted p^+-n diodes, especially for the lower temperature annealing diodes. The reason diodes formed with SAS and SPS films exhibited a superior performance than those formed with ADP and ADA films may be due to the multidopant segregation peaks resulting in potential barriers to block minority carriers transport [9], [10] and to the segregated dopants saturating the dangling bonds and enhancing the minority-carrier lifetime [14], [20].

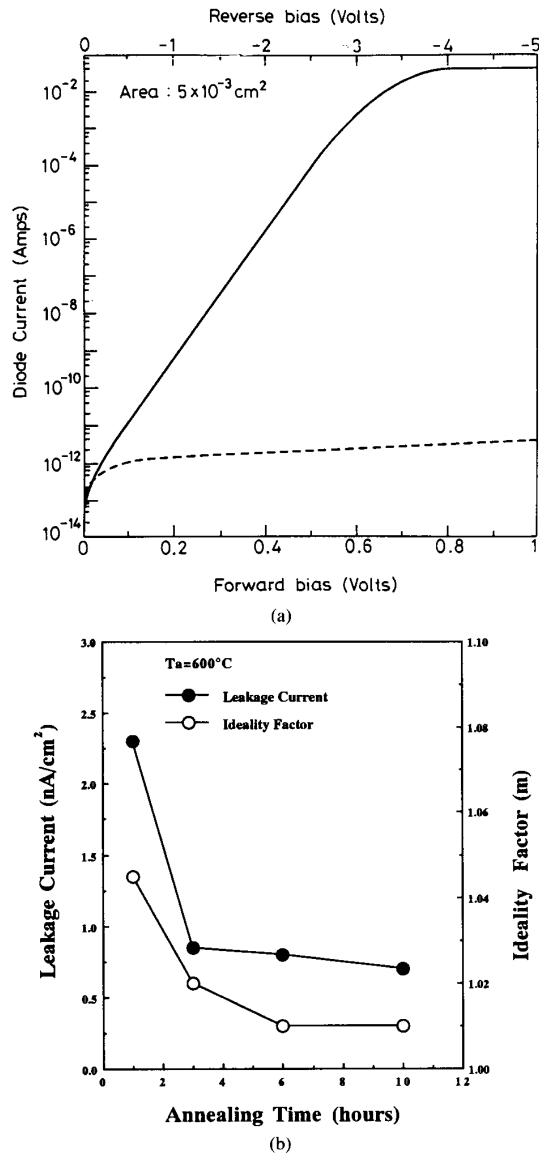
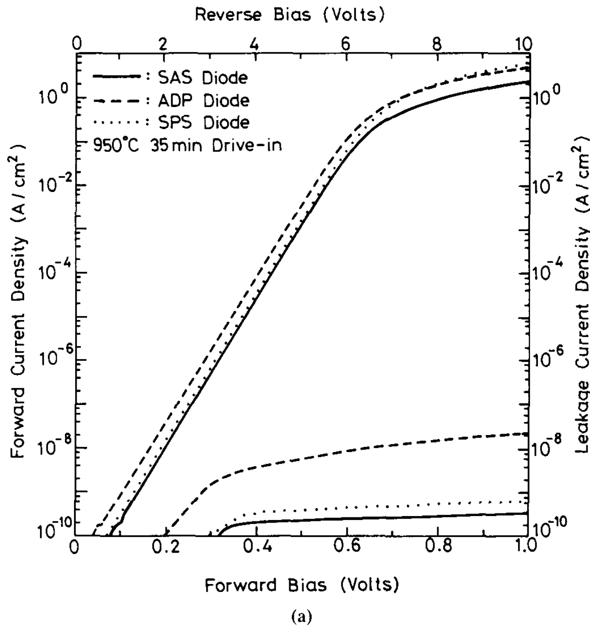


Fig. 3. (a) Typical forward (solid line) and reverse (dashed line) *I–V* characteristics of the SAS emitter contacted p^+-n diode. The dopant drive-in at 600°C for 3 h. (b) Plots of the reverse leakage current density (*JR*) at -5 V and the forward ideality factor (*m*) versus the annealing time for the SAS emitter contacted p^+-n diodes annealed at 600°C.

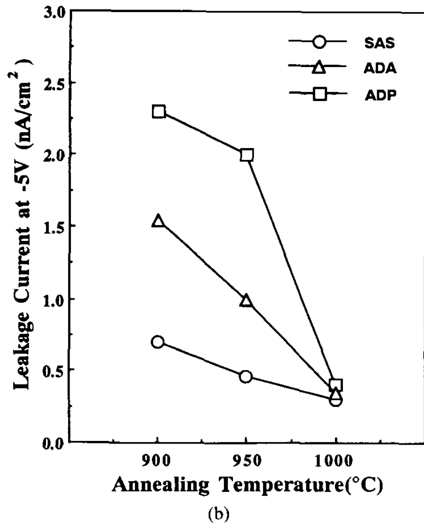
C. Temperature Dependence of I–V Characteristics

As mentioned previously, it has been proposed that the current of a PET may be mainly limited by the poly/mono silicon interface barrier and that the base current may be a combination of a thermionic and a drift-diffusion current [9], [10]. In this study, the temperature dependence of the diode current was measured from room temperature to approximately 220°C on a thermal chuck to determine the mechanism of the junction leakage. Figure 5(a) shows the Arrhenius plots of $\log_e (J_s/A^*T^2)$ versus $1/T$ for the SAS and ADP emitter contacted p^+-n diodes have shown in Fig. 4(a), where J_s is the saturation current density of diodes and A^* is the Richardson constant [21]. The barrier heights for minority carrier transport into polysilicon derived from these plots are 1.27 and 1.20 eV for the SAS and ADP emitter contacted p^+-n diodes, respectively. These values are comparable to those reported in [9], but the SAS diodes have a little higher value than the ADP diodes. This higher value may be due to the additional dopant segregation peaks at the poly/poly silicon interfaces. With the larger barrier height, it can be suggested that a PET formed by using the SAS film as a diffusion source may have a higher current gain.

From the temperature dependence of the reverse *I–V* characteristics, the mechanism of the junction leakage

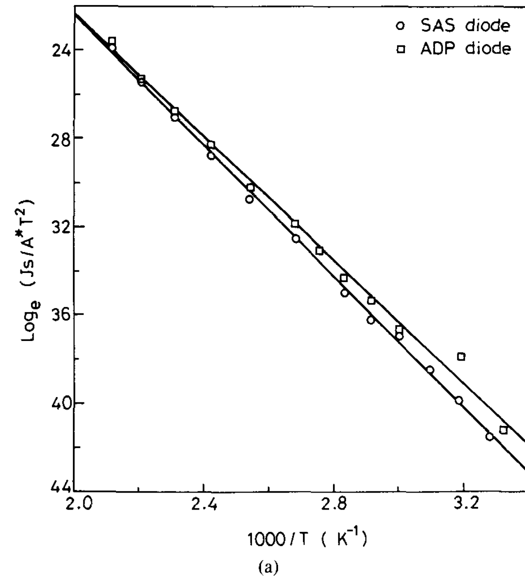


(a)

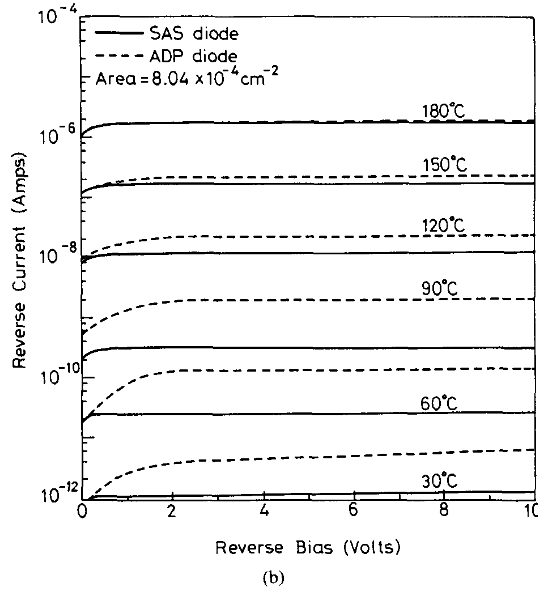


(b)

Fig. 4. (a) Forward and reverse *I-V* characteristics of the SAS (solid line), the SPS (dashed line), and the ADP (dotted line) emitter contacted p^+-n diodes annealed at 950°C for 35 min in an N_2 ambient, respectively. The SIMS profiles were shown in Fig. 2(a). (b) Plots of the reverse leakage current versus the annealing temperature of the SAS, ADP, and ADA emitter contacted p^+-n diodes, respectively.



(a)



(b)

Fig. 5. (a) Arrhenius plots of $\log_e (J_s/A^*T^2)$ versus $1/T$ for the SAS and ADP emitter contacted p^+-n diodes, respectively. (b) Typical temperature dependence of the reverse *I-V* characteristics of the SAS (solid line) and the ADP (dashed line) emitter contacted n^+-p diodes, respectively.

current may be determined [21], [22]. Figure 5(b) shows the typical temperature dependence of the reverse *I-V* characteristics of the SAS (solid line) and ADP (dashed line) emitter contacted n^+-p diodes [18], respectively. It can be seen that the reverse *I-V* characteristics of the SAS emitter contacted diode were nearly independent of the reverse voltage from the room temperature to 200°C. This implies that the junction region of the SAS emitter contacted diode is nearly defect free. The curves for the ADP emitter contacted diode, however, were somewhat dependent on the reverse-biasing voltage, especially at the lower temperature. Also, at the lower temperature ($T \leq 100$°C), the junction leakage currents of the ADP diode were much larger than those of the SAS diode. This indicates that, for the ADP emitter contacted diode, the defect-induced generation current is more significant than that of the SAS emitter contacted diode. The activation energies $E_{g(\mathrm{eff})}$ deduced from the temperature dependence of the reverse *I-V* characteristics were 1.13 eV and 0.937 eV for the SAS and ADP emitter contacted n^+-p diodes [18], respectively. This implies that the reverse leakage current of the SAS emitter contacted diode was due nearly com-

pletely to the diffusion current outside the junction depletion region, while for the ADP emitter contacted diode the generation current in the depletion region and/or at the junction peripheral region plays somewhat an important role in contributing the reverse current.

The above can also be seen by plotting the reverse leakage current density of n^+-p diodes of various areas measured at -80 V versus the perimeter to area ratio (P/A), as shown in Fig. 6. The reverse leakage current density JR is composed of two components, that is, the area component JRa and the periphery component JRp [23]:

$$JR = JRa + (P/A)JRp$$

where A is the area of the diode and P is the perimeter length of the diode. In Fig. 6, for the SAS emitter contacted diode, the slope for the plotted curve is much smaller than that of the ADP emitter contacted diode. That is, for the SAS emitter contacted diode, the periphery generation current only contributed a smaller portion to the total leakage. This suggests that for the SAS emitter contacted diode, the edge defects induced leakage current may be neglected.

There are three possible reasons to explain the superior performance of both the SAS p^+-n and n^+-p diodes. 1) The α-Si film is of a random structure and has no preferential grain orientation [16]. It has no preferential path for impurity diffusion; hence, smoother α-Si/SiO_2 or α-Si/Si interface and a shallower emitter-base junction may be obtained [16]. Moreover, the transmission electron microscopy (TEM) micrographs of the surface and the cross section [18], [19] show that the grain size of the SAS diode is much smaller than that of the ADP diode. By referencing Park *et al.* [17], a more uniform junction may be obtained. 2) As mentioned in Section II, the multisegregation peaks of arsenic, oxygen, and fluorine atoms at the poly/silicon and the stacked polysilicon interfaces would act as the multipotential barriers to the minority-carrier transport [8]–[10]. Also, the segregated arsenic, oxygen, and fluorine atoms would saturate the dangling bonds within the interface to reduce the surface recombination velocity [14], [20]. This consequently reduces the base current. 3) The conventional and high resolution TEM shows that the poly/mono silicon interface of the SAS emitter contacted diode is more liable to be broken up than that of the ADP emitter contacted diode [19], because the oxygen atoms of the interfacial oxides are liable to migrate to the grain boundaries [8]. In this study, the interfacial region of the SAS emitter contacted diode was nearly fully broken up and the maximum thickness of the epitaxial regrowth layer was about 260 Å [18], [19]. This would cause an extended emitter region and reduce the gradient of the minority-carrier distribution in the emitter [7]. This also reduces the base current. Hence it is believed that PET's formed by using the SAS film as a diffusion source would have a better performance than those formed from the ADP film.

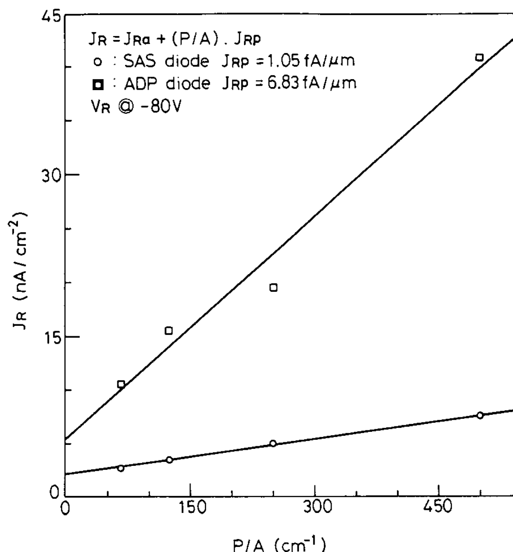


Fig. 6. Plots of the reverse leakage current density measured at -80 V of the SAS and ADP emitter contacted n^+-p diodes versus the perimeter to area ratio, respectively.

IV. Conclusion

In this paper, we have presented a high-performance shallow junction diode formed by using an SAS film as the dopant diffusion source. The processing temperature for the SAS emitter contacted p^+-n diode can be as low as 600°C. Since the boundaries of stacked silicon layers as well as the poly/mono silicon interface act as a diffusion barrier for implanted dopants, the junction depth of SAS emitter contacted diode is about 500 Å shallower than that of the ADP emitter contacted diode. The SAS emitter contacted p^+-n junction as shallow as about 0.06 μm can be obtained. Due to the stacked emitter structure, the implanted dopants would segregate at the stacked boundaries and at the poly/mono silicon interface during the annealing process and subsequently cause multipotential barriers to block the minority-carrier transport. Moreover, the TEM micrographs revealed that the interfacial oxide layer was nearly fully broken up and the maximum thickness of the epitaxial film aligned to the silicon substrate was about 260 Å [18], [19]. This would cause an extended emitter region and reduce the gradient of the minority-carrier distribution in the emitter [7]. The stacked boundaries can also serve as the natural grain boundaries of grains between polysilicon layers and limit the grain growth; the average grain size of the SAS film is much smaller than that of the ADP film [19]. By referencing Park *et al.* [17], a much more uniform junction can be obtained for the SAS emitter contacted diode. Thus the base current was reduced.

Both the SAS emitter contacted p^+-n and n^+-p diodes exhibited a very low reverse leakage current (≤ 1 nA/cm^2 at -5 V), a very high breakdown voltage (≈ 100 V) and

a forward ideality factor $m \approx 1.001$ over 7 decades on a log scale. The reverse-biased I–V characteristics of the SAS emitter contacted diode were found to be nearly independent of the reverse voltage from the room temperature to 200°C, and the derived activation energy was 1.13 eV. This indicated that the diode leakage current was due mostly to the diffusion current. The plots of the diode leakage current versus the perimeter-to-area ratio showed that the periphery generation current only contributed a small portion to the total leakage. All of the above suggest that devices formed with the SAS structure provide a superior performance in the VLSI applications than does the ADP structure.

Acknowledgments

The authors are grateful to Prof. S. M. Sze and Prof. L. J. Chen for helpful discussions. The authors would like to thank D. A. Tasi for assistance in some samples preparation, C. C. Wang and S. Y. Wu for ion implantation, and T. L. Lee and C. F. Chen for HRTEM micrographs.

References

[1] S. M. Sze, Ed., *High-Speed Semiconductor Devices.* New York: Wiley, 1990, ch. 3.
[2] E. Kinsbron and W. T. Lynch, "Source and drain junction by oxidizing arsenic doped polysilicon," in *IEDM Tech. Dig.*, 1983, p. 674.
[3] D. Pramanik and A. N. Saxena, "VLSI metallization using aluminum and its alloys. Part II," *Solid-State Tech.*, pp. 131–138, 1983.
[4] A. K. Kapoor and D. J. Roulston, Ed., *Polysilicon Emitter Bipolar Transistors.* New York: IEEE Press, 1989.
[5] J. Graul, A. Glasl, and H. Murrmann, "High performance transistors with arsenic-implanted polysil emitters," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 491–496, 1976.
[6] H. C. deGraaf and J. G. deGroot, "The SIS tunnel emitter: A theory for emitters with thin interface layers," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 1771–1776, 1979.
[7] T. H. Ning and R. D. Isaac, "Effect of emitter contact on current gain of silicon bipolar devices," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 2051–2055, 1980.
[8] A. Neugroschel, M. Arienzo, and C. Y. Wong, "Experimental study of the minority-carrier transport at the polysilicon-monosilicon interface," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 807–816, 1985.
[9] C. C. Ng and E. S. Yang, "A thermionic-diffusion model of polysilicon emitter," in *IEDM Tech. Dig.*, 1986, pp. 32–35.
[10] B. Jalali and E. S. Yang, "A general model for minority carrier transport in polysilicon emitters," *Solid-State Electron*, vol. 32, pp. 323–327, 1989.
[11] P. Ashburn and B. Soerowirdjo, "Comparison of experimental and theoretical results on polysilicon emitter bipolars," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 853–860, 1984.
[12] G. L. Patton, J. C. Bravman, and J. D. Plummer, "Physics, technology, and modeling of polysilicon emitter contacts for VLSI bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1754–1768, 1986.
[13] P. A. Potyraj, D. L. Chen, M. K. Hatalis, and D. W. Greve, "Interfacial oxide, grain size, and hydrogen passivation effects on polysilicon emitter transistors," *IEEE Trans. Electron Devices*, vol. ED-35, pp. 1334–1343, 1988.
[14] C. Y. Wong, C. R. M. Grovenor, P. E. Batson, and D. A. Smith, "Arsenic segregation to silicon/silicon oxide interface," *J. Appl. Phys.*, vol. 58, pp. 2779–2782, 1985.
[15] J. M. C. Stork, M. Arienzo, and C. Y. Wong, "Correlation between the diffusive and electrical barrier properties of the interface in polysilicon contacted n^+-p junctions," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1766–1770, 1985.
[16] T. Kamins, *Polycrystalline Silicon for Integrated Circuit Applications.* Boston: Kluwer Academic, 1988.
[17] K. Park, S. Batra, and S. Banerjee, "Analysis of lateral uniformity of ultrashallow junction in polycrystalline silicon-on-single crystalline systems," *Appl. Phys. Lett.*, vol. 59, pp. 709–711, 1991.
[18] S. L. Wu, C. L. Lee, and T. F. Lei, "High performance polysilicon contacted shallow junctions formed by stacked-amorphous-silicon films," *IEEE Electron Device Lett.*, vol. EDL-13, pp. 23–25, 1992.
[19] S. L. Wu, C. L. Lee, and T. F. Lei, "Investigation on the interface of the polycrystalline silicon contacted diode formed with a stacked amorphous silicon film," *J. Electron. Materials*, vol. 21, pp. 811–816, 1992.
[20] Y. Nishioka, K. Ohyu, Y. Ohji, N. Natsuaki, K. Mukai, and T. P. Ma, "The effect of fluorine implantation on the interface radiation hardness of Si-gate metal-semiconductor transistors," *J. Appl. Phys.*, vol. 66, pp. 3909–3912, 1989.
[21] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981, ch. 2.
[22] R. Liu, D. S. Williams, and W. T. Lynch, "A study of the leakage mechanisms of silicided n^+/p junctions," *J. App. Phys.*, vol. 63, pp. 1990–1999, 1988.
[23] H. M. Rein, "A simple method for separation of the internal and external (peripheral) currents of bipolar transistors," *Solid-State Electron*, vol. 27, pp. 625–631, 1984.

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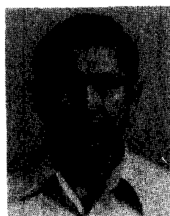

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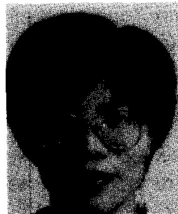
From 1970 to 1972, he was with the Fine Products Microelectronics Corporation, Taiwan, as an Engineer working on the fabrication of small-signal transistors. From 1980 to 1982, he was the Plant Manager of Photronic Corporation, Taiwan (now Silitek Corporation). In 1983, he joined the faculty at National Chiao Tung University as an Associate Professor in the Department of Electronics Engineering and the Institute of Electronics. From 1984 to 1986, he was the Director of the Semiconductor Research Center. Presently, he is a Professor of the Department and the Associate Director of National Nano Device Laboratory. His research interests are semiconductor devices and optoelectronics.



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