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Investigation of Cu/TaN Metal Gate for Metal-Oxide-Silicon Devices

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This work investigates the work function modulation of TaN_x films and the thermal stability of Cu/TaN_x stack as a gate electrode for metal-oxide-silicon devices. The N/Ta ratio was varied in the range of 0.30-0.65 by using reactive-sputter deposition with various Ar/N_2 mass flow ratios. The TaN_x films are almost amorphous and are thermally stable up to 800°C. However, the formation of Ta_3N_5 phase in a film with a high N/Ta ratio or annealed at high temperature increases the resistivity. The work function of TaN_x is about 4.31-4.38 eV and the modulation is less than 70 mV. Such a short range modulation of the work function implies that TaN_x is only suitable to be a gate electrode of surface channel n-channel metal oxide semiconductor field effect transistors (NMOSFETs). The mean value of the flatband voltage decreases and the deviation of the flatland voltage increases with the increase of the annealing temperature. Although phase change, grain growth, and Cu contamination contribute to the instability at high temperature, thermal stress-induced oxide charges dominate this decrease and deviation of the flatband voltage at temperature below 500°C. According to the material and electrical analysis, the Cu/TaN_x stack gate electrode can be used for NMOSFETs only, and the maximum process temperature following gate electrode deposition should be lower than 500°C.
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As conventional complementary metal oxide semiconductor (CMOS) devices are scaled down to improve performance, gate engineering becomes a crucial issue. It was found that the conventional gate material, poly-silicon, suffered from gate depletion, high gate resistance, and boron penetration into the channel region in sub-100 nm CMOS technology node.[1-5] Poly-Si gate depletion increases the equivalent gate dielectric thickness by about 3 Å and degrades channel current drive capability.[1-3] High gate resistance increases the resistance/capacitance (RC) time delay to degrade high frequency performance. Salicide technology can reduce the gate resistance but it is difficult to maintain a proper aspect ratio for gate stack in scaled devices.[4] Boron penetration in p-channel metal oxide semiconductor field effect transistor (PMOSFET) reduces the ability of threshold voltage control and gate oxide reliability.[1,5] High dielectric constant (high *k*) materials are expected to replace SiO_2 for scaling gate dielectric thickness below 1.5 nm where direct tunneling current through SiO_2 may be too high to be acceptable.[4] Unfortunately, poly-Si is incompatible with most high *k* materials due to chemical reaction or interface layer formation.[6,7] It has been demonstrated that metal gate devices are free from gate depletion, high resistance, and boron penetration. Therefore, there is an immense interest in metals to be a replacement in gate electrodes.

To select metal gate material properly, several issues must be considered to satisfy the manufacturability and performance. The typical thermal budget of front-end process usually causes thermal instability of metal gate devices. Therefore, low temperature or low thermal budget processes must be developed to prevent the metal gate from experiencing high temperature processes.[8-11] To simplify the process and to achieve high performance, the metal gate electrode should have low resistivity, suitable work function (Φ_m), high thermodynamic stability, and good chemical durability under wet chemical processing. From these points of view, refractory metals such as W, Mo, Ta, and Ti are more attractive candidates. Since the work function of some refractory metal nitrides can be modulated with the nitrogen atom content, several investigations have been carried out in this field.[12-14] However, the nitrogen content also increases the resistivity of the metal. According to the ITRS roadmap of 2001, the effective resistivity of the gate electrode must be lower than 32 $\mu\Omega$ cm.[15] This implies that several metal nitrides are not suitable to be used as a single layer gate electrode. Consequently, the gate electrode might be formed with stack structure that consists of a low resistivity metal and refractory metal nitride layers.[12,16,17] Wherever it is possible, the low resistivity layer serves as the major conduction material and metal nitride layer serves as the threshold voltage control material.

Recently, the widely accepted barrier metal, TaN_x, was reported as the gate electrode of fully depleted silicon-on-insulator devices and showed that its work function is closer to the midgap of silicon than that of β-tantalum.[17] The Cu interconnect has become an alternative to conventional Al interconnect, because of its low resistivity, low via resistance, and high electron-migration resistance.[18] Investigating the feasibility of using Cu/TaN_x at the front-end-of-line (FEOL), as the gate electrode, becomes natural.[16] The use of Cu/TaN_x at both the FEOL and back-end-of-line (BEOL) can simplify the management of production line and reduce the cost-of-ownership because the equipment for BEOL can share with FEOL. Therefore, Cu/TaN_x gate is one of the desirable gate structures. In

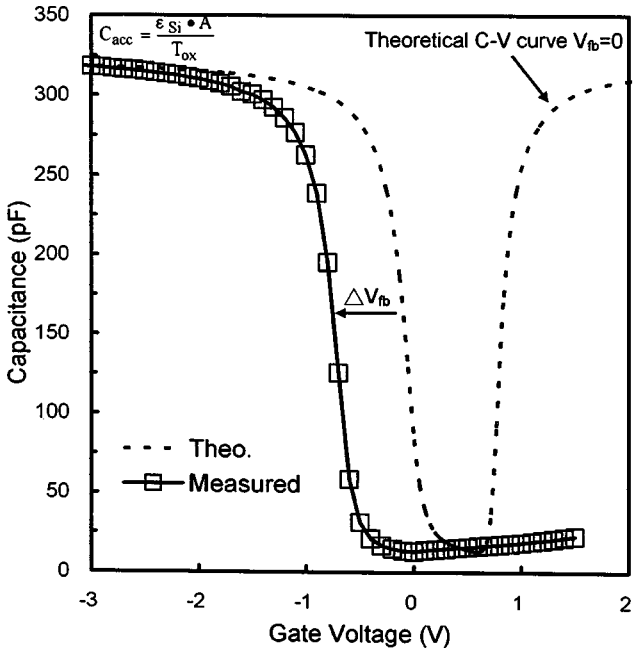

Figure 1. Example of the measured and the well-fitted theoretical capacitance/voltage curves for the extraction of corrected flatband voltage.

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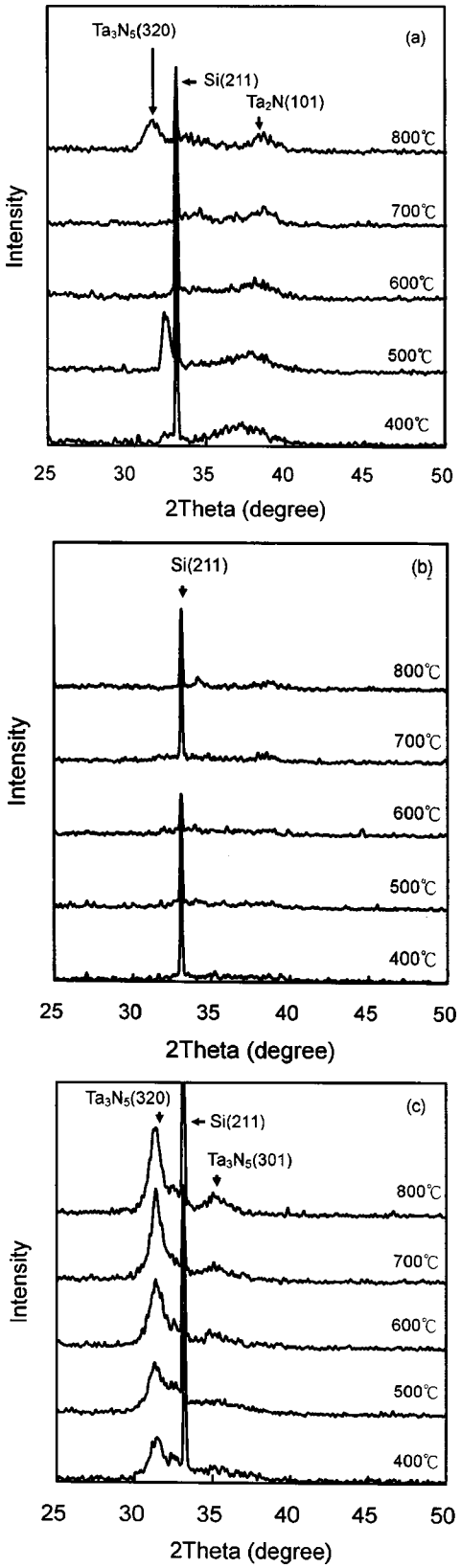

Figure 2. Wide angle XRD spectrums of (a) TaN-1, (b) TaN-2, and (c) TaN-3 films after annealing at various temperatures.

this work, the work function modulation of TaN_x film and the thermal stability of Cu/TaN_x MOS devices were investigated. The criteria and the optimum thermal process conditions for Cu/TaN_x gate MOS devices were proposed.

Experimental

Simple metal oxide semiconductor (MOS) capacitors were fabricated with a single damascene process on p-type (100)-oriented Si wafers. After cleaning, a 500 nm thick thermal oxide was thermally grown and a 1 μm thick oxide was deposited in a high-density-plasma chemical vapor deposition (HDPCVD) system. A conventional photo-lithography process was then used to define an active region with an area of 300 × 300 μm. The oxide in the active region was etched by a two-step (dry by wet) process to prevent Si surface from being damaged. Following preoxidation cleaning, a dry oxide, 10 nm thick, was thermally grown at 900°C as the gate dielectric. The purpose of using such a thick gate oxide is to isolate the gate electrode issues from the ultrathin oxide issues. TaN_x films with various Ta/N ratios were reactively sputtered in a physical vapor deposition (PVD) system to a thickness of 50 nm, with various gas-flow ratios of Ar to N_2. Before deposition, the process chamber was pumped down to 10^{-7} Torr. During deposition, neither bias nor heating was applied to the wafers, and the chamber pressure was kept at 10^{-4} Torr. It is known that the PVD process may introduce physical bombardment damage and radiation damage to the substrate.[19,20] The physical bombardment damage can be reduced with lower deposition power and zero substrate bias. Therefore, the dc power and radio frequency (rf) power were set to 15 kW and 350 W, respectively. Radiation-induced oxide charges can be neutralized after a postdeposition annealing at 400°C. The Ar/N_2 gas flow ratio was set to 60/12, 60/20, and 60/28 for TaN-1, TaN-2, and TaN-3 films, respectively. A 200 nm thick Cu film was continuously deposited on TaN_x films as a seed layer in another chamber of the same PVD system, without exposing to air. Then a 1 μm thick electrochemically deposited copper film was deposited. Finally, the chemical mechanical polishing separated MOS capacitors and a 30 nm thick silicon nitride film were deposited to passivate the Cu surface. The completed structure is Si_3N_4 (30 nm)/Cu (500 nm)/TaN_x (50 nm)/SiO_2 (10 nm)/Si substrate. The thickness of dielectric layers were measured with the ellipsometry method and the thickness of metal layers were inspected with cross-sectional scanning electron microscopy (SEM).

The element ratios of TaN_x films were determined with the Rutherford backscattering spectroscopy (RBS) analysis. The phase transformation after annealing at different temperatures was identified with Cu Kα radiation wild angle X-ray diffraction (XRD) spectrum. A transmission electron microscope (TEM) was used to determine grain size as well as phase formation. On the other hand, the sheet resistance (R_s) of blanket TaN_x films was measured with a four-point probes system to monitor the thermal stability of various films. Secondary ion mass spectroscopy (SIMS) depth profiling technique was used to elucidate the distribution of Cu atoms in the Cu/TaN_x gate MOS capacitor.

In the electrical analysis, high frequency capacitance-voltage (C-V) characteristic was measured at a frequency of 100 kHz. Low frequency (C-V) characteristic was measured with a ramp voltage method.[21] The oxide thickness (T_{ox}) was calculated from the capacitance at strong accumulation mode ($C_{acc} = \varepsilon_{ox}A/T_{ox}$). The substrate concentration can be obtained by fitting the measured C-V curve with the theoretical C-V curve at the depletion mode without concerning the interface state density (D_{it}). Because of the relatively thick gate oxide, classical MOS theory can be applied and the equations used to generate theoretical C-V curve can be found in any general textbook.[22]

By shifting the measured C-V curve to coincide with the theoretical curve, the flatband voltage can be determined without the interference from the variation of gate oxide thickness and substrate concentration. Figure 1 shows an example of the measured 400°C annealed Cu/TaN-2 sample and the well-fitted C-V curves. The perfect coincidence between the measured and theoretical C-V curves confirms that no PVD damages induced charges remain after 400°C annealing. After subtracting the work function of Si substrate, we obtain the corrected flatband voltage ($V_{FB,c}$) which is equal to

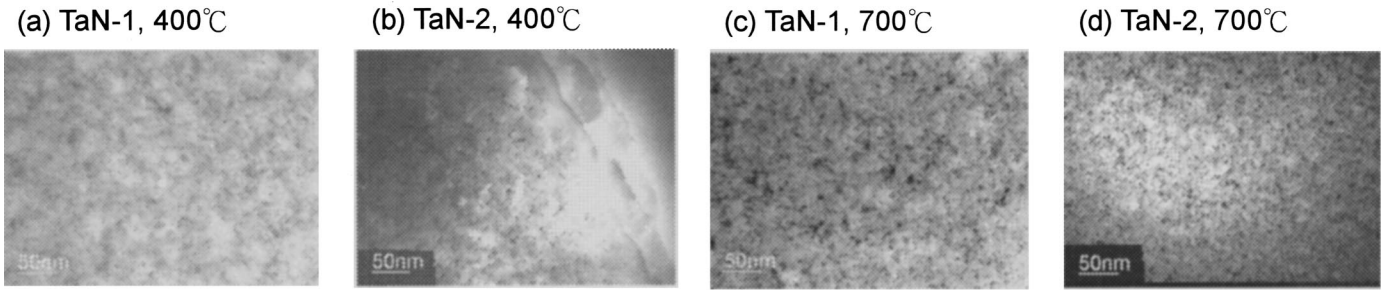

Figure 3. Plane view TEM micrographs of (a) TaN-1 film annealed at 400°C, (b) TaN-1 film annealed at 700°C, (c) TaN-2 film annealed at 400°C, and (d) TaN-2 film annealed at 700°C.

$\Phi_m - Q_{eff}/C_{ox}$, where Φ_m is the work function of gate electrode and Q_{eff} is the effective oxide charges. In the case of thin oxide or low oxide charge, the $V_{FB,c}$ becomes very close to Φ_m.

The corrected flatband voltage of TaN_x after annealing at 400 and 500°C was extracted according to the above procedure. However, as the D_{it} can not be ignored, the fitting error becomes large. In this case, the flatband voltage was estimated from the flatband capacitance.[22] Finally, the interface state density (D_{it}) at the midgap was measured with the high-low frequency method.[23]

Result and Discussion

Thermal stability of TaN_x films.—The N/Ta ratios of TaN_x films determined with RBS analysis are 0.3, 0.5, and 0.65 for TaN-1, TaN-2, and TaN-3 films, respectively. The phases of TaN_x are quite thermally stable. Figures 2a-c show the wide angle XRD spectra of TaN-1, TaN-2, and TaN-3 films after annealing at various temperatures. For the TaN-1 film, an extremely weak $Ta_2N(101)$ signal was detected after annealing at all temperatures. No significant phase change was observed with the increase of annealing temperature except that a weak Ta_3N_5 signal appeared after 800°C annealing. The small peak at 32.5° of the 500°C annealed TaN-1 film cannot be found in the data sheets of Si Ta, and TaN_x. It might be attributed to exterior particles and is hard to be identified from the single peak.

No XRD signal was detected for the TaN-2 film after annealing at different temperatures. For TaN-3 film, the $Ta_3N_5(320)$ phase is observed after 400°C annealing and the signal intensity increases with the increase in the annealing temperature. Because the signal intensity of XRD is relatively weak, grain size and phases are identified with plane view inspection and diffraction pattern of TEM, respectively. Figure 3 shows the plane view TEM micrographs of TaN-1 and TaN-2 films after annealing at 400 and 700°C. Since there is no apparent grain boundary but only some microcrystals, the films are almost amorphous. Despite 700°C annealing treatment, the grain is small and the grain sizes are in the nanometer range. It is sure that TaN_x film is dense and has no serious grain growth, but some microcrystals are precipitated. The transmitted electron diffraction patterns identify the phases of TaN-1 and TaN-2 more precisely than those identified with XRD. As shown in Fig. 4, Ta_2N and TaN phases were observed for TaN-1 and TaN-2 films, respectively, after annealing at 700°C.

The sheet resistance of TaN_x films was also measured to understand the effect of phase transformation. The resistivities of the as-deposited TaN-1, TaN-2, and TaN-3 films were 463, 480, and 1290 $\mu\Omega$ cm, respectively. Figure 5 shows the variation of sheet resistance of the three kinds of TaN_x films *vs.* annealing temperature. These values were normalized to the sheet resistance of the corresponding films annealed at 400°C. A slight decrease of sheet resistance is observed in the TaN-1 and TaN-2 films upon increasing the annealing temperature form 400 to 700°C. Referring to the TEM pictures in Fig. 3, the decrease of sheet resistance is attributed to the slight grain growth with the increase of annealing temperature. According to Radhakrishnan *et al.*, the Ta_3N_5 phase has a very high resistivity.[24] Thus, the sheet resistance of TaN-1 film increased suddenly at 800°C which can be attributed to the formation of Ta_3N_5 phase, as identified with the XRD spectra. Unlike TaN-1 and TaN-2 films, the sheet resistance of TaN-3 films increases with the annealing temperature. The XRD spectra reveal that the increase is due to the growth of Ta_3N_5 phase after high temperature annealing.

Flatband voltage variation of Cu/TaN_x MOS capacitor.—Figure 6 shows the corrected flatband voltage ($V_{FB,c}$) of Cu/TaN-1, Cu/TaN-2, and Cu/TaN-3 samples *vs.* the annealing temperature. All the $V_{FB,c}$ difference of Cu/TaN_x samples is less than 70 mV below or at 600°C. This implies that the modulation of work function of TaN_x film with the usage of various N/Ta ratios is very limited. In other words, the work function of TaN_x film is quite stable against variation induced by process disturbance. According to the ITRS road-

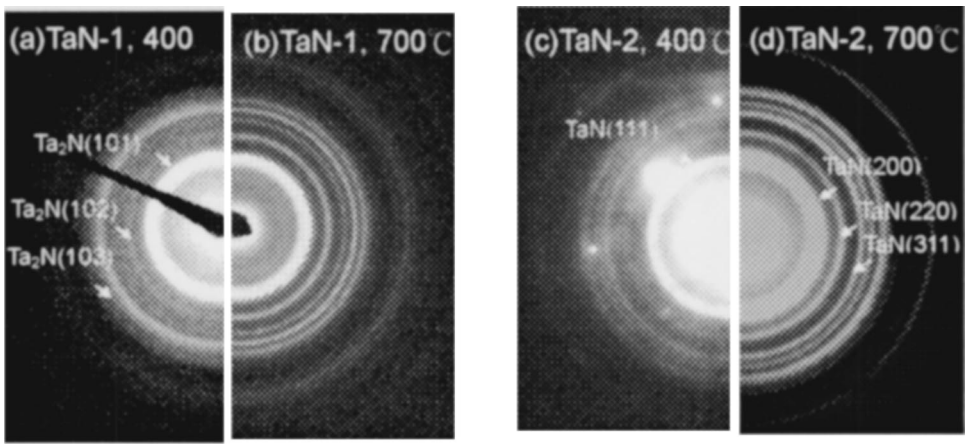

Figure 4. Diffraction patterns of (a) TaN-1 film annealed at 400°C, (b) TaN-1 film annealed at 700°C, (c) TaN-2 film annealed at 400°C, and (d) TaN-2 film annealed at 700°C.

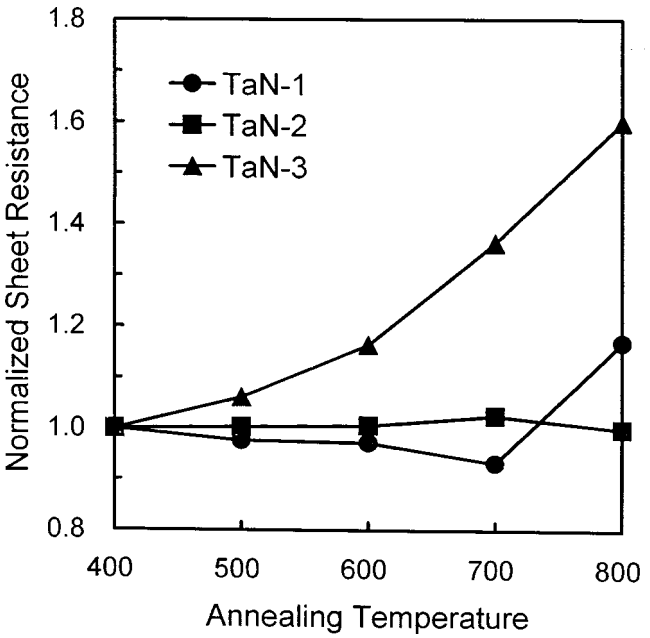

Figure 5. Variation of sheet resistance of the three kinds of TaN_x films *vs.* annealing temperature.

map, the allowed deviation of threshold voltage (V_{th}) is 25 mV at the sub-0.07 μm technology node.[25] For 400 °C annealing condition, the 3-sigma (3σ) deviation of $V_{FB,c}$ of all samples satisfied the demand of 25 mV. Particularly, the 3σ deviation of $V_{FB,c}$ of Cu/TaN-2 sample is less than 5 eV. However, the deviation of $V_{FB,c}$ continuously increases with the increase of annealing temperature and is out of the demand after annealing at and beyond 500°C.

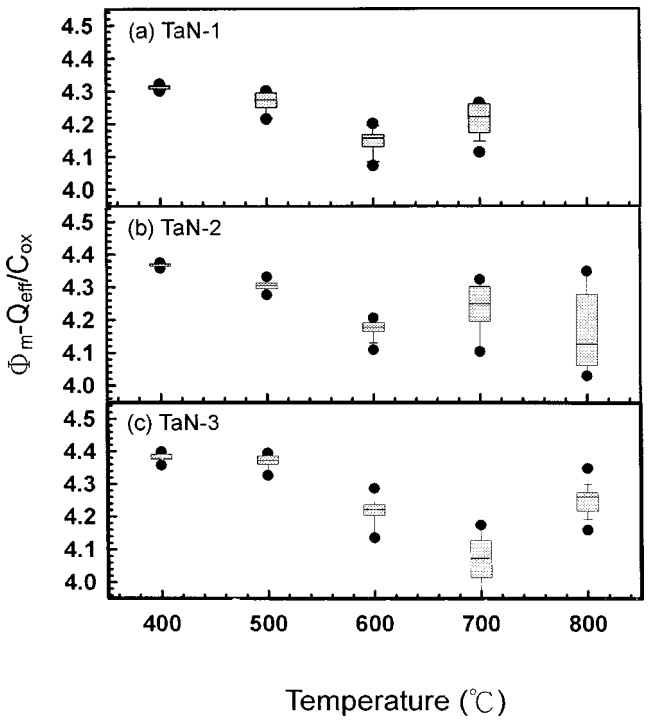

Figure 6. Corrected flatband voltage ($V_{FB,c}$) of (a) Cu/TaN-1 sample, (b) Cu/TaN-2 sample, and (c) Cu/TaN-3 sample *vs.* the annealing temperature.

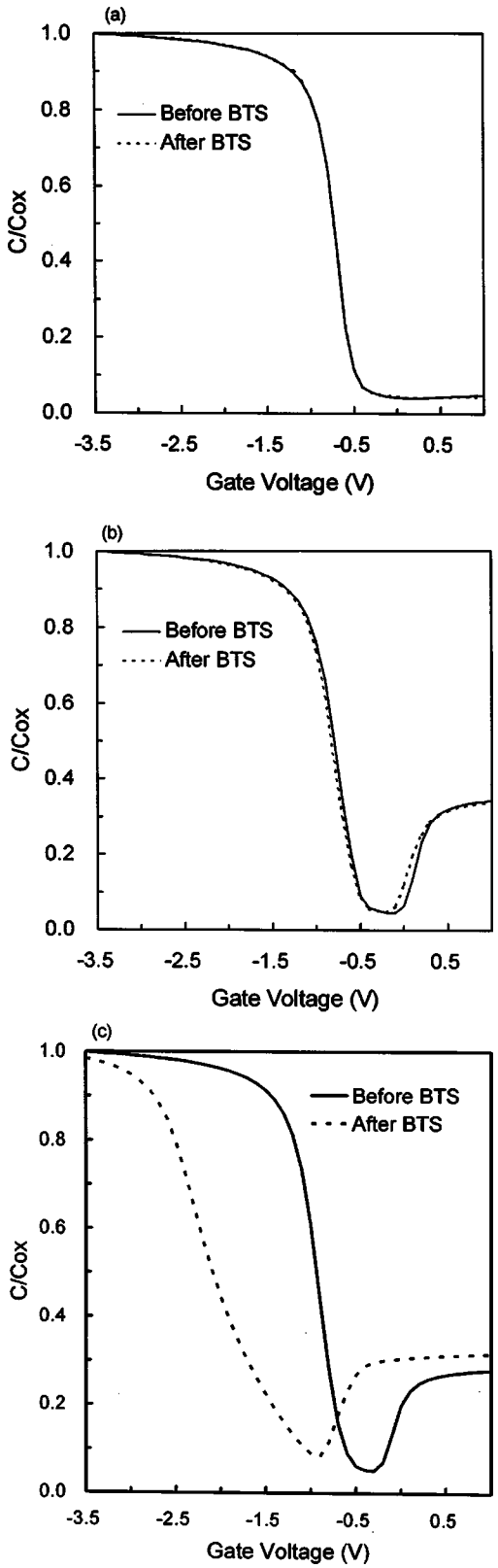

Figure 7. Capacitance/voltage curves before and after BTS test at +1 MV/cm and 150°C for 60 min of Cu/TaN-2 sample annealing at (a) 500°C, (b) 550°C, and (c) 600°C.

The reasons that cause the deviation of $V_{FB,c}$ include the characteristic of gate material, substrate doping concentration, oxide thickness, and oxide charges. The factors of oxide thickness and substrate deviation of 400 and 500°C annealed samples are ruled out using the

Table I. Mean value and standard deviation of retention time of Cu/TaN-2 MOS capacitors under transient capacitance measurement.

Temperature (°C)	400	500	550	600
Retention time (s)	33.4	14.1	<0.1	<0.1
Deviation (s)	16.2	7.4	0	0

$V_{FB,c}$ extracting procedure. The characteristics of gate electrode resulting in $V_{FB,c}$ variation are phase change and grain growth. The XRD spectra show no apparent difference among the TaN_x films annealed below 700°C. The primary phase after annealing at 400°C changed from Ta_2N to Ta_3N_5 as the N/Ta ratio increased from 0.3 to 0.65 but the difference of $V_{FB,c}$ is only 70 mV. In addition, the $V_{FB,c}$ differences of Cu/TaN_x samples annealed at the same temperature below 700°C are almost the same. It is thus clear that the phase transformation cannot dominate the $V_{FB,c}$ variation. In other words, the main reason that caused the variation of $V_{FB,c}$ should be the variation of effectives oxide charges.

Copper contamination is the first possible factor to be examined. Figures 7a, b, and c show the C-V curves before and after bias-temperature stress (BTS) test at +1 MV/cm and 150°C for 60 min of Cu/TaN-2 sample annealed at 500, 550, and 600°C, respectively. The C-V curves before and after BTS test of the 500°C annealed sample are identical. A slight shift of C-V curve toward the negative voltage axis after the BTS test is observed on the 550°C annealed sample. Furthermore, the appearance of a hump at the inversion region (about +0.5 V) reveals that the carrier lifetime at the Si substrate is shortened. Both the observations indicate that the device was contaminated, while the most possible contamination source is Cu.

The transient capacitance technique is sensitive to small quantity of deep-level atoms, such as copper.[26,27] Once the copper reaches silicon, it affects the silicon/oxide interface and the minority carrier lifetime in the bulk. Therefore, transient capacitance analysis was performed to detect lifetime degradation. The MOS capacitor was biased at the accumulation mode of −4 V and was switched to deep depletion mode of +5 V. The retention time is defined as the time required for capacitance to recover 90% of the stable value. Table I lists the retention time and its deviation of Cu/TaN-2 samples annealed at 400, 500, 550, and 600°C. The retention time of 550 and 600°C annealed samples decreases to shorter than 0.1 s, which indicates that copper had penetrated into the Si substrate. A slight decrease in the retention time of the 500°C annealed sample is discussed later. Although SIMS was not detected Cu signal in the substrate of the 550°C annealed sample, Fig. 8 shows the SIMS depth profile of Cu in the 600°C annealed Cu/TaN-2 sample before BTS test. Before SIMS analysis, the Cu film was removed with dilute HNO_3 solution. It is thus concluded that the decrease of $V_{FB,c}$ and increase in the deviation of $V_{FB,c}$ beyond 550°C annealing is related to Cu contamination. However, the decrease of $V_{FB,c}$ and increase of $V_{FB,c}$ deviation occur after annealing at 500°C even if no Cu contamination would occur.

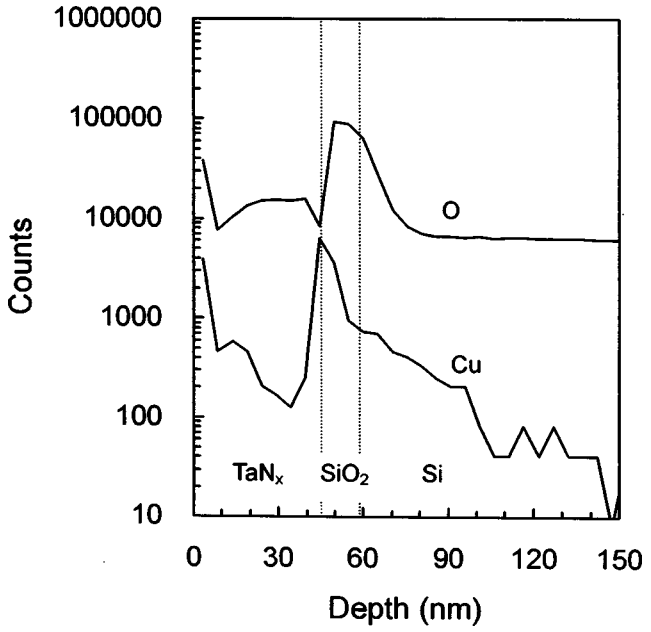

Figure 8. SIMS depth profile of Cu of the 600°C annealed Cu/TaN-2 sample. No BTS was performed before SIMS analysis and the Cu layer was removed with dilute HNO_3 solution.

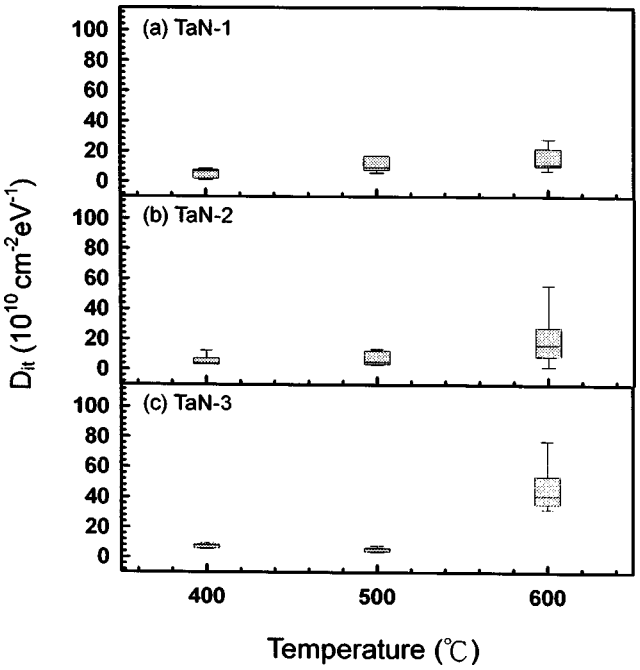

Figure 9. Interface state density (D_{it}) of (a) Cu/TaN-1 sample, (b) Cu/TaN-2 sample, and (c) Cu/TaN-3 sample *vs.* the annealing temperature.

Figure 9 shows the interface state density (D_{it}) at the midgap of Cu/TaN-1, Cu/TaN-2, and Cu/TaN-3 samples *vs.* the annealing temperature. The magnitude and deviation of D_{it} increase with the increase of annealing temperature. It is reasonable to expect that the effective oxide charges (Q_{eff}) also increase with the increase of annealing temperature. A deviation in Q_{eff} of 1×10^{11} cm^{-2} results in a deviation in flatband voltage of 46 mV. Therefore, $V_{FB,c}$ deviation can be reasonably attributed to the deviation of Q_{eff} induced by the deviation of thermal stress. For 500°C annealed samples, the drop in the $V_{FB,c}$ compared to the corresponding 400°C annealed samples is less than 60 mV, and the 3σ deviation is about 50 mV which is higher than the value of the demand. It is postulated that the deviation of $V_{FB,c}$ comes from the large difference of thermal expansion coefficient (TEC) between Cu and Si. By scaling down the gate dielectric thickness, the effect of Q_{eff} on threshold voltage can also be scaled down. However, the Q_{eff} generated by thermal stress may increase. The slight increase in the retention time of 500°C annealed sample, listed in Table I, is thus explained by the increase of surface generation rate due to the increase of D_{it}. Replacing Cu by another low resistivity material with TEC close to Si, for example, W and Mo, is recommended.

Above 600°C annealing, the $V_{FB,c}$ rises with the annealing temperature. It is presumable that the interface dipoles caused by the interaction between oxide and metal gate induce effective work function offsets since effective oxide charges are increasing.[28] The interaction between metal gate and gate dielectric is still under investigation.

Conclusion

This work investigates the work function modulation of TaN_x film and the thermal stability of Cu/TaN_x stack as the gate electrode. The N/Ta ratio was varied in the range 0.3-0.65 by using the reactive sputtering with various Ar/N_2 gas flow ratios. The main phases of the TaN-1, TaN-2, and TaN-3 films are Ta_2N, TaN, and Ta_3N_5, respectively. The TaN_x films are thermally stable up to 800°C. However, the formation of the Ta_3N_5 phase in a TaN_x film annealed at high temperature or with a high N/Ta ratio increases the effective resistivity. The work function of TaN_x is about 4.31-4.38 eV and the range is less than 70 mV. Such a short range work function modulation implies that the work function of TaN_x film is quite stable to avoid the variation induced by process disturbance. On the other hand, TaN_x is a suitable to be a gate electrode only for the surface channel n-channel metal oxide semiconductor field effect transistor (NMOSFETs). The flatband voltage decreases with an increase in the annealing temperature. In addition, the deviation of the flatband voltage increases with the annealing temperature. Although phase change, grain growth, and Cu contamination contribute at high temperature, thermal stress-induced oxide charges dominate the decrease and deviation of the flatband voltage at temperature below 500°C.

In conclusion, according to the material and electrical analysis, the Cu/TaN_x stack can be used as a gate electrode for the surface channel NMOSFETs only, and the maximum process temperature following gate electrode deposition should be lower than 500°C. The thermal stress-induced oxide charges are additional sources of deviation in the threshold voltage. This result must be considered in controlling the threshold voltage during metal gate generation.

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