Journal of The Electrochemical Society, **150** (1) G28-G32 (2003)
0013-4651/2002/150(1)/G28/5/$7.00 © The Electrochemical Society, Inc.

Characteristics of Vertical Thermal/PECVD Polysilicon Oxides Formed on the Sidewall of Polysilicon Films

M. Z. Lee, Y. A. Chang, Chung-Len Lee, and Tan-Fu Lei[z]

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

Vertical thermal and PECVD (plasma enhanced chemical vapor deposition) polysilicon oxides, formed on polysilicon sidewalls, are investigated to demonstrate that the oxides on polysilicon sidewalls have much better electrical qualities than do conventional planar polysilicon oxides. For thermally grown vertical polysilicon oxides, the charges-to-breakdown were as high as 10 C/cm^2, values that are comparable to that of the single crystal oxide. This improvement is primarily due to the fewer number of grain boundaries in the vertical direction of the polysilicon.
© 2002 The Electrochemical Society. [DOI: 10.1149/1.1524613] All rights reserved.

Manuscript submitted February 3, 2002; revised manuscript received July 2, 2002. Available electronicallyNovember 21, 2002.

Layers of polycrystalline silicon (polysilicon) are used extensively in the fabrication of silicon metal-oxide semiconductor (MOS) devices. Generally, these films are heavily doped to minimize their electrical resistance, and are used to form gate electrodes and interconnections in MOS integrated circuits or charge-coupled devices. They are also used as emitter contacts in bipolar transistors and resistors.[1-4] The ongoing trend to scale down devices demands a reduction in the thickness of polysilicon films and inter poly oxides, to yield a higher integration density. Moreover, innovative device structures such as vertical thin film transistors (VTFTs)[5,6] and processes have been proposed to increase chip packing density. They are suited to high density integration since their channel lengths are determined by the thickness of SiO_2 or polysilicon films, rather than by the photolithographic limitations. However, to our knowledge, no research has discussed the quality of the vertical polyoxides grown on the sidewall of a polysilicon thin film, on which the vertical device is to be made. Therefore, the quality of the vertical polyoxide for the nonplanar structure device, including the dielectric breakdown field (E_{bd}) and the charge to breakdown (Q_{bd}) must be studied.[7,8]

Over the last year, we have researched the quality of thermally grown oxides on the vertical sidewalls of polysilicon films and the results have been submitted to *IEEE Electron Device Letters*. In this work, however, we consider these oxides in more detail. Additionally, a low temperature plasma enhanced chemical vapor deposition (PECVD) oxide is fabricated on the sidewall for further research. The experimental results indicate that the vertical polyoxide can yield an E_{bd} and Q_{bd} comparable to those of the conventional planar oxide grown on single crystal silicon. This improvement comes primarily from the reduced number of grain boundaries on the vertical wall of the polysilicon film.

Experimental

Figure 1 shows the vertical structure used in the experiments. A 500 nm silicon dioxide film grown on a p-type silicon (100) wafer was used as an isolation layer by wet thermal oxidation. Then a 1 μm thick polycrystalline silicon film (poly-I) was deposited by low pressure CVD (LPCVD) on the oxidized wafer and doped with $POCl_3$ to yield a substrate polysilicon layer with 10-20 Ω/□ sheet resistance. The deposition process was separated into one to six steps to yield a polysilicon film with various numbers of layers, but with the same total thickness to investigate the effect of grain boundaries in the vertical sidewall of the polysilicon film. Then, a 300-500 nm PE-tetraethylorthosilicate (PE-TEOS) polyoxide film was deposited by PECVD on poly-I to isolate the gate and the substrate in the planar region. Thereafter, the top isolation oxide and poly-I were patterned to form the vertical sidewall by dry etching.

Before inter poly oxides were formed, a thin sacrificial oxide film was grown by wet thermal oxidation and then stripped for partial samples to perform a sacrificial process. After standard RCA cleaning, gate oxides with three different thicknesses were grown using a thermal furnace or deposited by PECVD. The temperature of the furnace was 900°C, in a dry O_2 ambient, and the PECVD was performed at 300°C with TEOS vapor. For PECVD TEOS deposition samples, an additional 900°C rapid thermal anneal (RTA) annealing in N_2O ambient was applied to improve the quality of the oxide. The polysilicon gate was then formed and capped with a layer of passivation oxide. Finally, Al contact patterns were formed and used to create ohmic contacts.

The top views of devices include two patterns, one circular and the other square, as shown in Fig. 2a, designed to investigate the influence of corners on the quality of the vertical polyoxide. The border length of square patterns is 200 μm, and the radius of circular patterns is 150 μm. Figure 2b depicts the scanning electron microscopy (SEM) image of the sidewall of the square pattern after dry etching. The step in this figure included 1 μm of polysilicon substrate and 300 nm of isolation oxide.

The sheet resistance was measured using a four-points probe and the thickness was determined by cyclic voltammetry (CV) measurement. Finally, an HP 4156B was used to measure the current-density potential (J-E), E_{bd}, and Q_{bd} characteristics. Capacitors with an area of 1.6×10^{-5} cm^2 were used to measure the capacitance.

Results and Discussion

The results of CV measurement cannot be considered alone to determine the thickness of the vertical polyoxides on the sidewall of polysilicon films, because of the parasitic capacitance. Figure 3 presents the capacitance distribution in the vertical structure. The pure capacitance induced by the vertical oxide is labeled as C3k, C4k, or C5k as shown in Fig. 3. The thickness of the isolation oxide was changed from 300 to 500 nm to determine the parasitic capacitance induced by the bottom polysilicon and the extension of the vertical gate in the isolation oxide region. The capacitors effectively created between the bottom polysilicon and the gate in the vertical region are C3k, C4k, and C5k as shown in Fig. 3. The bottom polysilicon and top overlap gate also generate an additional parasitic capacitance. Two overlapping lengths, 5 and 10 μm are designed to realize this capacitance. The generated capacitors are labeled as C5u and C10u as shown in Fig. 3. The total capacitances, obtained with isolation oxides of different thicknesses, obtained by CV measurement, are labeled Cm3k, Cm4k, or Cm5k. Hence these capacitors are related by

$$\text{C3k, 4k, or 5k} = \text{Cm3k, 4k, or 5k} - \text{C5u or 10u} \quad [1]$$

This equation yields C3k, C4k, and C5k for different gate oxide thicknesses. Finally, C3k, C4k, and C5k can be plotted and the ca-

[z] E-mail: tflei@cc.nctu.edu.tw

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

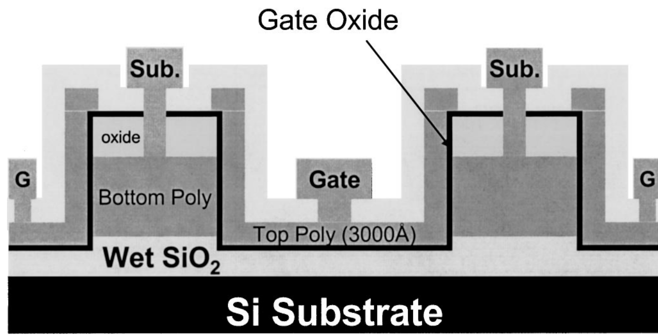
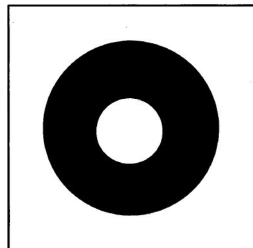
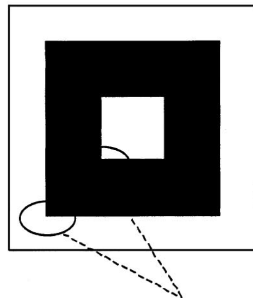


Figure 1. Cross section of vertical polyoxide structure.





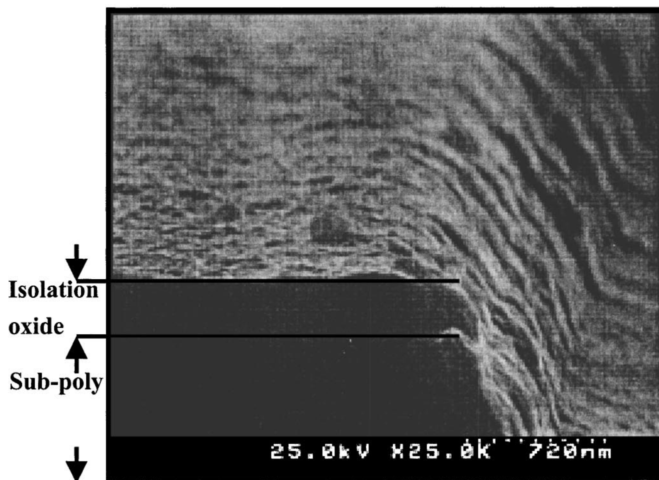


Figure 2. (a) Designed patterns of vertical polyoxide structure. (b) SEM image of the sidewall of the square pattern after dry etching.

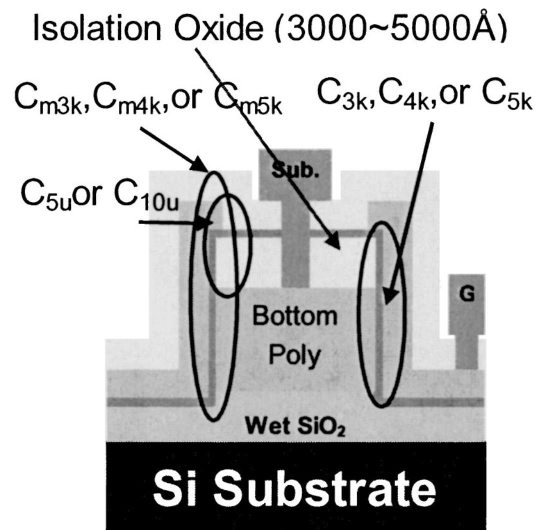


Figure 3. Parasitic capacitance distribution in vertical polyoxide structure.

pacitance for zero isolation oxide thickness can be extracted as C_{ini}. Then the oxide thickness in the vertical direction is given by

$$T_{\text{ox}} = kA/C_{\text{ini}} \quad [2]$$

where A has capacitor area $1.6 \times 10^{-5}\ \text{cm}^2$.

Figure 4 shows the fitting plot of the capacitance of the 10.6 nm vertical polyoxide. The vertical capacitance increases from 13.41 to 14.49 pF as the thickness of the isolation oxide increases from 300 to 500 nm. The pure vertical capacitance is extracted as 11.22 pF, and the vertical polyoxide thickness is 10.6 nm. Transmission electron microscopy (TEM) is used to verify the fitted results. Figure 5 shows TEM images of oxides on (a) vertical sidewall and (b) planar polysilicon film. The thickness of the vertical polyoxide is about 10

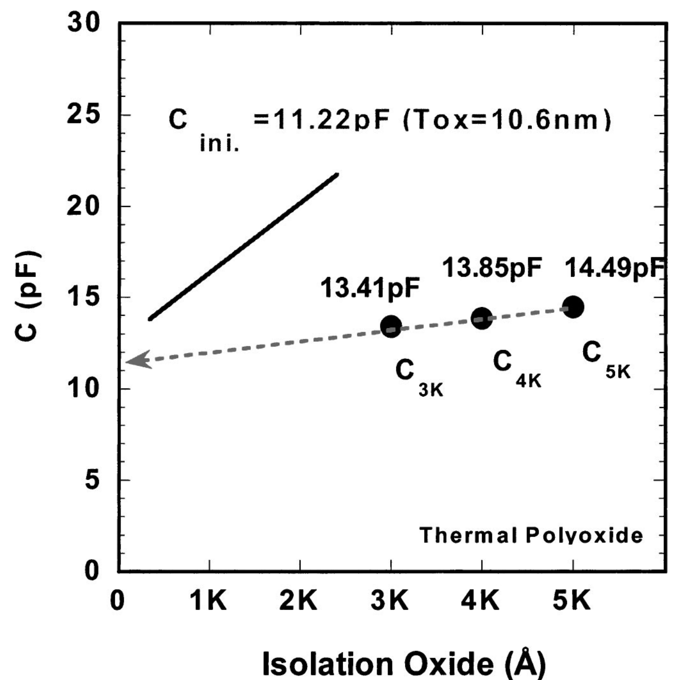
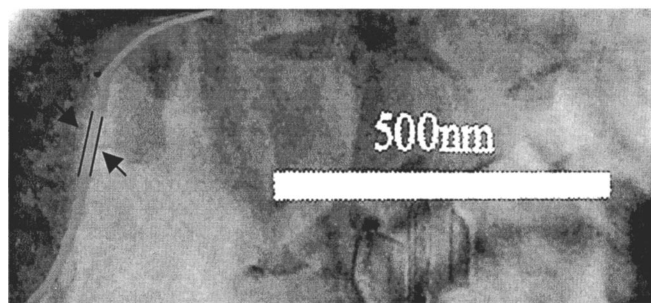


Figure 4. Oxide thickness-fitting curve for thermal vertical polysilicon oxide.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).



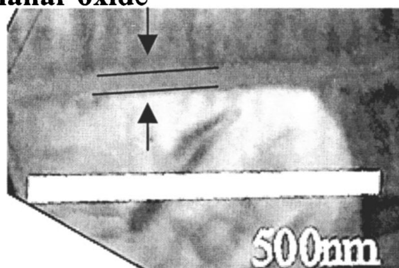


Figure 5. TEM images of oxides on (a) vertical sidewall and (b) planar polysilicon film.

nm, and the thickness of the planar polyoxide is about 20 nm, according to the TEM results. This result is of the same order as the fitted data, 10.6 and 18.5 nm.

Table I lists the final oxide thicknesses. The oxide thicknesses of planar structures are measured from planar polysilicon oxides, under the same substrate and oxide conditions as for vertical polysilicon oxides. This table reveals that the growth or deposition of oxides is much slower in the vertical direction than in the planar direction, because the grain boundary density and the gas adsorption rate are lower on the sidewall of the polysilicon layers.[9]

Figure 6 shows E_{bd} distributions of the thermal vertical polyoxides for three different thicknesses, where 6.5, 10.6, and 18.2 nm are the thicknesses of the oxide grown on the vertical sidewall of polysilicon films. For each thickness, data for samples with and without presacrificial oxidation are presented. A thinner vertical polyoxide yields a larger E_{bd}.[10,11] The presacrificial oxidation samples exhibit lower E_{bd}s, especially $+E_{bd}$s. This result is believed to follow from the increase in the roughness of the surface due to presacrificial oxidation. However, the E_{bd} values of circular samples are approximately the same as those of the square samples; that is, the corner

Table I. Oxide thickness of planar and vertical polysilicon oxides.

Gate oxide condition	Planar structure thickness (Å)	Vertical structure thickness (Å)
Thermal 100	100	65
Thermal 200	185	106
Thermal 300	284	182
PECVD 100	138	107
PECVD 200	184	118
PECVD 300	311	139

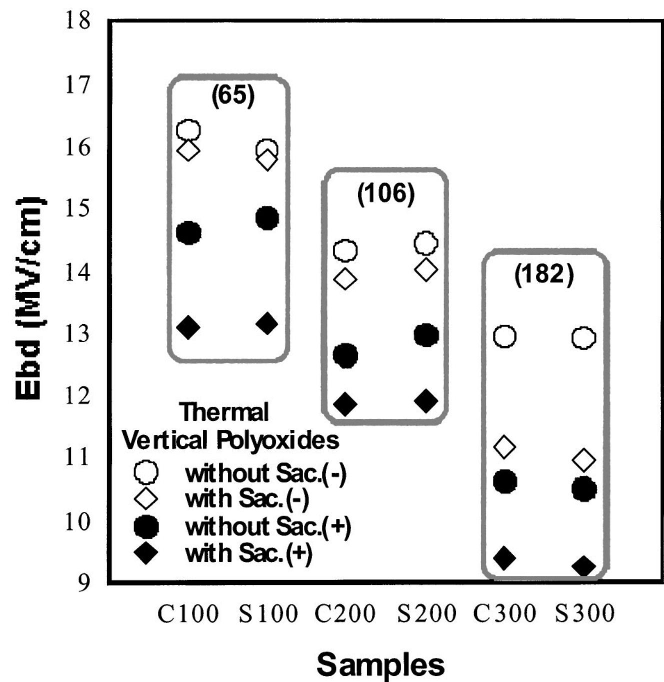


Figure 6. E_{bd} distributions of vertical thermal polyoxides with three thicknesses, 6.5, 10.6, and 18.2 nm. S and C represent square and circular pattern samples. (+) and (−) indicate the positive and negative gate bias applied to gate.

effect is insignificant for the thermal vertical polyoxide, because the sharp corners have been smoothed during high temperature oxidation, and thereafter do not affect the quality of vertical oxide.

Figure 7 shows E_{bd} distributions of the 10.7-13.9 nm thick PECVD TEOS vertical polyoxides. As the vertical oxide thickness

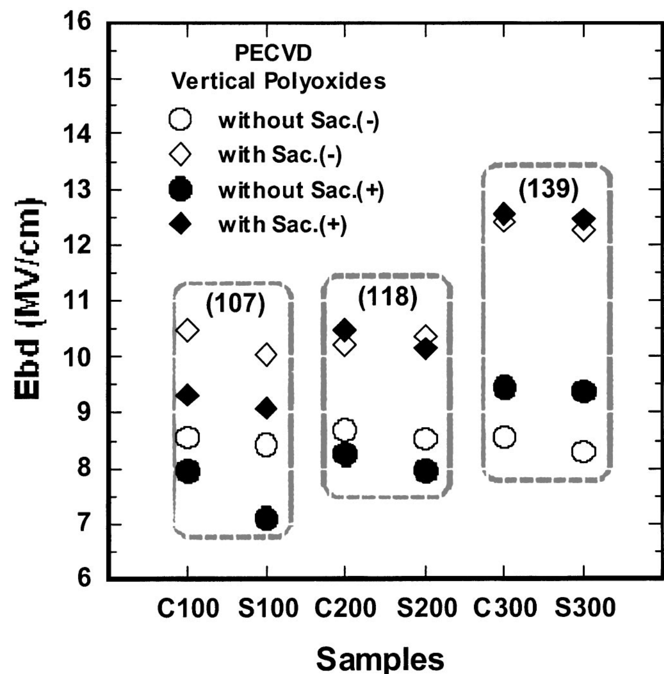


Figure 7. E_{bd} distributions of vertical PECVD polyoxides with three thicknesses 6.5, 10.6, and 18.2 nm. S and C represent square and circular pattern samples.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

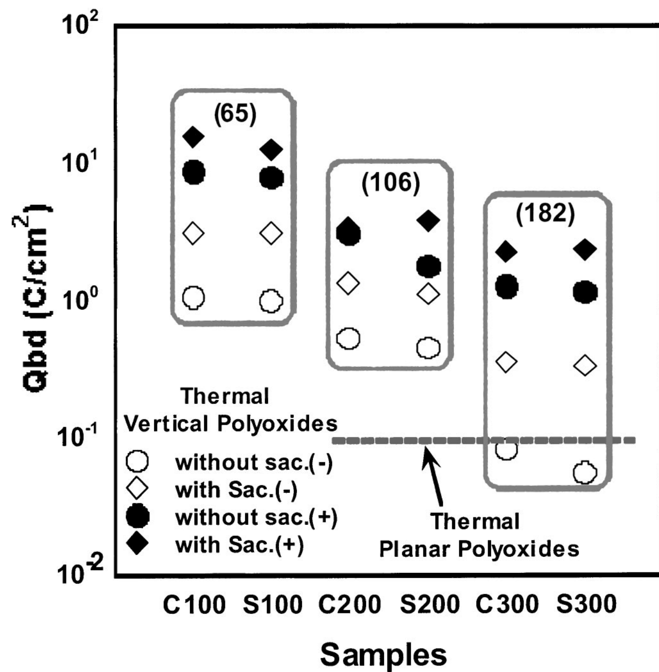


Figure 8. Q_{bd} distributions of the three vertical thermal polyoxides in Fig. 5.

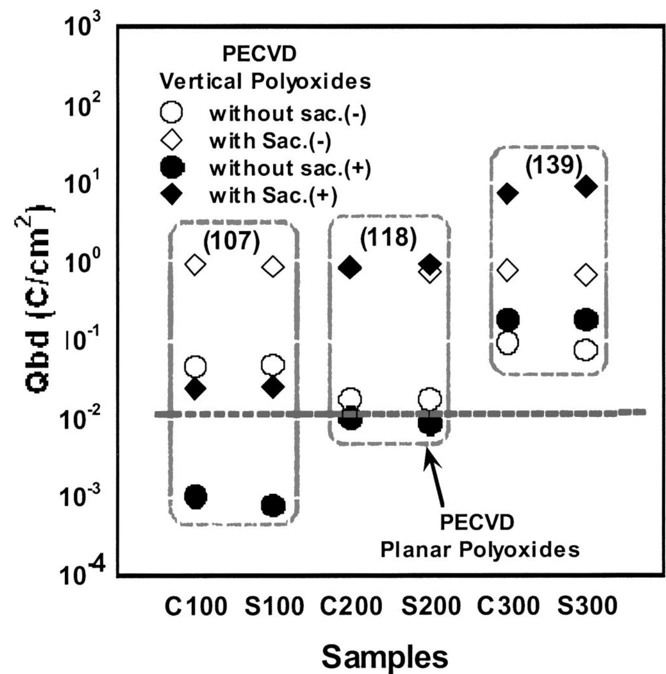


Figure 9. Q_{bd} distributions of the three vertical PECVD polyoxides in Fig. 6.

increases, the E_{bd} remains almost constant or increases slightly. This trend is the same as for low temperature deposited oxide, prepared on conventional planar structures. The samples with presacrificial oxidation exhibit a higher E_{bd} than do samples without the oxidation. The result follows from the fact that the reactive ion etch (RIE) process used to form the substrate patterns damages the polysilicon sidewall. However, the PECVD deposition temperature is too low to anneal the residual damage. Hence, an additional presacrificial oxidation process is required to remedy these defects, unlike for the thermal vertical oxide. The corners clearly degrade the vertical oxides' E_{bd} values. In particular, for samples without presacrificial oxidation, the E_{bd} values of the samples with circular patterns are higher than those of the samples with square patterns.

Figure 8 presents Q_{bd} values of the same samples as were considered in Fig. 6. These samples are stressed at $+50$ mA/cm^2 for $+Q_{bd}$ and -5 mA/cm^2 for $-Q_{bd}$. The Q_{bd} values are approximately two orders higher than those of the conventional planar polyoxides. Also, a thinner polyoxide corresponds to a higher Q_{bd}. For the 6.5 nm sample, Q_{bd} can be as high as 10 C/cm^2, because polysilicon grains in the vertical direction are columnar, so the grain boundaries are fewer than in the horizontal direction. Additionally, the samples with presacrificial oxidation have higher Q_{bd} values. Although the additional oxidation increases the roughness of the substrate, the surface damage induced by RIE or remnant impurities on the bottom polysilicon surface can be removed by sacrificial oxidation, reducing the number of traps in the bulk of the polyoxide, thereby decreasing E_{bd} but increasing Q_{bd}.

Figure 9 shows Q_{bd} for the PECVD vertical polysilicon oxides. These samples are stressed at $+0.1$ mA/cm^2 to yield $+Q_{bd}$ and -5 mA/cm^2 to yield $-Q_{bd}$. Q_{bd} increases with the thickness of the PECVD oxide because of the instability at the beginning of PECVD oxide deposition. The Q_{bd} values of these vertical samples also exceed those of conventional planar PECVD TEOS polyoxides. Besides, samples with the preoxidation process also have higher Q_{bd} values than samples without the preoxidation process. We believe that the major cause of the increase in Q_{bd} is the reduction of RIE-induced damage in the polysilicon sidewall. However, the Q_{bd} values of circular samples are approximately the same as those of square samples, and the corner effect is insignificant for the vertical polyoxide.

Figures 8 and 9 show that the vertical polysilicon oxides have much higher Q_{bd} values than do conventional planar polysilicon oxides. This result follows from the lower grain boundary density in the vertical direction of the polysilicon. This suggestion was checked by changing the substrate's structure and measuring the results, as plotted in Fig. 10. Figure 10 presents J-E curves of vertical oxides with the same thickness, 6.5 nm, but were made on the sidewall of several equally thick polysilicon substrates with various numbers of layers. Figure 11 presents a TEM image of a two-layered

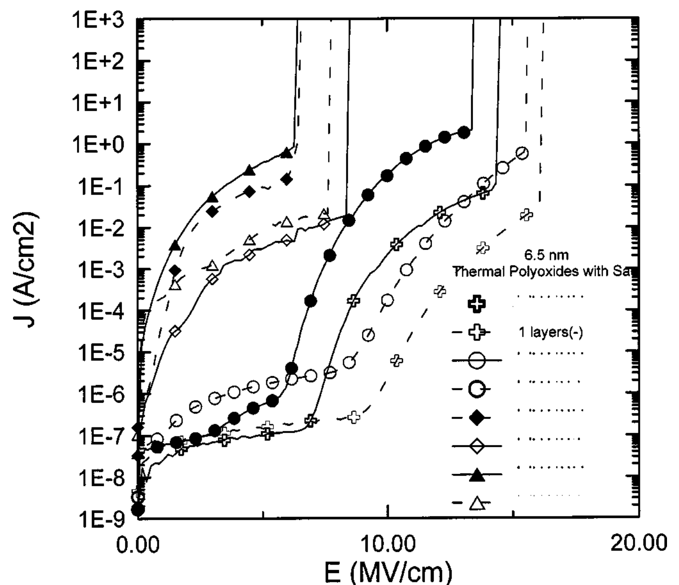


Figure 10. J-E curves of vertical oxides with the same thickness of 6.5 nm, but made on the sidewall of several equally thick polysilicon substrates with various numbers of layers.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

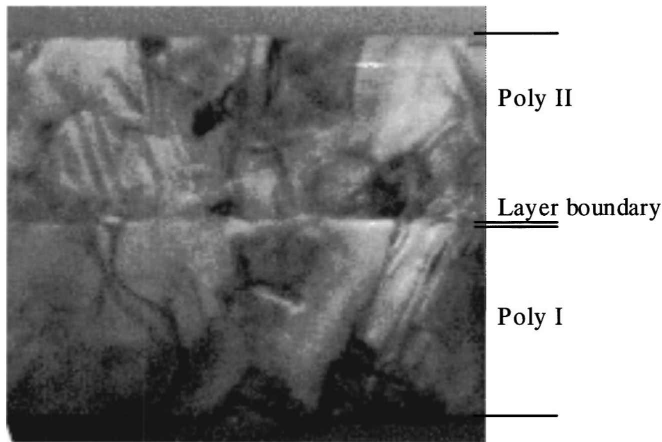


Figure 11. TEM image of a polysilicon film with two layers.

polysilicon film. This figure shows that the grains grow from the bottom to the top, to form a single grain in the vertical direction. Hence, the number of polysilicon layers controls the numbers of vertical grains in polysilicon. The J-E curve degrades away from the standard Fowler-Nordheim (F-N) characteristics as the number of layers increases. This experiment demonstrates clearly that the increase in the number of polysilicon layers increases the number of grain boundaries in the vertical direction, degrading the quality of the grown polyoxide. The improvements in the vertical polyoxide result from the reduced number of grain boundaries in the vertical direction of the deposited polysilicon substrate.

Conclusions

Thermally or PECVD-deposited vertical polyoxides formed on the sidewall of a polysilicon substrate have higher E_{bd} and Q_{bd} values than do conventional planar polyoxides. The improvements are primarily due to the fewer grain boundaries present in the vertical direction of the polysilicon substrate. Additional presacrificial oxidation can be used to improve the quality of vertical oxide, and the corners in patterns must be taken into consideration, especially for low temperature oxides.

Acknowledgments

This work was partially supported by the National Science Council of the Republic of China under contract no. NSC89-2218-E009-069.

National Chiao Tung University assisted in meeting the publication costs of this article.

References

1. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Electron Device Lett.,* **44**, 526 (1997).
2. L. Faraone, *IEEE Trans. Electron Devices,* **ED-33**, 1785 (1986).
3. S. L. Wu, T. Y. Lin, C. L. Lee, and T. F. Lei, *IEEE Electron Device Lett.,* **14**, 113 (1994).
4. E. G. Lee and J. J. Kim, *Thin Solid Films,* **226**, 123 (1993).
5. C. S. Lai, T. F. Lei, and C. L. Lee, *IEEE Electron Device Lett.,* **17**, 199 (1996).
6. T. Zhao, M. Cao, K. C. Saraswat, and J. D. Plummer, *IEEE Electron Device Lett.,* **15**, 415 (1994).
7. H. J. Mattausch, H. Baumgartner, R. Allinger, M. Kerber, and H. Braun, *IEEE Trans. Electron Devices,* **47**, 1251 (2000).
8. H. J. Mattausch, R. Allinger, M. Kerber, and H. Braun, *IEEE Electron Device Lett.,* **19**, 402 (1998).
9. S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI ERA*, Chap. 7, Lattice Press, Sunset Beach, CA (1986).
10. C. M. Osburn and D. W. Ormond, *J. Electrochem. Soc.,* **119**, 591 (1972).
11. E. Harari, *J. Appl. Phys.,* **49**, 2478 (1978).

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).