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Polycrystalline silicon thin-film transistor with self-aligned SiGe raised source/drain

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We have fabricated a polycrystalline silicon thin-film transistor with self-aligned SiGe raised source/drain (SiGe-RSD TFT). The SiGe-RSD regions were grown selectively by ultrahigh vacuum chemical vapor deposition at 550 °C. It was observed that, with SiH_4 and GeH_4 gas flow rates of 5 and 2 sccm, respectively, the poly-SiGe could be selectively grown up to 100 nm for source/drain regions. The resultant transistor structure features an ultrathin active channel region (20 nm) and a self-aligned thick source/drain region (120 nm), which is ideally suited for optimum performance. The significant improvements in electrical characteristics, such as higher turn-on current, lower leakage current, and higher drain breakdown voltage have been observed in the SiGe-RSD TFT, compared to the conventional TFT counterpart. These results indicate that TFTs with SiGe raised source/drain structure would be highly promising for ultrathin TFTs applications. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1528727]

Polycrystalline silicon thin-film transistors (poly-Si TFT) are attractive for many potential applications, including the active matrix liquid crystal display (AMLCD).[1,2] In order to integrate peripheral driving circuits on the same glass substrate, both a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT device characteristics. It has been previously reported that the use of a thinner active channel film is beneficial for obtaining a higher current drive.[3–5] The use of thin active channel layer, however, inevitably results in poor source/drain contact and large parasitic series resistance. Worse, for the super thin active channel devices, short-channel poly-Si TFTs also suffer from a low drain breakdown voltage. An ideal TFT device structure, therefore, should consist of a thin active channel region, while maintaining a thick source/drain region. The thick source/drain region serves not only to reduce the lateral electric field, thus maintaining the breakdown voltage,[6,7] but to reduce the source/drain series resistance.

In this letter, a TFT with self-aligned SiGe raised source/drain (SiGe-RSD) structure is proposed and fabricated. Silicon wafers coated with a 500 nm thermal oxide were used as the starting substrates. An ultrathin layer of 20 nm undoped amorphous-Si (*a*-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited *a*-Si layer was then recrystallized for 24 h in nitrogen ambient at 600 °C. After patterning and plasma etching to form the active device island, a 50 nm gate oxide was deposited by plasma-enhanced CVD (PECVD) method. This was followed by the deposition and patterning of a 300 nm poly-Si gate layer. A 300 nm TEOS oxide was then deposited by PECVD, and anisotropically etched by reactive ion etching (RIE) to form a sidewall spacer abutting the poly-Si gate. The remaining TEOS oxide above the source and drain regions was removed in diluted HF to ensure the exposure of the S/D poly-Si region. Subsequently, some wafers were loaded into an UHVCVD system to selectively grow an undoped SiGe layer on the exposed source, drain, and gate regions at 550 °C. The thickness of the SiGe layer was 100 nm, and the Ge composition was 0.68. In previous work, we have shown that fine-grain poly-SiGe films could be deposited at 550 °C in UHVCVD system without further treatment.[8–10] The effect of GeH_4 flow on the incubation time for poly-SiGe films deposited on a oxide surface have been reported previously.[9,11] In this work, with SiH_4 and GeH_4 gas flow rate of 5 and 2 sccm, respectively, a longer incubation time compared to our previous results could be obtained. Therefore, we could grow a thicker poly-SiGe film up to 100 nm for S/D regions. The chamber pressure for the gas flow rates and the deposition time were 0.37 mTorr and 4 h, respectively. The number of nuclei on the oxide is negligible from our SEM images, and this indicated that under this condition, the selective growth could proceed up to 4 h. The growth of SiGe on source, drain, and gate regions was inherently self-aligned. A cross-sectional TEM image of the fabricated structure is shown in Fig. 1. Next, the gate electrode and source/drain regions were implanted by phosphorus ions at a dosage of 5×10^{15} cm^{-2}, and an energy of 55 keV. For comparison, wafers with conventional TFTs were also processed on the same run by deliberately skipping the growth of SiGe and using a phosphorus implant energy of 10 keV instead. All wafers were then subjected to a RTA anneal at 850 °C for 20 s for dopant activation. Next, a 300-

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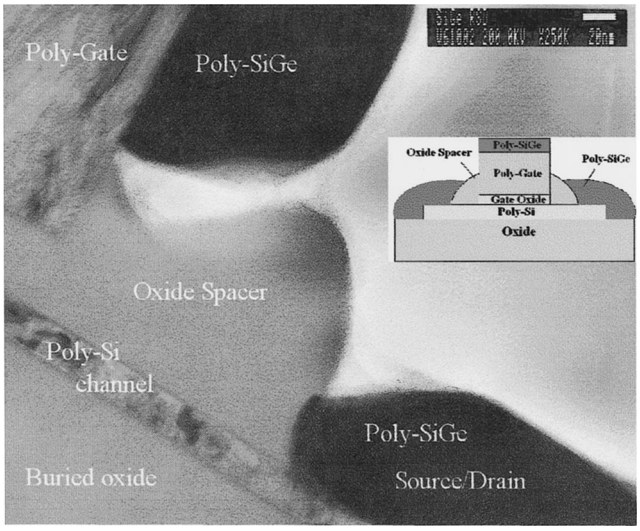

FIG. 1. (Color) Cross-sectional transmission electron microphotograph (TEM) of a fabricated SiGe-RSD TFT. The thickness of the SiGe on source/drain region is ~100 nm.

nm-thick oxide was formed as the cap layer by PECVD. Finally, contact hole definition and Al metallization were performed, followed by a 400 °C sintering in nitrogen ambient for 30 min. For lower thermal budget in AMLCD applications, lower temperature for SPC and dopant activation can be applied onto glass substrate. The resultant thickness and extracted resistivities in S/D regions were 20 nm and 4.6 Ω cm for conventional and 120 nm and 2×10^{-3} Ω cm for SiGe-RSD TFTs, respectively. This indicates that a significant reduction in S/D resistivity was indeed obtained by using a thicker poly-SiGe film.

Figure 2 shows typical transfer characteristics for the conventional and SiGe-RSD TFTs at drain voltage (V_d) of 5 V. It can be seen that the turn-on characteristics are significantly improved for SiGe-RSD TFT. Approximately one order of magnitude improvement in the on/off current ratio is observed, compared to the conventional TFT. The larger leakage current for conventional TFTs is probably due to the stronger horizontal electric field near the drain side, which results in smaller breakdown voltage for conventional TFTs, as will be discussed later. Figure 3 shows the output characteristics for both SiGe-RSD and conventional TFTs. It can be seen that for the conventional TFT, as the gate voltage gets higher, the $I-V$ curves behave more like resistance. This is because for larger gate bias, the channel resistance becomes smaller; hence the dominant resistance would be due to the source and drain region ($2R_{S/D}$, i.e., $R_{total}=2R_{S/D}+R_{channel}$). With the ultrathin source/drain region, the conventional TFT suffers from a high $R_{S/D}$, so when the gate bias increases, the output current is subject to be limited by the source and drain resistance ($R_{S/D}$), as shown in Fig. 3. In contrast, due to its thick source/drain region, the $R_{S/D}$ is much smaller for SiGe-RSD TFT. As a result, the output current is not limited by the parasitic source/drain resistance, and therefore is much larger than that of the conventional TFT.

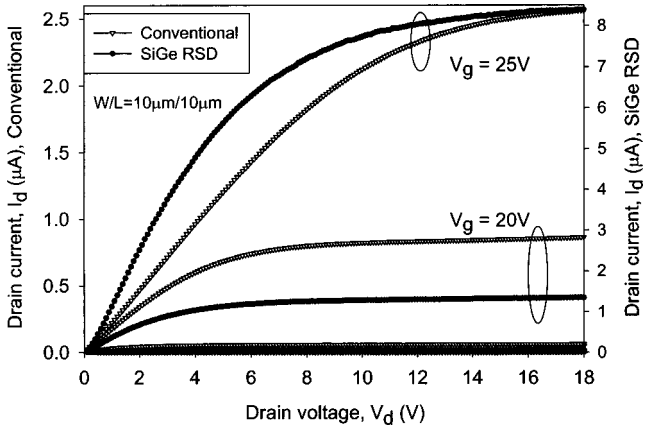

FIG. 3. Comparison of I_d-V_d output characteristics of SiGe-RSD and conventional poly-Si TFTs. The triangle and circle are for the SiGe-RSD and conventional TFTs, respectively.

Figure 4 shows the drain breakdown voltage, which is defined arbitrarily as the drain voltage when the drain current equals 2 nA with $V_{gs}=5$ V, for both the conventional and SiGe-RSD TFTs. It can also be seen from Fig. 4 that for channel length (L_g) changing from 10 to 1 μm, the breakdown voltage for conventional TFTs decreases from 10.7 to 5.3 V (~50%), while only 12% of difference (from 16.1 to 14.2 V) in breakdown voltage is observed for SiGe RSD TFTs. The larger breakdown voltage for SiGe-RSD TFTs can be attributed to the thicker source/drain region and hence smaller horizontal electric field near the drain side.[4,5] This

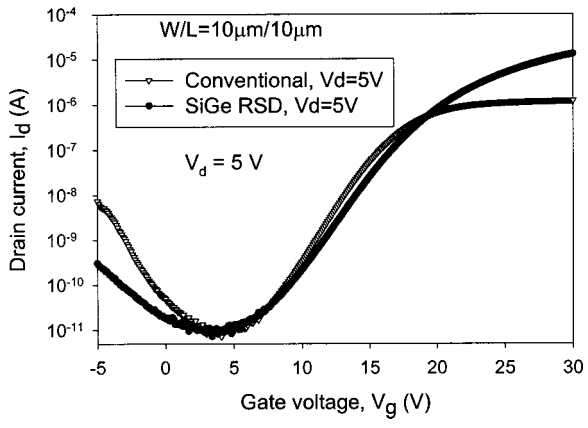

FIG. 2. Comparison of I_d-V_g characteristics of SiGe–RSD and conventional poly-Si TFTs for $V_d=5$ V.

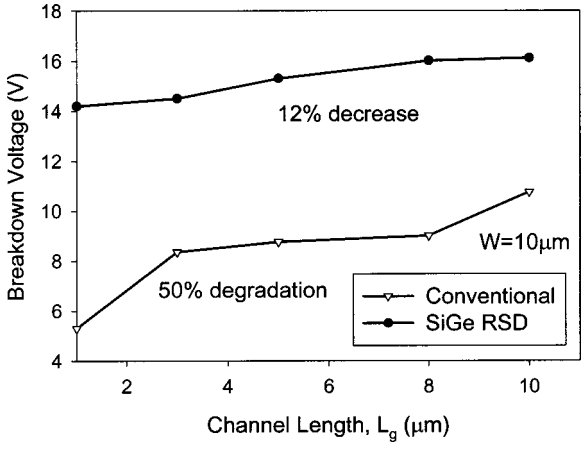

FIG. 4. Drain breakdown voltage as a function of channel length (L_g) for both SiGe-RSD and conventional TFTs.

result is also consistent with the larger leakage current observed in Fig. 2 for conventional TFTs with $L_g = 10\ \mu$m.

In summary, we have proposed a poly-Si TFT with self-aligned SiGe raised source/drain (SiGe-RSD) structure without additional masks. Our experimental data show that the SiGe-RSD poly-Si TFT has a higher turn-on current and on/off current ratio, compared to the conventional TFTs. Moreover, the drain breakdown voltage for SiGe-RSD poly-TFTs is significantly improved for smaller channel length. The structure is therefore ideally suitable for implementing high-density and high-performance driver circuits on the glass panel for AM-LCD applications.

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