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New Nanometer T-Gate Fabricated by Thermally Reflowed Resist Technique

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Novel nanometer T-gate process has been developed utilizing electron beam (EB) lithography and thermally reflowed resist technique. Through well-controlled EB exposure dosage, heating time and reflow temperature, the resist structures can be efficiently reflowed to form the desired T-gate configuration with dimension ranging from 150 nm to 30 nm. After Ti/Pt/Au metal deposition by electron gun evaporation and lift-off process, the nanometer T-gates with thickness of about 500 nm were formed. With the optimized conditions, ultra-short 30 nm T-shaped gate was clearly demonstrated on the GaAs substrate. This is the smallest T-gate reported with the thermally reflowed technique in the literature so far and can practically be used in the GaAs monolithic microwave integrated circuit (MMIC) fabrications. [DOI: 10.1143/JJAP.41.L1508]

KEYWORDS: nanometer T-gate, reflowed resist technique, lift-off process, electron beam lithography, monolithic microwave integrated circuit

With the advances in nano-fabrication tools, techniques and material growth methods, high performance devices such as GaAs and InP-based high electron mobility transistors (HEMTs) are currently attracting great interests and investments. Actually, they are considered as the most promising candidates for active devices used both high-speed digital integrated circuit (ICs) and millimeter-wave and microwave analog ICs. In order to improve the device performance, submicron T-shaped gates, in addition to high mobility device structures, are usually used to achieve higher cut-off frequency (f_T) and higher maximum oscillation frequency (f_{max}) for the devices. Therefore, a well-controlled nanolithography technology is a strong requirement for the fabrication of high frequency devices. So far, a number of processes[1–5] have been reported. Yamashita *et al.*[1] succeeded in fabricating 25-nm-T-shaped gates by combining electron beam (EB) lithography and plasma chemical vapor deposition (CVD) with conventional reactive ion etching (RIE) to define a multilayer resist and resulted in a device with f_T of 396 GHz. Suemitsu *et al.*[2,3] have demonstrated a fabrication technology utilizing a fulllerene-incorporated nanocomposite resist for EB lithography and a two-step-recessed gate structure[4] and have succeeded in fabricating InAlAs/InGaAs HEMTs with f_T of 352 GHz. However, the T-gate fabrication steps described above were too complicated. InP based HEMTs with gate length ranging from 0.06 to 0.2 μm[5] were fabricated by using triple resist layer structure, which consists of a bottom layer of polymethylmethacrylate (PMMA), a middle layer of poly(dimethylglutarimide)(PMGI), and a top layer of PMMA. However, there were too many developers used to enable the fine gate formation for this process. Other nanometer gate processes that combined optical and EB lithography[6] have also been reported, however, all the processes required accurate alignment and highly sophisticated mask design.

In this study, a simple technique for the fabrication of the nanometer T-gate was developed. Standard EB lithography and thermally reflowed resist technique[7,8] were employed to form the expected resist profile for nanometer T-gate formation. High-resolution scanning electron microscope (SEM) was then used to measure the dimension of the nanometer footprint. Ultra-short 30-nm T-shaped gate on GaAs substrate was realized, and the optimum conditions for the formation of smallest gaps of T-gate footprints were obtained.

Figure 1 summarizes the bi-layer resist process flow for the fabrication of the nanometer T-gates. First, typical 160-nm-T-gate trenches were formed by exposing at the Leica EBML300 EB direct writing system at 40 KeV with a thermionic LaB_6 filament emitter and using the bi-layer EB resists which consist of a 250 nm bottom high-resolution PMMA layer and a 720 nm top sensitive polymethyl methacrylate-methacrylic acid P(MMA-MAA) layer. Then, single center exposure and added sidewall exposure were used to define both the footprint and the head of the

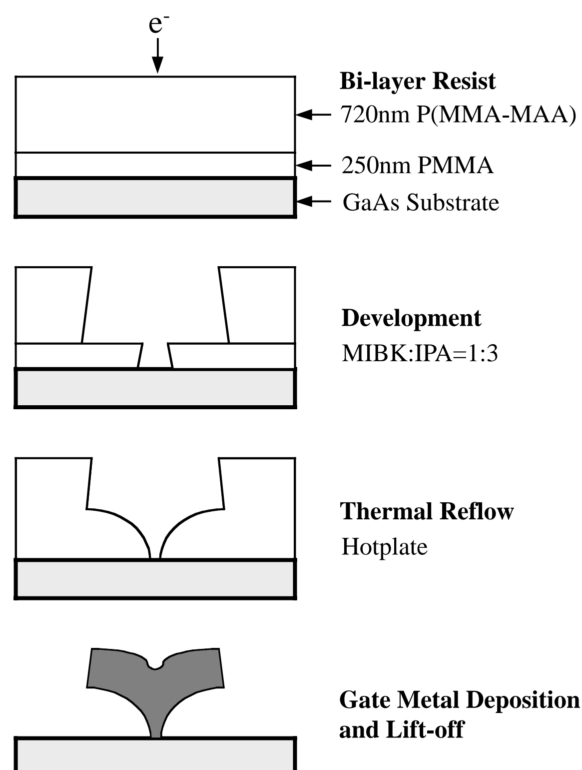

Fig. 1. Process flow of the thermally reflowed T-gate.

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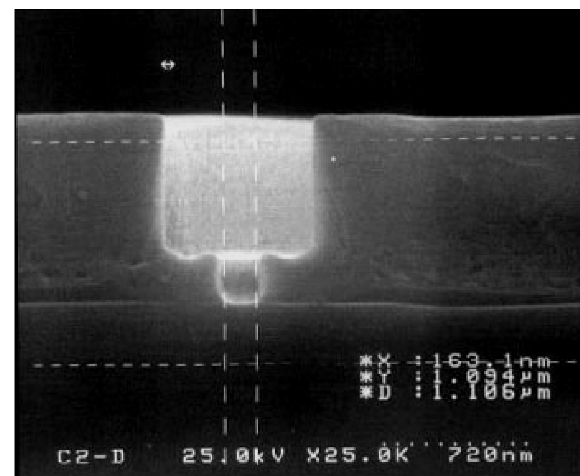
T-gate by modulating the exposure doses. After EB exposure, the samples were developed in methyl isobutyl ketone: isopropyl alcohol (MIBK : IPA) (1 : 3) for 100 s and then rinsed in IPA for 30 s and blown dry with nitrogen. In addition, all samples were descumed using inductively coupled plasma (ICP) in a 1 : 3 gas mixture of O_2 and Ar for 20 s. The wafers were then sequentially cleaned with 1 : 10 HCl : H_2O solution for 60 s and then rinsed in D.I water for 60 s and blown dry with nitrogen to ensure that the thin oxide layer on the GaAs surface were removed to assure metal adhesion. After development and descum, the photoresist was thermally reflowed using a hotplate on the bottom which ensured the uniform heat transformed to the bottom resist, PMMA. Through optimal reflow temperature and heating time, the resist structures were reflowed to form the nanometer T-gate foot openings without any substantial change to the top P(MMA-MAA) layer and the desired lift-off structure for T-gate formation was maintained. Finally, Ti/Pt/Au Schottky layers were sequentially deposited on the GaAs substrate at a temperature below 50°C by electron gun evaporation with a deposition distance of about 60 cm. After lift-off process, the nanometer T-gates with thickness of about 500 nm were formed on the GaAs substrate.

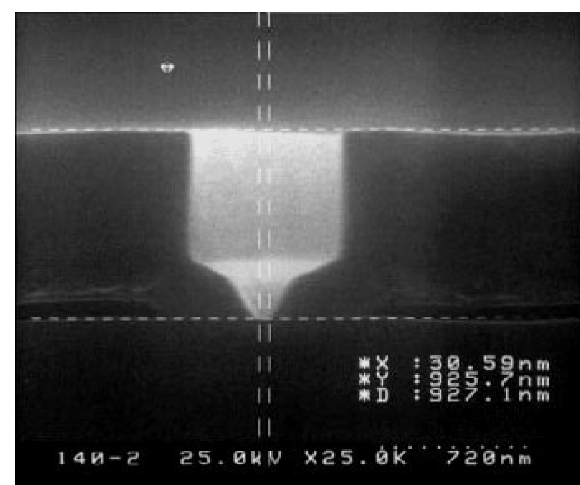
Figures 2(a) to 2(c) are the cross-sectional SEM images of the photoresist and the T-gate formed during the process. Figure 2(a) shows the as-developed bi-layer resist structure with gate length of about 160 nm and resist thickness of about 1000 nm after the photoresist was developed. Figure 2(b) exhibits the thermally reflowed resist configuration. Figure 2(c) is the T-gate formed after lift-off process with thickness of about 500 nm and the gate length at the bottom of the T-shaped gate is 30 nm. As can be seen from the SEM micrographs in Fig. 2, the bottom resist PMMA was successfully shrunk to form the desired footprint opening of about 30 nm without any obvious change on the top P(MMA-MAA) layer.

Figure 3 shows the critical dimension (C.D.) of the observed gate length versus reflow time with different reflow temperatures. As can be seen in this figure, the gate length decreases with increasing thermal reflow time. Furthermore, the reflow temperature also influences the thermal reflow process. When the reflow temperature was 135°C, a highly sensitive relationship ($\sim$ 3.5 nm/s) between gate length and reflow time was observed. However, the high sensitivity of the gate length on the reflow time led to difficult process control and resulted in a small process window. As the reflow temperature was decreased to 115°C, the shrinking effect between gate length and the reflow time was not so significant. Consequently, an optimal reflow temperature of 125°C was chosen for nanometer gate fabrication. In addition, the results of the distributions of the pattern-sizes with different reflow time at a fixed reflow temperature of 125°C are shown in Fig. 4. For each reflow time, the sizes of the gate length were measured at different locations across the 3-inch GaAs wafer. When the reflow time reached 90 s, the openings of the gate length on the GaAs substrate were covered with the reflowed resist which led to the failure in the following lift-off process. By combining the results indicated in Figs. 3 and 4, a lift-off structure with 30-nm opening was achieved with a reflow temperature of 125°C and the reflow time was 75 s in this study.

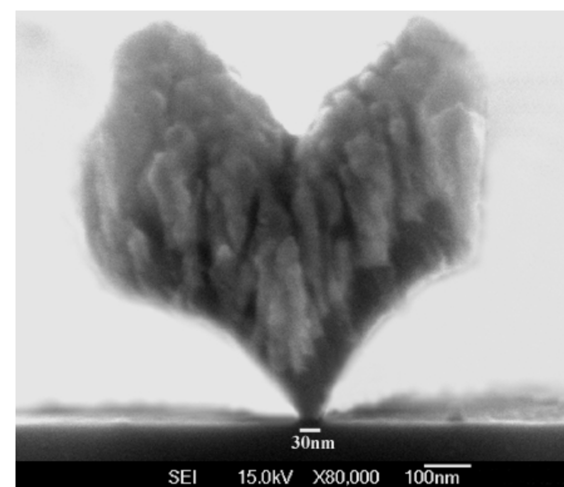
In summary, a novel method for fabricating ultra-short 30-nm T-gate on the GaAs substrate by combining advanced



(a)



(b)



(c)

Fig. 2. SEM cross-sectional images of (a) as-developed resist structure, (b) thermally reflowed resist configuration and (c) 30-nm-T-gate after lift-off.

EB lithography and thermally reflowed resist technique has successfully been demonstrated. The effects of reflow temperature and reflow time on the gate length formed were il-

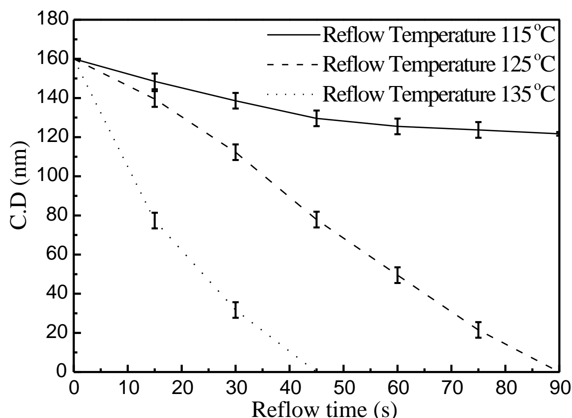


Fig. 3. Dependence of different reflow temperature and reflow time on C.D. of gate length for thermal reflow technique.

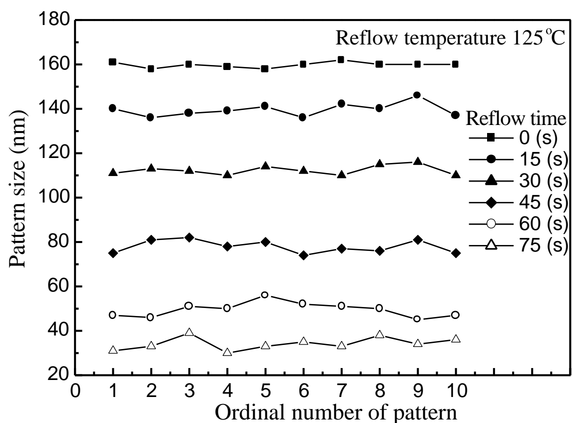


Fig. 4. Distributions of the pattern-sizes across the wafer with different reflow time at a fixed reflow temperature of 125°C (Total 10 data points across the wafer for each reflow time).

lustrated. The typical as-developed 160-nm-T-gate patterns can be easily shrunk to nanometer scale in length ranging from 150 nm to 30 nm after a simple thermal reflow procedure without any substential change to the top layer resist structure of the T-gate. Finally, a 30 nm T-gate was demonstrated using this reflow technique which is the smallest T-gate with the thermally reflowed technique reported in the literature so far and can practically be used in the GaAs monolithic microwave integrated circuit (MMIC) fabrications.

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