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Effects of nitridation of silicon and repeated spike heating on the electrical properties of $SrTiO_3$ gate dielectrics

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Electrical properties of $SrTiO_3$ (STO) gate dielectrics on Si substrates grown by rf-magnetron sputtering were studied. We employed the surface nitridation and repeated spike heating to improve the interfacial properties of STO/Si. The nitrogen was moderately incorporated at the interface by first growing a thin SiON layer and then removing this sacrificial layer before growing STO gate dielectric. The experimental results indicate that this nitridation treatment may retard the formation of thin interfacial layer during the high-temperature growth of STO gate dielectric and consequently decrease the equivalent oxide thickness (EOT) by about 10% toward 24% at various deposition pressures. The STO gate dielectric with this nitridation treatment exhibited slightly lower leakage current at an accumulation region and nearly 2 orders of magnitude lower leakage current at an inversion region. The repeated spike heating technique was also employed to deposit a STO gate dielectric at repeated oscillating temperatures. The results show that this thermal treatment reduced the interfacial trap states and the leakage current was also reduced by about 1 order of magnitude at the same EOT. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1526914]

Following the international technology roadmap of semiconductor, the conventional SiO_2 gate oxide thickness is required to be less than 2 nm in the near future.[1] However, the use of ultrathin SiO_2 gate oxide results in a number of issues,[2] including high gate leakage current, reduced drive current, reliability degradation, boron penetration, uniformity, etc. Any of these effects will fundamentally limit the usefulness of SiO_2 as a gate dielectric. As the oxide thickness is scaled down to below 2 nm, the gate leakage current increases significantly due to the direct tunneling, leading to undesired power consumptions in complementary metal–oxide semiconductor devices. As a result, many high-*k* gate dielectrics have been investigated as potential replacements for SiO_2 to provide a physically thicker film to reduce the leakage current. Among many possible candidates of high-*k* gate dielectrics, $SrTiO_3$ (STO) provides special functions because it can be epitaxially grown on silicon substrate.[3] STO possesses a very large dielectric constant, which is advantageous for the realization of a metal/ferroelectric/insulator/semiconductor (MFIS) structure for the application of 1 T ferroelectric random access memory.[4] In the MFIS structure, the dielectric constant of the insulator should be increased to match that of the ferroelectric material in order to reduce the operation voltages. Moreover, STO is perovskite-type material, which provides a good buffer layer for the growth of perovskite-type ferroelectric thin films. However, it is very difficult to fabricate high-quality STO gate dielectrics because a thin interfacial layer forms due to Si oxidation and interdiffusion at high temperature. The resultant interfacial layer with low permittivity will limit the highest possible gate capacitance or the lowest achievable EOT. Several methods have been employed to improve the interfacial properties. Nitrogen implantation into silicon substrate has been used to grow ultrathin oxide because nitrogen can effectively suppress the growth of silicon oxide.[5] A repeated-spike oxidation technique has been proposed by Hong *et al.*[6,7] to grow ultrathin oxide. The variation of radiation heat absorption in different regions on a wafer could be compensated by repeated-spike heating technique so that temperature uniformity can be improved. Their results also showed that the leakage current is reduced by an order of magnitude. In the present study, we improve the interfacial properties of STO/Si by means of surface nitridation and repeated-spike-heating method. The microstructure, leakage current density, and capacitance of STO gate dielectrics are reported.

Boron-doped *p*-type silicon (100) wafers with 1 to 10 Ω cm resistivity were used as the starting substrates. After a standard Radio Corporation of America clean, an 8 nm SiON film was grown on the silicon wafer at 950 °C in pure N_2O gas in a furnace. For comparison, 8 nm SiO_2 was thermally grown in a pure O_2 ambient as the control sample. After these sacrificial SiON and SiO_2 layers were removed by dipping the wafer in diluted HF solution, the 20 nm STO thin films were deposited on the aforementioned two pretreated substrates by using rf-magnetron sputtering at a substrate temperature of 500 °C. The two samples were grown on a spin substrate holder at the same time for comparison. After the removal of the SiON and SiO_2 sacrificial layer, it can be seen from the x-ray photoelectron spectroscopy profiles of the silicon substrates that the characteristic binding energy of N 1s was slightly increased for the N_2O-pretreatment sample, indicating that nitrogen has been moderately incorporated into the silicon surface.

The repeated-spike-heating technique was carried out by setting the temperature to ramp up and down between 450 and 550 °C for 30 min, while the control sample was held at a constant temperature of 500 °C for the same time. After the

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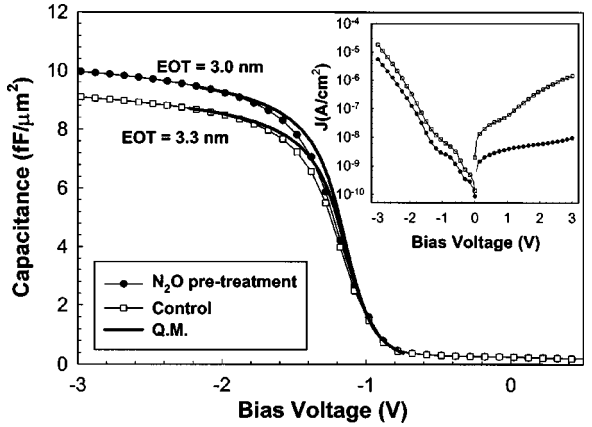

FIG. 1. The high-frequency ($C-V$) curves of control and N_2O pretreatment samples. The inset is the corresponding leakage current density.

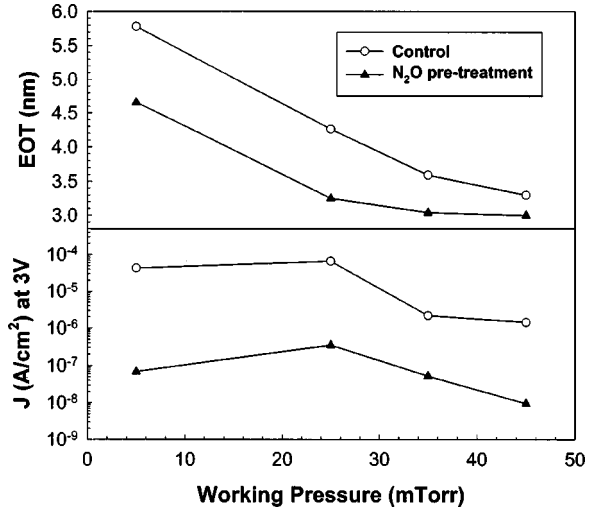

FIG. 3. Variation of EOT and leakage current with working pressure for control and N_2O pretreatment samples.

film depositions, rapid thermal annealing in an N_2 ambient at 650–800 °C was carried out to improve the crystallinity of the films. The thickness of interfacial layer between STO and Si was determined using transmission electron microscopy (TEM). For the electrical measurement, aluminum was used as both the top electrode and backside substrate ohmic contact. The capacitance–voltage ($C-V$) measurements were performed by a HP 4284A LCR meter at 100 K to 1 MHz while the current–voltage ($I-V$) measurements were recorded by a HP 4156A semiconductor parameter analyzer.

The C–V curves showed frequency dispersion during $C-V$ measurement which may be due to extrinsic parasitic inductance and resistance. After being calibrated by four-element model,[8] the $C-V$ curves of the STO gate dielectrics at 45 mTorrr deposition pressure with and without N_2O pretreatment and the quantum-mechanical (QM) fitting curve [9] are shown in Fig. 1. We can observe that the EOT of the N_2O pretreatment sample is smaller than that of the control sample. The reason for this phenomenon is attributed to the nitrogen incorporation in the silicon surface that alleviated the reaction of the silicon surface into low dielectric constant SiO_x thin interfacial layer during the high-temperature growth of STO gate dielectrics. In fact, it shows from TEM images that the thickness of the interfacial layers of the N_2O pretreatment sample and the control sample are 1.9 and 2.6 nm, respectively (Fig. 2). The inset of Fig. 1 shows the corresponding leakage current densities. The N_2O pretreatment sample has leakage current of 2 orders of magnitude lower than that of the control sample at the inversion region (positive bias), while the leakage current of the N_2O pretreatment sample is only 0.5 order of magnitude lower than that of control sample at the accumulation region (negative bias). The reasons may be explained by the following. Previously reported results[10] indicated that the conduction band offset between STO and Si is almost zero. If STO is directly in contact with Si, the leakage current density should be very large. In order to reduce the leakage current, a thin interfacial layer with higher band gap must be employed to increase the barrier height. Since the nitridation can reduce the interdiffusion of STO and Si, the thinner interfacial layer with N_2O pretreatment contains less amounts of Sr or Ti species and is expected to have a larger band gap, resulting in the reduction of leakage current. The effect of increased barrier height is more important in the inversion region than the accumulation region because the electrons flow from Si substrate at positive bias voltage (inversion).

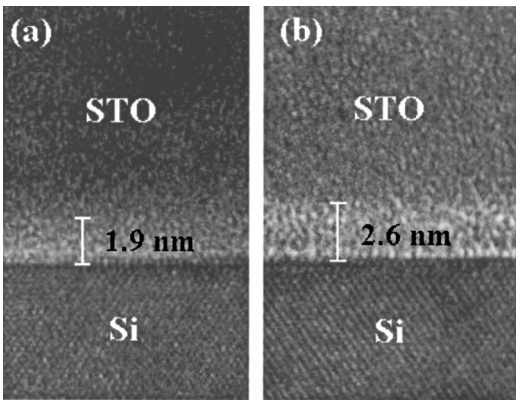

FIG. 2. TEM interface images of (a) N_2O pretreatment sample and (b) control sample.

The EOT and leakage current density at +3 V of 500 °C deposited 20 nm thick STO gate dielectrics at various deposition pressures are shown in Fig. 3. Generally, the EOT decreases with increasing deposition pressure. The main reason may be that the composition of STO thin film is varied with deposition pressures and, consequently, affect the dielectric constant of the thin films. Therefore, the EOT decreases with the increase of deposition pressure for the samples indicated. We can observe that all the N_2O pretreatment samples have a significantly lower EOT than the control samples at various deposition pressures. The variation of the leakage current density with deposition pressure is also illustrated in Fig. 3. The N_2O pretreatment sample has a leakage current density of nearly 2 orders of magnitude lower than that of the control samples at various deposition pressures.

The plots of leakage current density versus EOT for typical and repeated-spike-heating samples are shown in Fig. 4. It is indicated that the repeated-spike-heating samples with the same EOT have leakage current densities of 1–2 orders of magnitude lower than those of typical samples. The reason for the reduction of leakage current may be due to the

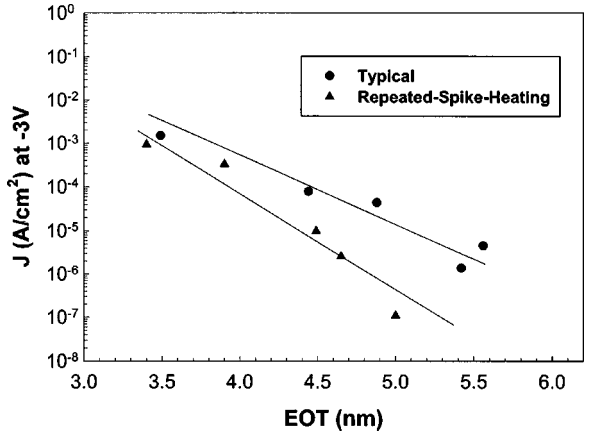

FIG. 4. Plots of leakage current density vs EOT for typical and repeated-spike-heating samples.

smaller interface state density.[11] Figure 5 shows the normalized $C-V$ curves of typical and repeated-spike-heating samples. Theoretical QM simulation[9] accounting for the quantum well corrections for the metal–insulator–semiconductor structure was also provided for comparison. We can observe that the $C-V$ curve of the repeated-spike-heating sample is very close to the theoretical curve, while the $C-V$ curve of a typical sample shows obvious deviation. This result implies that the repeated-spike-heating technique reduces the interfacial trap state of the STO gate dielectric, which is also similar to the previous reported results for ultrathin gate oxide.[6,7] The wagging and stretching of the Si—O bond are temperature dependent. Therefore, during the temperature ramping up and down in the repeated-spike-heating recipe, it is possible that the residual oxygen in films has more of a chance to fill the silicon dangling bonds and thus, a better interface has been formed.

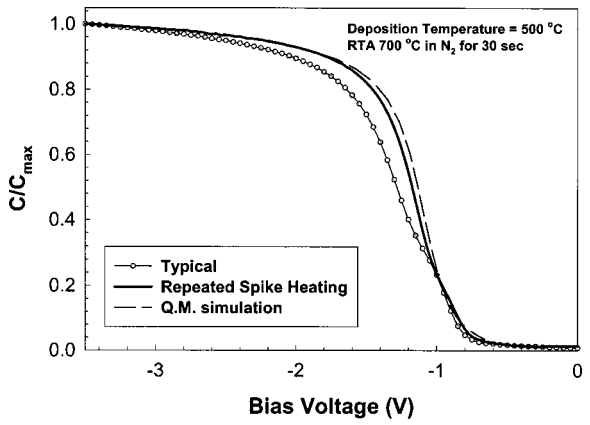

FIG. 5. The normalized $C-V$ curves of typical and repeated-spike-heating samples. The dashed line is the theoretical QM simulation.

In summary, we have proposed a method of surface nitridation of silicon by first growing a sacrificial SiON layer and then removing this layer before growing STO gate dielectrics. The experimental results show that the EOTs of N_2O pretreatment samples were 10%–24% lower than that of the control samples, and the leakage current density was also reduced by 2 orders of magnitude at the positive bias. The results imply that the incorporation of a certain amount of nitrogen into the substrate surface may improve the interfacial properties due to the depression of the formation of the interfacial layer during the high-temperature growth of STO gate dielectrics. In addition, we have incorporated the repeated-spike-heating method to grow STO gate dielectrics. The experimental results show that this technique reduced the interfacial trap states and the leakage current density by 1 order of magnitude compared to constant temperature deposited films.

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