Hot-Carrier-Induced Degradation for Partially Depleted SOI 0.25–0.1 μm CMOSFET With 2-nm Thin Gate Oxide

Wen-Kuan Yeh, *Member, IEEE*, Wen-Han Wang, Yean-Kuen Fang, Mao-Chieh Chen, and Fu-Liang Yang

***Abstract*—Hot-carrier-induced degradation of partially depleted SOI CMOSFETs was investigated with respect to body-contact (BC-SOI) and floating-body (FB-SOI) for channel lengths ranging from 0.25 down to 0.1 μm with 2 nm gate oxide. It is found that the valence-band electron tunneling is the main factor of device degradation for the SOI CMOSFET. In the FB-SOI nMOSFET, both the floating body effect (FBE) and the parasitic bipolar transistor effect (PBT) affect the hot-carrier-induced degradation of device characteristics. Without apparent FBE on pMOSFET, the worst hot-carrier stress condition of the 0.1 μm FB-SOI pMOSFET is similar to that of the 0.1 μm BC-SOI pMOSFET.**

***Index Terms*—Hot-carrier effect, hot-carrier-induced degradation, partially depleted SOI.**

I. Introduction

SILICON-ON-INSULATOR (SOI) CMOS devices are attractive since they provide full dielectric isolation and reduced junction capacitance as compared to bulk-Si devices. Partially depleted SOI (PD-SOI) devices, in which threshold voltages are decoupled from silicon film thicknesses [1], are preferable for high-performance applications because of their better feasibility of scaling and manufacture. However, the large drop in threshold voltage at high drain biases due to the floating-body effect (FBE) remains to be a critical issue regarding the use of PD-SOI devices. The body-contact (BC) configuration is one of the most effective and practical methods of suppressing the FBE [2]. Thus, body-tie is necessary for the suppression of FBE, especially for the I/O logic circuit. As devices are scaled down, SOI MOSFETs also suffer from the hot-carrier effect (HCE). Thus, a study on hot-carrier injection is needed for the prediction of the long-term reliability of MOSFETs. The relevant operation regimes for HCE in conventional bulk-Si devices are the maximum substrate current (with $V_G \approx V_D/2$) and the maximum gate current (with $V_G = V_D$) [3], [4]. However, HCE in SOI devices is more complex than that in bulk devices because of the parasitic bipolar transistor effect (PBT) and FBE [5]. Reduction in dimensions of the deep submicron MOSFET could further deteriorate these problems, including the increase in transistor electric fields. High fields provide sufficient energy to channel carriers and enhance the impact ionization rate, increasing the PBT current gain and the impact ionization multiplication factor. Moreover, as the gate oxide thickness is scaled down to a thickness less than 3 nm, the direct tunneling current and the oxide reliability problem become important issues of concern. There are a number of studies about the reliability of 0.1 μm SOI devices [6]–[8], but few studies are reported regarding the devices with ultra-thin gate-oxide of less than 3 nm. This work investigates the HCE in 0.1 μm partially depleted SOI CMOSFET with 2 nm gate-oxide. The hot-carrier-induced degradation of device characteristics is investigated for the devices with a channel length ranging from 0.25 down to 0.1 μm with respect to body-contact SOI (BC-SOI) MOSFET and floating-body SOI (FB-SOI) MOSFET.

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W.-K. Yeh is with the Department of Electrical Engineering, National University of Kaohsiung, Kaohsiung, Taiwan, R.O.C (e-mail: wkyeh@nuk.edu.tw).

W.-H. Wang and Y.-K. Fang are with the VLSI Technology Laboratory, Institute of Microelectronics, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, R.O.C.

M.-C. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

F.-L. Yang is with the Exploratory Device Department, Device Engineering Division, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C.

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II. Experiments

PD-SOI CMOSFET devices on IMplanted OXygen (SIMOX) SOI substrate were fabricated with 190 nm thick Si active layer and 150 nm thick buried oxide (BOX). A 0.1 μm dual poly-Si gate technology was employed for the formation of 2 nm nitride gate oxide grown by rapid thermal oxidation in NO ambient, composite oxide/SiN spacers via low-temperature processing, and junctions via arsenic (As) and boron (B) ion implantations. After $CoSi_2$ salicidation, devices were metalized using a typical backend flow. To investigate the HCE, device stressing and measurements were made on a probe station at various drain voltages ($V_D = 1.2$–2.4 V) and gate voltages ($V_G = 0$–2.4 V) with a stressing time ranging from 0 to 100 min.

III. Results and Discussion

A. An 0.1 μm BC-SOI nMOSFET Versus 0.1 μm FB-SOI nMOSFET

Fig. 1 shows the I_D-V_D characteristic of 0.1 μm BC-SOI and FB-SOI nMOSFETs before and after a hot carrier stress under constant drain and gate voltages ($V_D = V_G = 2.4$ V) for 100 min. The FBE occurred in the FB-SOI devices [Fig. 1(b)], while it can be suppressed in the BC-SOI devices by the body contact [Fig. 1(a)] using a T-gate structure with contact

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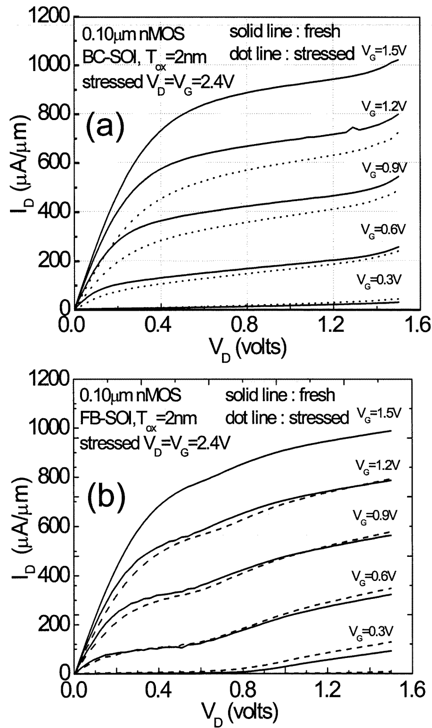

Fig. 1. Drain current versus drain voltage (I_D–V_D) characteristics for (a) 0.1 μm BC-SOI and (b) 0.1 μm FB-SOI nMOSFETs before and after a voltage stress at $V_D = V_G = 2.4$ V for 100 min.

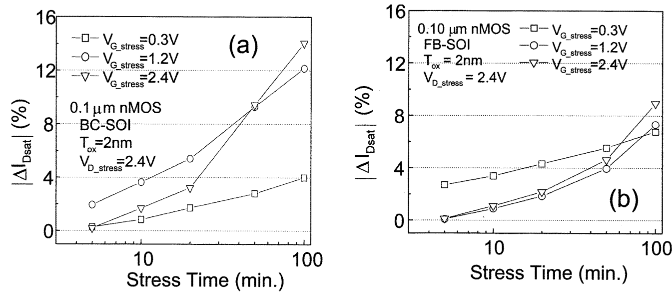

Fig. 2. Saturated drain current ($I_{D\rm sat}$) degradation as a function of stress time under a drain voltage of $V_D = 2.4$ V and various gate voltages for (a) 0.1 μm BC-SOI and (b) 0.1 μm FB-SOI nMOSFET.

terminals placed in the channel-width direction on the source or drain side [9]. It is apparent that the saturated drain current ($I_{D\rm sat}$) was degraded after the 100 min stressing and the hot-carrier-induced $I_{D\rm sat}$ degradation of BC-SOI was larger than that of FB-SOI. Fig. 2 shows the time-dependent $I_{D\rm sat}$ degradation for the 0.1 μm BC-SOI and FB-SOI nMOSFETs, stressed by a constant drain voltage ($V_D = 2.4$ V) and various gate voltages. In the BC-SOI devices, it can be seen that initially $V_G = V_D/2$ yields a higher change in $I_{D\rm sat}$, then the highest gate voltage stress ($V_G = V_D$) resulted in the largest final degradation of $I_{D\rm sat}$ after the 100 min stressing [Fig. 2(a)]. It has been reported that the hot-carrier-induced degradation of 0.1 μm bulk nMOSFETs under $V_G = V_D$ stress is more serious than that occurring under $V_G \sim V_D/2$ stress [4]. For the 0.1 μm device, hot channel electrons are confined closer to the Si surface at higher V_G values, which leads to greater Si surface damage. As with bulk devices, the hot-carrier-induced degradation in the 0.1 μm BC-SOI nMOSFET is due primarily to the interface state generation. In the thin-oxide devices ($T_{\rm ox} < 3$ nm), channel holes are also created at higher V_G values due to the valence-band electron tunneling [10]; these generated holes promote the probability of recombination with electrons in the channel region and transfer the excess energy to the other conduction electrons, accelerating hot electron tailing and interface trap generation rate. Thus, greater initial $I_{D\rm sat}$ degradation in the BC-SOI nMOSFET occurred at maximum substrate current $I_{\rm sub}$ when $V_G \sim V_D/2$ due to impact ionization, while higher valence-band electron tunneling occurred apparently when $V_G = V_D$, which enhanced the interface generation rate and finally resulted in the largest $I_{D\rm sat}$ degradation, as shown in Fig. 2(a). When FBE was present in the FB-SOI nMOSFET, $I_{D\rm sat}$ degradation at first did not occur at maximum gate current I_G ($V_G = V_D$) or at maximum $I_{\rm sub}(V_G \sim V_D/2)$, but occurred when $V_G \sim V_T$, as shown in Fig. 2(b). Electron and hole injection occurred at low gate voltage ($V_G \sim V_T$) because of the PBT effect [11]. The PBT action generated hot holes by impact ionization, resulting in interface defect generation. Bipolar injection can induce greater interface state density than pure electron injection. Thus, initially $V_G = V_T$ yielded a higher change in $I_{D\rm sat}$, however, the largest interface generation rate occurred at $V_G = V_D$ due to the valence-band electron tunneling, resulting in finally the largest degradation in $I_{D\rm sat}$. Thus, the stressing condition of $V_G = V_D$ resulted in the largest degradation in $I_{D\rm sat}$ after the 100 min stressing for both 0.1 μm BC-SOI and FB-SOI nMOSFETs.

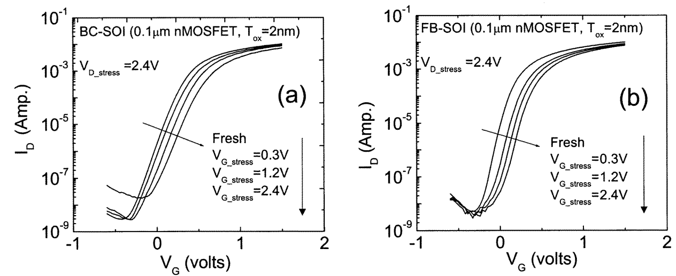

Fig. 3. Drain current as a function of gate voltage for (a) 0.1 μm BC-SOI and (b) 0.1 μm FB-SOI nMOSFETs before and after a hot carrier stress for 100 min at $V_D = 2.4$ and various gate voltages.

Fig. 3 shows the subthreshold swing and gate-induced drain leakage (GIDL) in the 0.1 μm SOI nMOSFET before and after various hot carrier stresses. After the hot carrier stress, the subthreshold swing exhibited degradation and the degradation apparently became more serious as the gate stress was increased. The swing degradation indicates the creation of interface traps resulting in a threshold voltage shift [Fig. 3(a)] [6]. The GIDL in the BC-SOI nMOSFET at a negative gate bias of $V_G = -0.6$ V also increased with the gate voltage stress. It has been reported that GIDL is a direct result of the generation of interface states [12]; thus, the largest degradation in $I_{D\rm sat}$ coincides with the largest increase in interface state density. For the FB-SOI nMOSFET, the subthreshold swing was also degraded after the stress and the degradation also became more pronounced as the gate stress was increased, similar to the behavior of the BC-SOI nMOSFET, as shown in Fig. 3(b). Moreover, the PBT and impact ionization effects also affected the subthreshold slope substantially, leading to the degradation of the device's hot-carrier

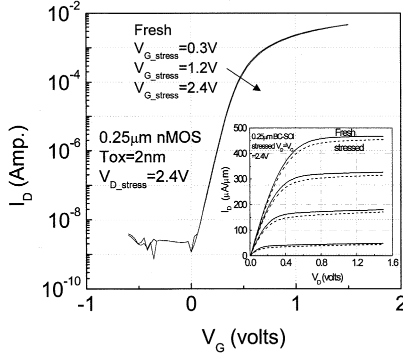

Fig. 4. Transfer characteristics (I_D–V_G) for a 0.25 μm SOI nMOSFET before and after various hot-carrier stresses. The inset in the figure shows the output characteristics (I_D-V_D).

performance [13]. However, GIDL of the FB-SOI devices decreased only slightly with the increasing gate stress. It is believed that the potential difference between substrate and drain in the FB-SOI nMOSFET is reduced due to the FBE; thus, GIDL is suppressed as the gate stress is increased.

B. Long Channel BC-SOI nMOSFET Versus 0.1 μm BC-SOI nMOSFET

Fig. 4 shows the transfer characteristics (I_D-V_G) and the output characteristics (I_D-V_G) for a 0.25 μm BC-SOI nMOSFET before and after various hot carrier stresses. It can be seen that the voltage stress resulted in a smaller degradation in the output current (drain current I_D) and that the subthreshold swing remained nearly unchanged following the stresses, as compared with those observed in the 0.1 μm BC-SOI nMOSFET [Fig. 1(a) and Fig. 3(a)]. In general, when a transistor is stressed by hot carrier injection, the maximum transconductance ($\mathrm{Gm_{max}}$) degradation is mainly associated with the trapped charges and the creation of defect states at the Si/SiO_2 interface [5]. Fig. 5 shows the hot-carrier-induced degradation on transconductance for the 0.25 μm and 0.1 μm BC-SOI nMOSFETs. It is obvious that the devices with a shorter channel resulted in a larger degradation after the gate stress. In fact, as the device channel length is scaled down to 0.1 μm, hot-carrier-induced transconductance degradation becomes very serious. The scaling down of the device dimension increases the electric field in the transistors and thus aggravates the hot carrier effect, because the high field provides a large amount of energy to the channel carriers and thus enhances the impact ionization rate and the creation of interface defect states. The inset in Fig. 6 shows the substrate current (I_{SUB}) as a function of gate voltage (V_G) for the BC-SOI nMOSFETs with different channel length. For the device of 0.25 μm channel length, the worst stress condition with maximum I_{sub} happened for maximum impact ionization ($V_G \approx V_D/2$); thus, the maximum $I_{D\mathrm{sat}}$ degradation of this device occurred at $V_G \approx V_D/2$, as shown in Fig. 6. However, for the device of 0.1 μm channel length, the maximum I_{sub} is more easily found at $V_G \approx V_D$ because the charge carriers not only need sufficiently high energy but they also have to bombard the Si/SiO_2 interface to generate the interface states. Fig. 7 shows that the hot-carrier-induced device's gate leakage

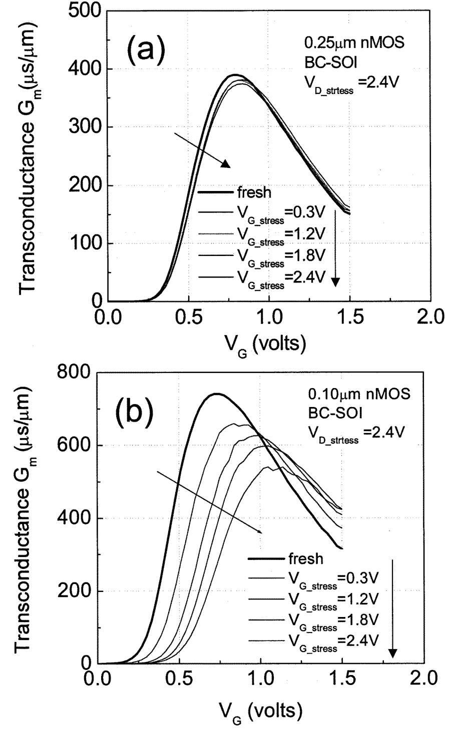

Fig. 5. Transconductance (G_m) as a function of gate voltage (V_G) for (a) 0.25 μm and (b) 0.1 μm BC-SOI nMOSFET stressed with $V_D = 2.4$ V and various gate voltages.

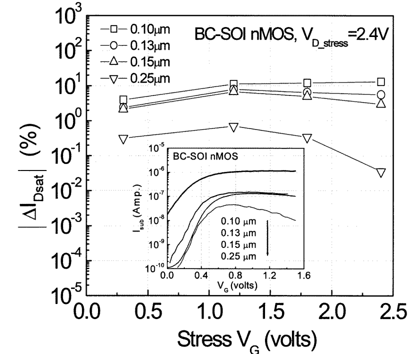

Fig. 6. Saturated drain current ($I_{D\mathrm{sat}}$) degradation as a function of stress gate voltage (V_G) for BC-SOI nMOSFETs with different channel length. The inset in the figure shows the substrate current (I_{sub}) as a function of gate voltage for BC-SOI nMOSFETs with different channel lengths.

increases with stress gate voltage, implying that the gate tunneling will enhance the device degradation. Similar to the bulk device, hot-carrier-induced $I_{D\mathrm{sat}}$ degradation of the 0.1 μm BC-SOI device at $V_G = V_D$ stress is more serious than that at $V_G \sim V_D/2$. Fig. 8 shows the dependence of impact ionization (I_{SUB}/I_D) on channel length for the SOI nMOSFET. For long channel device, the maximum impact ionization rate occurs at $V_G = V_D/2$ with maximum I_{sub}. In deep submicron device ($L_G < 0.15$ μm), the maximum impact ionization rate occurs at $V_G = V_D$ with maximum gate tunneling. Thus for thin oxide (<3 nm), the valence-band electron tunneling will enhance the device degradation for the BC-SOI nMOSFET in the worst case of HCE. The device lifetime (τ) can be predicted by the following logarithmic law [5]

$$\ln(\tau) \propto \exp(\beta/V_d)$$

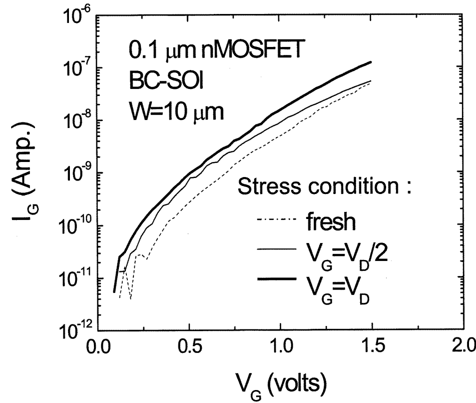

Fig. 7. Gate current (I_G) as a function of gate voltage (V_G) for 0.25 μm SOI nMOSFETs before and after different stressing.

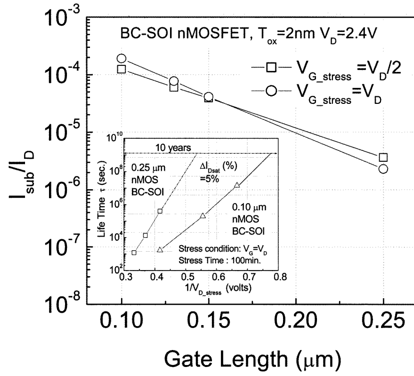

Fig. 8. I_{sub}/I_D as a function of channel length for stress BC-SOI nMOSFETs with different stressing conditions. The inset in the figure shows the device lifetime as a function of stress drain voltage for two different channel lengths.

where V_d is applied drain voltage. The device lifetime, defined at 5% $I_{D\mathrm{sat}}$ degradation, versus $1/V_{d_\mathrm{stress}}$ is shown in the inset in Fig. 8 for the 0.25 μm and 0.1 μm BC-SOI nMOSFETs. In this work, lifetime larger than ten years can be obtained at $V_D < 1.9$ V stress for the 0.25 μm device, and at $V_D < 1.3$ V stress for the 0.1 μm device. In general, it is more safe to stress the 0.1 μm BC-SOI nMOSFET with a drain voltage of 1 V.

C. An 0.1 μm BC-SOI pMOSFET Versus 0.1 μm FB-SOI pMOSFET

For the 0.1 μm FB-SOI pMOSFET, FBE is insignificant because of lower hole mobility and thus negligible impact ionization. Thus, there is no obvious difference of hot-carrier-induced $I_{D\mathrm{sat}}$ degradation between the BC-SOI and the FB-SOI pMOSFETs, as shown in the insets of Fig. 9. Fig. 9 also shows that there is no apparent hot-carrier-induced subthreshold swing degradation for both 0.1 μm SOI devices. The time dependent degradation in $I_{D\mathrm{sat}}$ for both SOI pMOSFETs was also investigated. The worst stress condition on the 0.1 μm BC-SOI pMOSFET occurred for $V_G = V_D$, as shown in Fig. 10(a), which is presumably due to higher valence-band hole tunneling, resulting in an enhanced interface generation rate and thus maximum $I_{D\mathrm{sat}}$ degradation. Without obvious FBE, the maximum hot-carrier-induced $I_{D\mathrm{sat}}$ degradation of the 0.1 μm FB-SOI pMOSFET also occurred on $V_G = V_D$, as shown in Fig. 10(b).

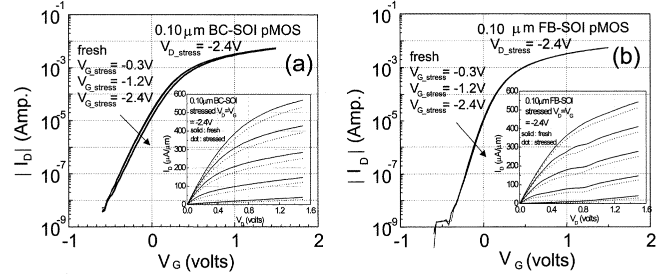

Fig. 9. Drain current as a function of gate voltage and drain voltage (inset figure) for (a) 0.1 μm BC-SOI and (b) 0.1 μm FB-SOI pMOSFETs before and after a hot carrier stress for 100 min at $V_D = -2.4$ V and various gate voltage.

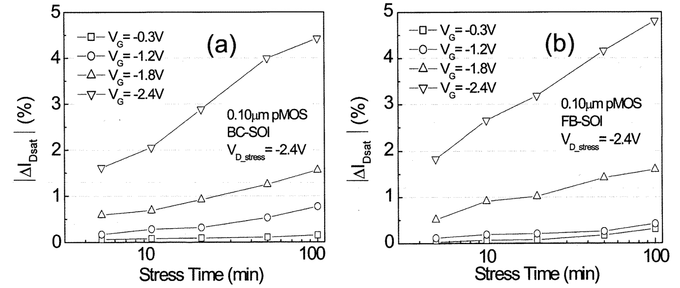

Fig. 10. Saturated drain current $(I_{D\mathrm{sat}})$ degradation as a function of stress time under various gate voltage (V_G) stresses for 0.1 μm (a) BC-SOI and (b) FB-SOI pMOSFET.

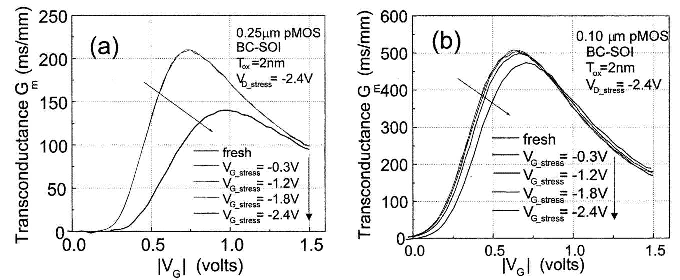

Fig. 11. Transconductance (G_m) as a function of gate voltage (V_G) for (a) 0.25 μm and (b) 0.1 μm BC-SOI pMOSFETs with different stress conditions.

Thus, the worst stress condition is nearly same for both the 0.1 μm FB-SOI and 0.1 μm BC-SOI pMOSFETs.

D. Long Channel BC-SOI pMOSFET Versus 0.1 μm BC-SOI pMOSFET

Transconductance (G_m) as a function of gate voltage for the 0.25 μm and 0.1 μm BC-SOI pMOSFETs with different stress conditions was observed, as shown in Fig. 11. There is no apparent device degradation until significant gate oxide tunneling occurred in the devices. Fig. 12 shows the hot-carrier-induced gate leakage as a function of gate voltage before and after $V_D = V_G$ stressing for the 0.1 μm BC-SOI pMOSFET. It is apparent that the gate leakage increased with gate voltage and decreased with drain voltage. Thus, larger gate leakage occurred after hot carrier (hole) stressing, which enhances the device degradation. Fig. 13 shows the $I_{D\mathrm{sat}}$ degradation as a function of stressing gate voltage V_G for the SOI pMOSFET with different channel length. For the channel length of 0.25–0.1 μm devices, maximum $I_{D\mathrm{sat}}$ degradation always occur at maximum I_G when $V_G = V_D$ because of the creation of maximum amount

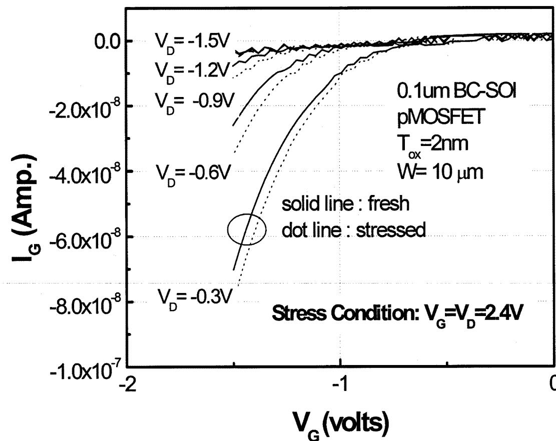

Fig. 12. Gate current (I_G) as a function of gate voltage (V_G) for 0.1 μm SOI pMOSFETs before and after stressing.

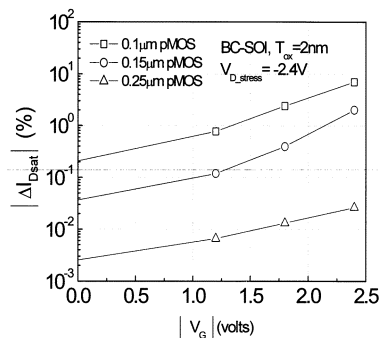

Fig. 13. Saturated drain current $(I_{D\mathrm{sat}})$ degradation as a function of stressing gate voltage (V_G) for BC-SOI pMOSFET with different channel length.

of interface states. For the pMOSFET, the charge carriers need sufficiently high energy to bombard the Si/SiO_2 interface; thus, interface states are more easily generated at maximum I_G for the 0.25–0.1 μm BC-SOI pMOSFETs, and the worst stress condition occur always at $V_G = V_D$.

IV. Conclusion

This work investigates the hot-carrier-induced degradation on current driving capacity and subthreshold characteristics of CMOSFETs with respect to the BC-SOI and FB-SOI devices with 2 nm thin gate-oxide. For the BC-SOI nMOSFET, the interface defect states created by valence-band electron tunneling is the major origin of the hot-carrier-induced $I_{D\mathrm{sat}}$ degradation on $V_G = V_D$. In the 0.1 μm FB-SOI nMOSFET, hole generation is suppressed by the FBE during electron tunneling; thus, $I_{D\mathrm{sat}}$ degradation occurs initially when $V_G = V_T$ due to the PBT effect, while the maximum $I_{D\mathrm{sat}}$ degradation occurs finally at $V_G = V_D$ because of the valence-band electron tunneling. For the FB-SOI pMOSFET, the impact ionization is not obvious because of the lower channel hole mobility; thus, FBE is not significant and has no apparent impact on the hot carrier effect. Experimental results shows that the maximum hot-carrier-induced $I_{D\mathrm{sat}}$ degradation occurred on $V_G = V_D$ for both 0.1 μm BC- and FB-SOI pMOSFETs.

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Wen-Kuan Yeh (M'00) received the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., in 1990, and the Ph.D. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1996.

From 1996 to 2000, he was with United Microelectronic Corporation Technology & Process Development Division as Member of Research Staff, to research and develop logic, embedded DRAM, SOI, and 0.1 μm transistor tech-applications. He is currently Associate Professor of electrical engineering, National University of Kaohsiung, Taiwan. His recent work is in the field of reliability on SOI and sub-0.1 μm devices. He has authored or coauthored over 30 papers and holds over 60 patents.

Wen-Han Wang received the B.S. and M.S. degrees in electronics engineering from National Cheng Kung University, Taiwan, R.O.C., in 2002. His recent work is in the field of reliability on SOI devices.

Yean-Kuen Fang received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1957 and 1959, respectively, and the Ph.D. degree in semiconductor engineering from the Department of Electrical and Computer Engineering, National Cheng Kung University (NCKU), Taiwan, in 1981.

From 1960 to 1978, he was a Senior Designer and Research Engineer in the private sector. From 1978 to 1980, he was an Instructor, then became an Associate Professor in 1981 and a Professor in 1986, in the Department of Electrical and Computer Engineering, NCKU.

Dr. Fang is a member of Phi Tau Phi.

Mao-Chieh Chen was born in Tainan Hsien, Taiwan, R.O.C., in 1939. He received the B.S. degree from National Taiwan University, Taipei, in 1961, the M.S. degree from National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1963, and the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, in 1969, all in electrical engineering.

In 1969, he joined the General Motors Research Laboratories, Warren, MI, where his work had been concerned with research and development of semiconductor devices. In 1973, he was appointed as a Professor at the Department of Material Science and Engineering, National Tsing Hua University, Taiwan. In 1974, he joined the faculty of the NCTU as a Professor in the Department of Electronics Engineering. He is presently interested in the studies of Cu/low-κ interconnect problem (including Cu-CVD) as well as metal silicides and high-κ dielectric relevant to VLSI application. In addition, he also served as a Visiting Scientist at the IBM T. J. Waston Research Center, Yorktown Heights, NY (1977–1978), and the Microelectronics Center of North Carolina, Research Triangle Park (1985–1986).

Fu-Liang Yang received the B.S. degree from National Tsing Hua University, Taiwan, R.O.C., in 1989, and the Ph.D. degree from Cambridge University, U.K., in 1994, both in materials science and engineering.

From 1994 to 2000, he served as Process Engineer, Integration Coordinator, and Device Manager with Vanguard International Semiconductor Corporation, working on DRAM manufacturing and development. Since 2000, he has performed exploratory research with Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), Hsinchu, Taiwan, for advanced Logic device and material study. He is currently managing a department responsible for SOI implementation development. He holds over 50 patents for CMOS technology.