$La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs With High Hole Mobility and Good Device Characteristics

C. H. Huang, S. B. Chen, and Albert Chin, *Senior Member, IEEE*

***Abstract*—We have studied the high-k La_2O_3 p-MOSFETs on $Si_{0.3}Ge_{0.7}$ substrate. Nearly identical gate oxide current, capacitance density, and time-dependent dielectric breakdown (TDDB) are obtained for La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ devices that indicate the excellent $Si_{0.3}Ge_{0.7}$ quality without any side effect. The measured hole mobility in nitrided La_2O_3/Si p-MOSFETs is 31 cm^2/V-s and comparable with published data in nitrided HfO_2/Si p-MOSFETs. In sharp contrast, a higher mobility of 55 cm^2/V-s is measured in $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET, which is improved by 1.8 times as compared with La_2O_3/Si control devices. The high mobility in $Si_{0.3}Ge_{0.7}$ p-MOSFET gives another step for integrating high-k gate dielectrics into VLSI process.**

***Index Terms*—High-k, hole mobility, La_2O_3, SiGe.**

I. Introduction

ALTHOUGH high-k gate dielectrics [1]–[5] have been proposed for possibly replacing SiO_2 or Si_3N_4, the smaller mobility in high-k MOSFET is still an important concern that may reduce the required high on-state drive current (I_{ON}). The mobility degradation is greater in p-MOSFET than n-MOSFET because of the larger hole effective mass, which becomes more serious after surface nitridation but is needed for maintaining the small equivalent oxide thickness (EOT) during thermal cycle [2]. One method to improve the hole mobility is to use SiGe channel, but unfortunately, the conventional UHVCVD-grown SiGe faces the strain relaxation related poor surface, large junction leakage, and degraded MOSFET performance after subsequent thermal cycle [6]–[9]. Recently, we have developed a high-temperature stable SiGe process [10], and good gate oxide integrity, small silicide junction leakage current, higher hole mobility, and better p-MOSFET characteristics than Si counterparts have been demonstrated [11]–[14]. In this letter, we have further integrated the high-temperature stable SiGe with high-k La_2O_3. We have achieved a hole mobility of 55 cm^2/V-s in nitrided $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET that is 1.8 times higher than the 31 cm^2/V-s mobility in nitrided La_2O_3/Si control p-MOSFET. The improved mobility is important to realize high-k dielectric integration into VLSI technology.

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The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: achin@cc.nctu.edu.tw).

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II. Experimental

Standard 4-in (100) n-type Si wafers with 1∼2 Ω-cm resistivity (5×10^{15}∼1×10^{16} cm^{-3} concentration) were used in this work. After device isolation and modified RCA clean, the amorphous Ge layer is selectively deposited on the active region. An HF-vapor passivation is used to suppress the native oxide formation before Ge deposition [10]–[14]. After rapid thermal annealing (RTA) at 900 °C, a 350 Å single crystal $Si_{0.3}Ge_{0.7}$ was formed by solid-phase epitaxy in the active region, as confirmed by X-ray diffraction, electron diffraction pattern, and cross-sectional transmission electron microscopy (TEM) [10]. The formed SiGe may be strain-relaxed, since it was formed at high temperature. Then, the source-drain p^+ region was formed by implantation followed by a 950 °C RTA [11]. The La_2O_3 gate oxide of ∼60 Å was formed by depositing La and oxidation and measured by ellipsometer. More detailed $Si_{0.3}Ge_{0.7}$ and La_2O_3 characterization can be found in our previous study [4], [5], [10]–[14]. Next, NH_3 nitridation was performed at ∼550 °C before gate electrode formation. The p-MOSFETs and MOS capacitors were fabricated using Al as gate electrode and characterized by I–V and C–V measurements. In addition to $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs, La_2O_3/Si control devices were also fabricated as references.

III. Results and Discussion

Fig. 1(a) and (b) shows the J_G–V_G characteristics and cumulative time-dependent dielectric breakdown (TDDB) of both $La_2O_3/Si_{0.3}Ge_{0.7}$ and La_2O_3/Si p-MOSFETs, respectively. The almost identical gate current suggests the $Si_{0.3}Ge_{0.7}$ channel has little negative effect as compared with the Si case. The same gate current is due to nearly the same work function of Si and SiGe [15] and conduction band difference between La_2O_3 and Si or SiGe. The comparable gate oxide integrity is also evidenced from the nearly identical TDDB for La_2O_3 on Si or SiGe.

We have further measured the quasi-static and high-frequency (100 KHz) C–V characteristics of both La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs and the results are shown in Fig. 2. The identical accumulation capacitance and the same small 10 meV hysteresis measured for both devices indicate that the using SiGe does not have any side effect. An EOT of ∼16 Å is measured with a leakage current of 1.5×10^{-4} A/cm^2 at 1 V that is four orders of magnitude lower than SiO_2 at the same EOT. The smaller flat band voltage in $La_2O_3/Si_{0.3}Ge_{0.7}$ devices may be due to the smaller energy bandgap, which gives additional flexibility to tune V_T.

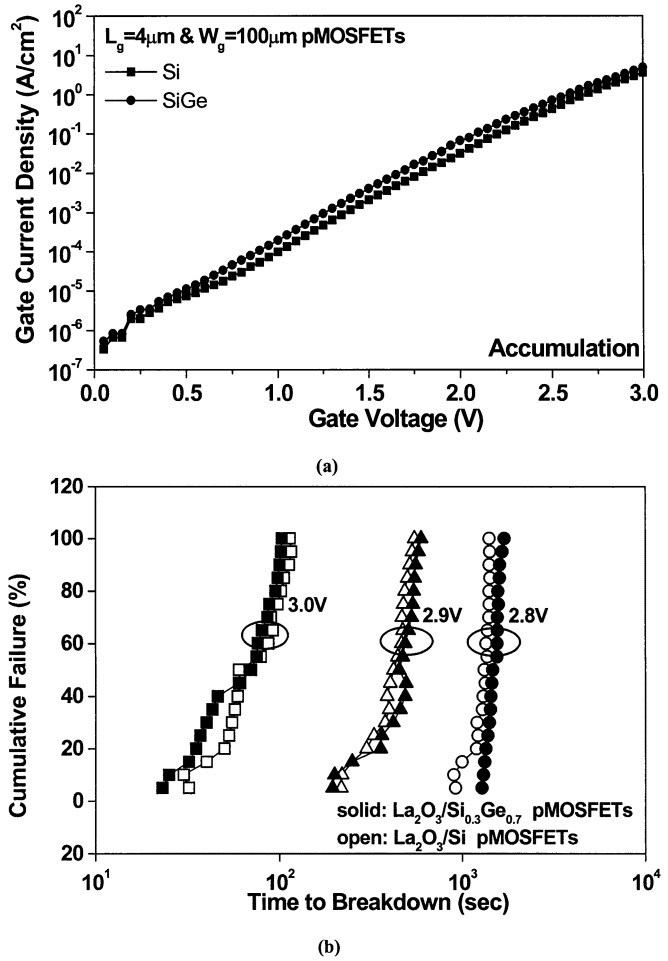

Fig. 1. (a) Gate leakage current and (b) cumulative TDDB of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs under positive gate bias.

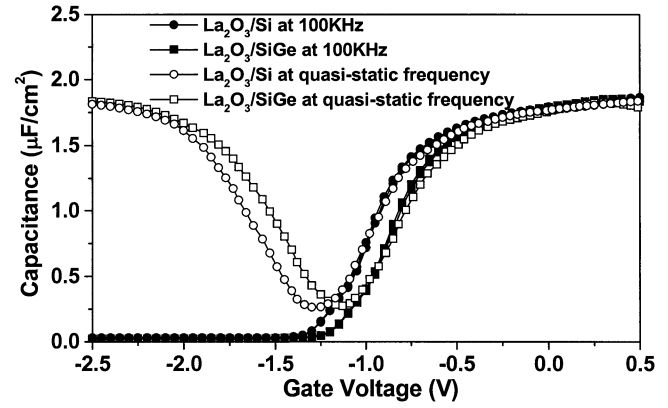

Fig. 2. C–V characteristics of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ MOS capacitors.

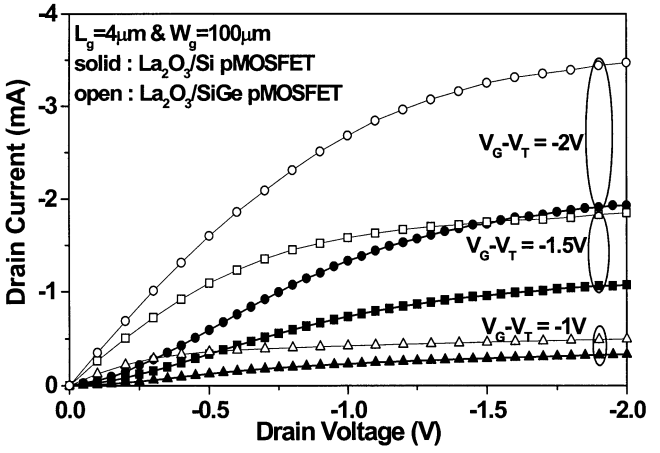

Fig. 3. I_D–V_D characteristics of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs.

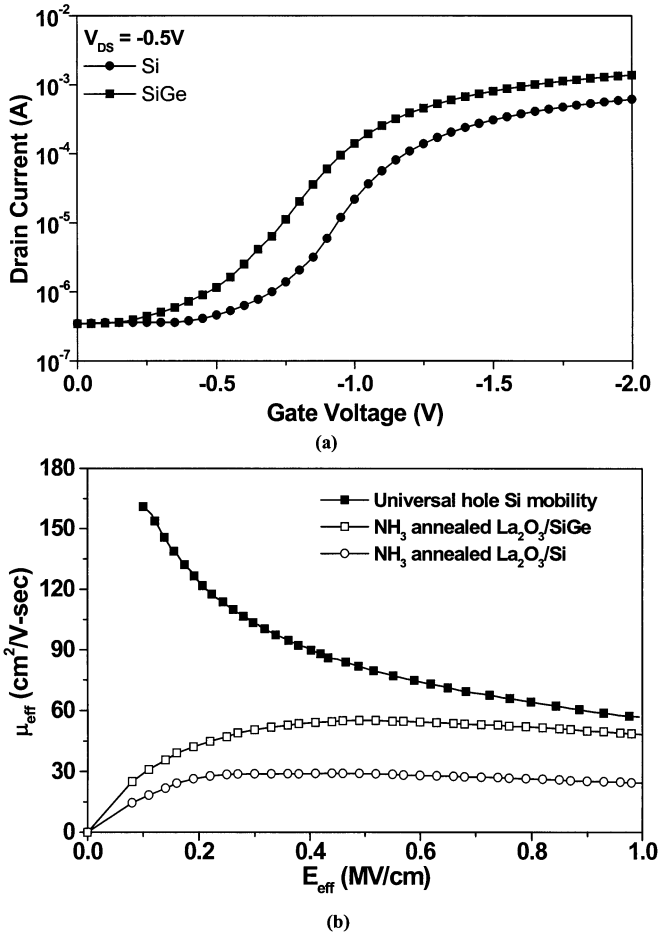

Fig. 4. (a) I_D–V_G characteristics and (b) the hole mobility of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs.

Fig. 3 shows the I_D–V_D characteristics of 4 μm La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs plotted at the same V_G–V_T. Although a relatively large junction leakage of 1×10^{-7} A/cm^2 is measured, it can be lowered to 1×10^{-8} A/cm^2 using Ni gemeno-silicide, which was used in our previous study [14]. In addition to the good device I–V characteristics, the $Si_{0.3}Ge_{0.7}$ has $\sim$2 times higher current driving capability than the Si device at the same V_g of -2 V. Because the La_2O_3 was formed on Si and $Si_{0.3}Ge_{0.7}$ on the same lot with identical inversion capacitance in Fig. 2, the higher hole current is not due to the different gate dielectric. The significantly higher hole current is especially important for high-speed circuit application, which is the fundamental motivation for continuously scaling down.

Because the improved hole current may come from both higher mobility and threshold voltage (V_T) difference, we have further measured the transfer I_D–V_G characteristics. Fig. 4(a)

and (b) shows the I_D–V_G and hole effective mobility for both La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs, respectively, where the V_T difference is also included for the mobility extraction. In addition to having a higher saturation hole current than La_2O_3/Si devices, the $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs have the same off-state current (I_{OFF}) and lower V_T. The lower V_T in the $La_2O_3/Si_{0.3}Ge_{0.7}$ device is due to the smaller energy bandgap in $Si_{0.3}Ge_{0.7}$. In addition to the small V_T difference of 0.2 V, the large hole current improvement is primary coming from the higher mobility using $Si_{0.3}Ge_{0.7}$. A peak hole mobility of 31 cm^2/V-s is obtained in the nitrided La_2O_3/Si p-MOSFET that is comparable with nitrided HfO_2/Si [2]. In sharp contrast, the $La_2O_3/Si_{0.3}Ge_{0.7}$ device has a higher hole mobility of 55 cm^2/V-s that is 1.8 times higher than the La_2O_3/Si control devices without using SiGe. In addition to the comparable gate oxide integrity and I_{OFF}, the higher mobility and I_{ON} indicate that the superior device performance can be realized in nitrided high-k La_2O_3 p-MOSFETs using solid-phase epitaxy formed SiGe.

IV. Conclusion

In addition to the almost identical gate oxide leakage current, capacitance density, TDDB, and I_{OFF}, we have achieved a $\sim$2 times higher I_{ON} and high hole mobility of 55 cm^2/V-s in nitrided $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs. The improved hole mobility in the $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET gives another step to realize high-k gate dielectrics for VLSI integration.

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