

Effect of CF₄ Plasma Pretreatment on Low Temperature Oxides

Tzu Yun Chang, Hsiao Wei Chen, Tan Fu Lei, *Member, IEEE*, and Tien Sheng Chao

Abstract—This study describes a novel technique for forming low temperature oxides (<350 °C) using a replacement metal gate process. Low temperature oxides were generated by N₂O plasma in a PECVD system with pretreatment in CF₄. Fabricated oxides demonstrate excellent current–voltage (*I*–*V*) characteristics, such as low leakage current, high breakdown charge and good reliability. Experimental results indicate that CF₄ plasma treatment can significantly improve the mobility and resistance against hot carrier stress of MOSFETs. With excellent electrical properties, this technique is suitable for fabrication low temperature devices.

Index Terms—Low temperature oxides, mobility and hot carrier stress, N₂O/CF₄ plasma, *Q*_{bd}, replacement metal gate, TDDB.

I. INTRODUCTION

AS SEMICONDUCTOR devices are being scaled down, increasing the speed of devices by reducing the parasitic resistances of gate/source/drain is becoming more important. Polysilicon processes with dopant activation retain a large gate parasitic resistance. The use of metal gates is a possible solution to reduce gate resistance in future generations of MOSFETs [1]–[4]. However, conventional high-temperature processes, such as thermally growing oxides will be incompatible with the desired device structure. For example, the metal replacement gate process [5]–[7] involves annealing the source/drain implant before the gate insulator is formed. Thermal oxides grown subsequently by high temperature processes deviate from the existing doping profiles. Based on fabrication procedure, gate oxides formed at low temperature conditions are very important for replacement gate applications. PECVD offers the advantages of depositing an oxide at a very low temperature. Depositing oxides directly on device substrates can eliminate the thermal process and the segregation or redistribution of the dopant. Moreover, some studies have revealed that oxynitrides formed by N₂O show good electrical properties [8]. Combining the two concepts, oxidation in N₂O plasma by PECVD provides a simple way to form low temperature oxides. Nevertheless, the interfacial properties of nitrides oxides are the outstanding issue [9], [10]. Fluorinated oxides with high resistance against ionized radiation and hot carriers have been reported [11], [12].

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TABLE I
SPLIT CONDITIONS OF GATE DIELECTRICS FORMATION
OF LT-OXIDES WITH METAL GATE

	CF ₄ pre-treatment	Oxide formation by N ₂ O plasma	
		Time interval	Chamber environment
CF ₄ +25sec	CF ₄ flow rate: 20sccm Time : 30sec RF power : 5W	25 sec	N ₂ O flow rate:20sccm RF power : 50W Ar flow rate : 50sccm Substrate heating : 300°C Chamber pressure : 500m T
CF ₄ +90sec		90 sec	
CF ₄ +180sec		180 sec	
25sec	None	25 sec	
90sec		90 sec	
180sec		180 sec	

Furthermore, plasma treatment has been recently used as a simple way to improve device characteristics in the IC industry. Our recent study described a simple fabrication process to grow low temperature fluorinated oxides, formed by N₂O plasma with further CF₄ plasma pretreatment [13]. This study investigates the electrical and physical characteristics of MOSFETs with this fluorinated oxide using CF₄ plasma pretreatment.

II. EXPERIMENTS

MOS capacitors and MOSFETs with a TiN metal gate were fabricated on a 6-in (100) p-type silicon wafer with a resistivity of 5–10 Ω-cm. Replacement metal gate processes were applied to fabricate the devices. After the Source/Drain was formed and the dummy gate was removed, gate dielectrics were grown by N₂O plasma in a PECVD system at 300 °C. Before the gate dielectric was formed, some samples were treated in CF₄ plasma in the same chamber. Table I lists the split conditions to form the gate dielectric. Thermal oxides were grown in O₂ ambient at 900 °C to serve as control samples. After the gate dielectric was formed, a 4-layer metal gate electrode (TiN/Al–Si–Cu/Ti/TiN) was deposited. All process temperatures after the dummy gate was removed were lower than 400 °C.

The current–voltage (*I*–*V*) characteristics were measured using an HP 4156A to determine the electrical properties and reliability of the gate dielectric. Capacitance–voltage (*C*–*V*) curves were measured by HP4284A and the equivalent oxide thickness (EOT) of gate dielectrics was extracted. The physical properties of gate dielectric films were investigated using an

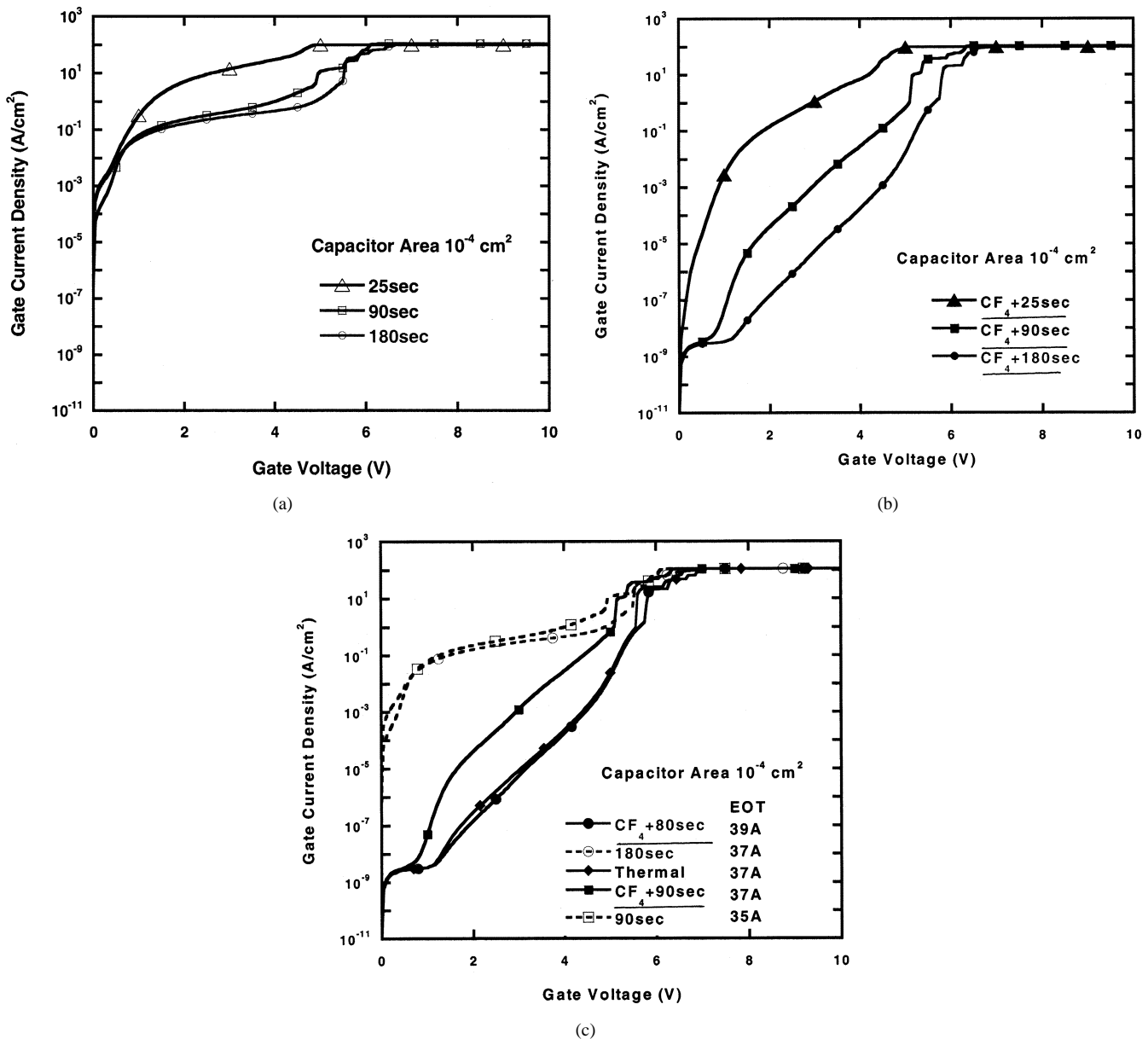


Fig. 1. (a) J - V characteristics of LT oxide films with different plasma duration. (b) J - V characteristics of LT oxide films with CF_4 pretreatment with different plasma duration. (c) J - V characteristics of LT oxides with/without CF_4 treatment and thermal oxides.

ESCA (electronic spectroscope for chemical analysis), and an AFM (atomic force microscope). The ESCA technique is highly surface specific due to the short range of the photoelectrons that are excited from the solid. The energy of the photoelectrons leaving the sample is determined using a CHA (Concentric Hemispherical Analyzer) and this gives a spectrum with a series of photoelectron peaks. The binding energy of the peaks is characteristic of each element. The peak areas can be used (with appropriate sensitivity factors) to determine the composition of the materials surface.

III. RESULTS AND DISCUSSION

A. Characteristics of Low Temperature Oxide With TiN Gate

Fig. 1(a) and (b) show J - V characteristics of low temperature oxides (LT oxides) with and without CF_4 treatment. LT oxides

were formed using N_2O plasma in 25, 90, and 180 s. As-deposited samples have a large leakage current due to damage caused by plasma and samples with longer process times have a lower leakage current as the equivalent oxide thickness (EOT) increases. The rate of deposition by N_2O plasma saturated at 90 s. Notably, excess N_2O plasma will increase the density of the low-temperature oxide and only slightly increases the EOT. Thus, the additional CF_4 pretreatment restores the LT oxides and yields a better I - V curve, perhaps due to the formation of strong Si-F bonds replacing weak bonds such as Si-H and Si-OH. Fig. 1(c) plots the J - V characteristics of LT oxides with/without CF_4 treatment and thermal oxides. The numbers represent the duration of N_2O plasma treatment. According to our results, as-deposited or "90 sec" samples, have the largest leakage current among these samples due to plasma damage. However, the sample pre-treated with CF_4 exhibits a significant reduction in leakage that is comparable to that of thermal

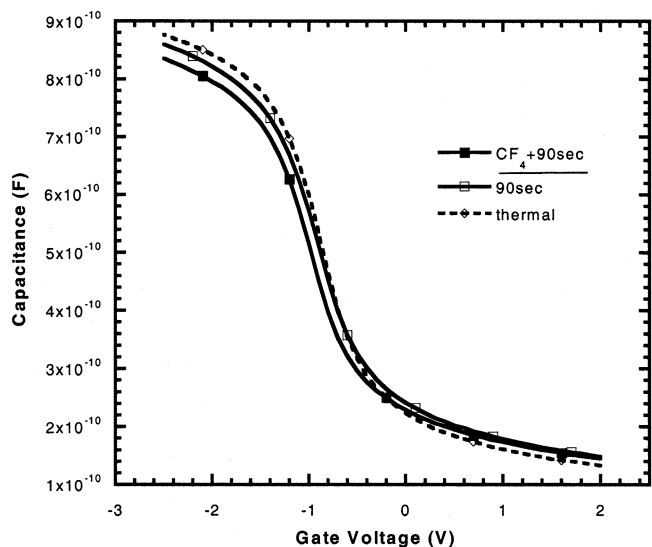


Fig. 2. *C*-*V* characteristics of thermal oxide and LT oxides with/without CF₄ pre-treatment.

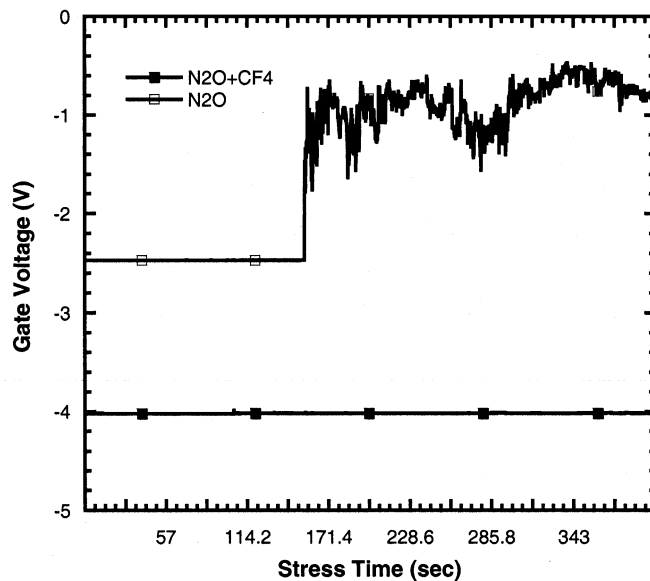


Fig. 4. Stress time versus gate voltage of LT oxides with/without CF₄.

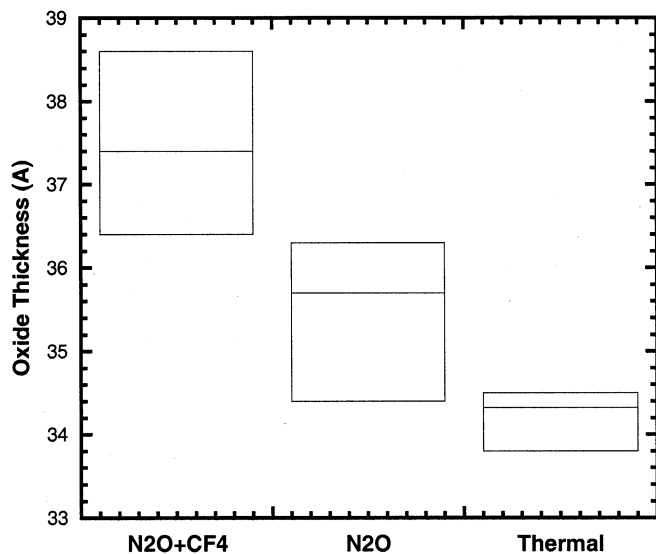


Fig. 3. EOT for each sample.

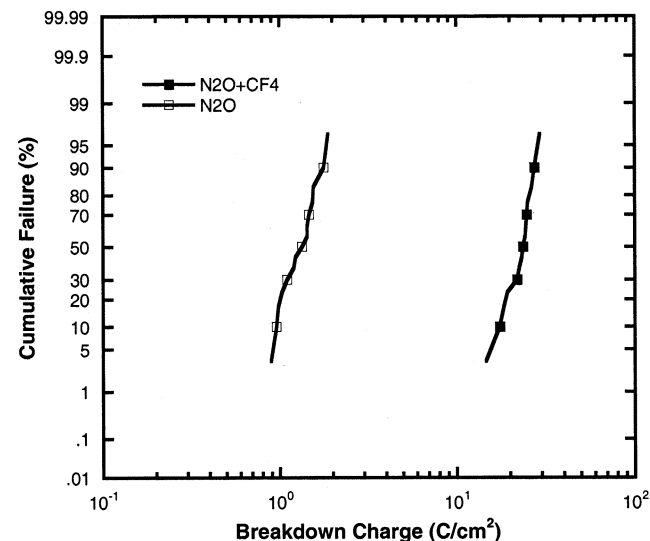


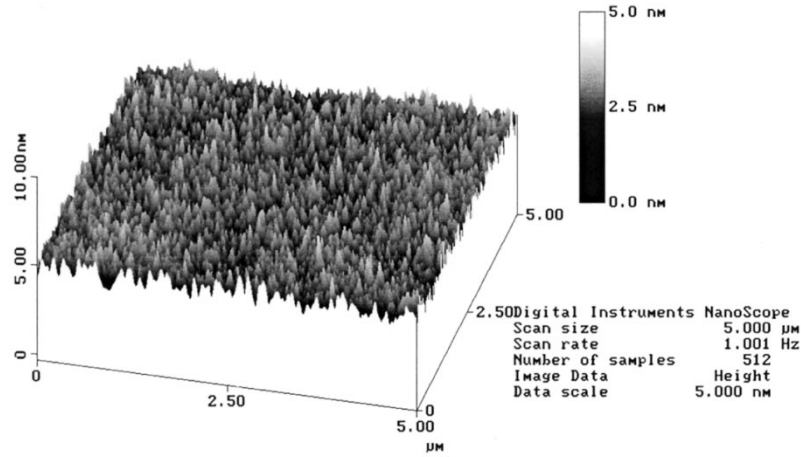
Fig. 5. Charge to breakdown (*Qbd*) distribution.

oxide. This improvement appears to follow from the formation of strong Si-F bonds. Although a longer plasma time typically causes significant damage to the film, according to the results obtained, the sample pre-treated with CF₄ performs excellently almost as well as thermal oxides. With CF₄ treatment, a longer N₂O plasma time is preferred over a shorter one. Therefore, the low-temperature oxide formed by N₂O plasma (for 180-sec) with CF₄ pretreatment could effectively improve the *I*-*V* characteristics similar to thermal oxides.

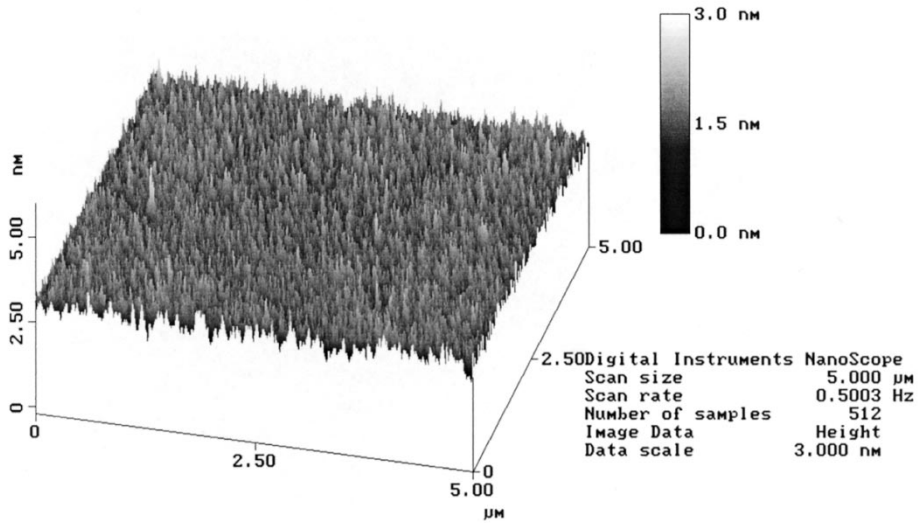
Fig. 2 plots the high-frequency *C*-*V* characteristics of thermal oxide and LT oxides with/without CF₄ pre-treatment. The frequency of *CV* measurement was 100 KHz. The LT oxide curve is similar to that of thermal oxide, but the capacitance of the LT oxide is slightly lower than that of thermal oxide. A negligible *V*_{FB} shift implies that nearly no fixed charge or traps exist in the LT oxide. Moreover, additional CF₄ treatment causes a *V*_{FB} shift due to the incorporation of fixed charges in oxide regimes. Restated, fluorine incorporated into

oxide regimes enhances the generation of oxide fixed charges. Fig. 3 plots the EOT of each sample. Fifty samples were tested for each condition. The EOTs were extracted in accumulation mode. CF₄ pre-treatment did not greatly increase the electrical thickness of the dielectric film. The thickness variation of LT oxides with/without CF₄ pre-treatment exceeds that of thermal oxide, resulting in PECVD dielectric film that is less uniform than thermal oxide film.

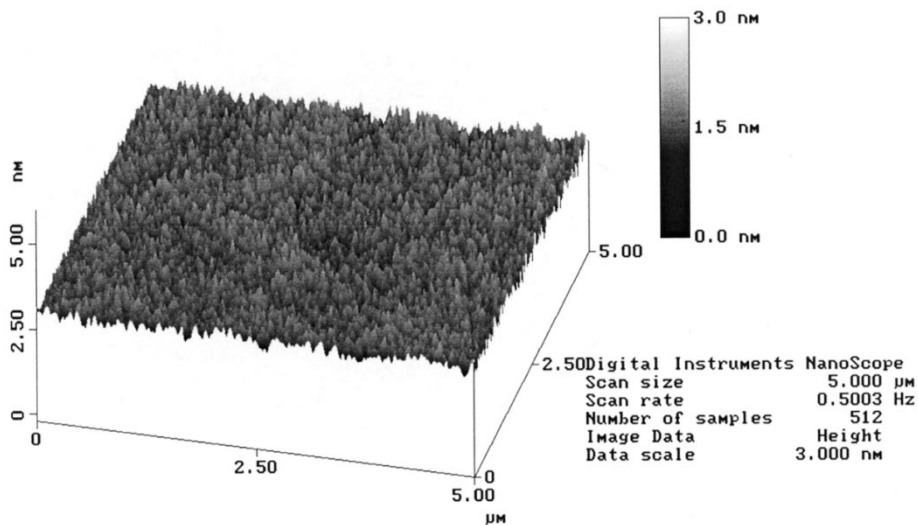
Maintaining a constant current stress enables the integrity of the gate insulator to be determined. Fig. 4 plots stress time versus gate voltage for LT oxides with/without CF₄. The applied current density is 10 mA/cm². The CF₄-treated sample exhibits negligible voltage variation. But LT oxides without CF₄ pre-treatment exhibit breakdown phenomena after approximately 170 s. The time to breakdown is one order of magnitude smaller than CF₄-treated; we did not include time to breakdown of CF₄-treated sample in Fig. 4. The CF₄ pre-treated film is better than the other film, implying that the



(a)



(b)



(c)

Fig. 6. (a) AFM image of the sample after standard cleaning with RMS roughness of 3.4 Å. (b) AFM image of the sample using N₂O 90 s formation without CF₄ treatment with RMS roughness of 1.8 Å. (c) AFM image of the sample using N₂O 90 s formation with CF₄ treatment with RMS roughness of 1.3 Å.

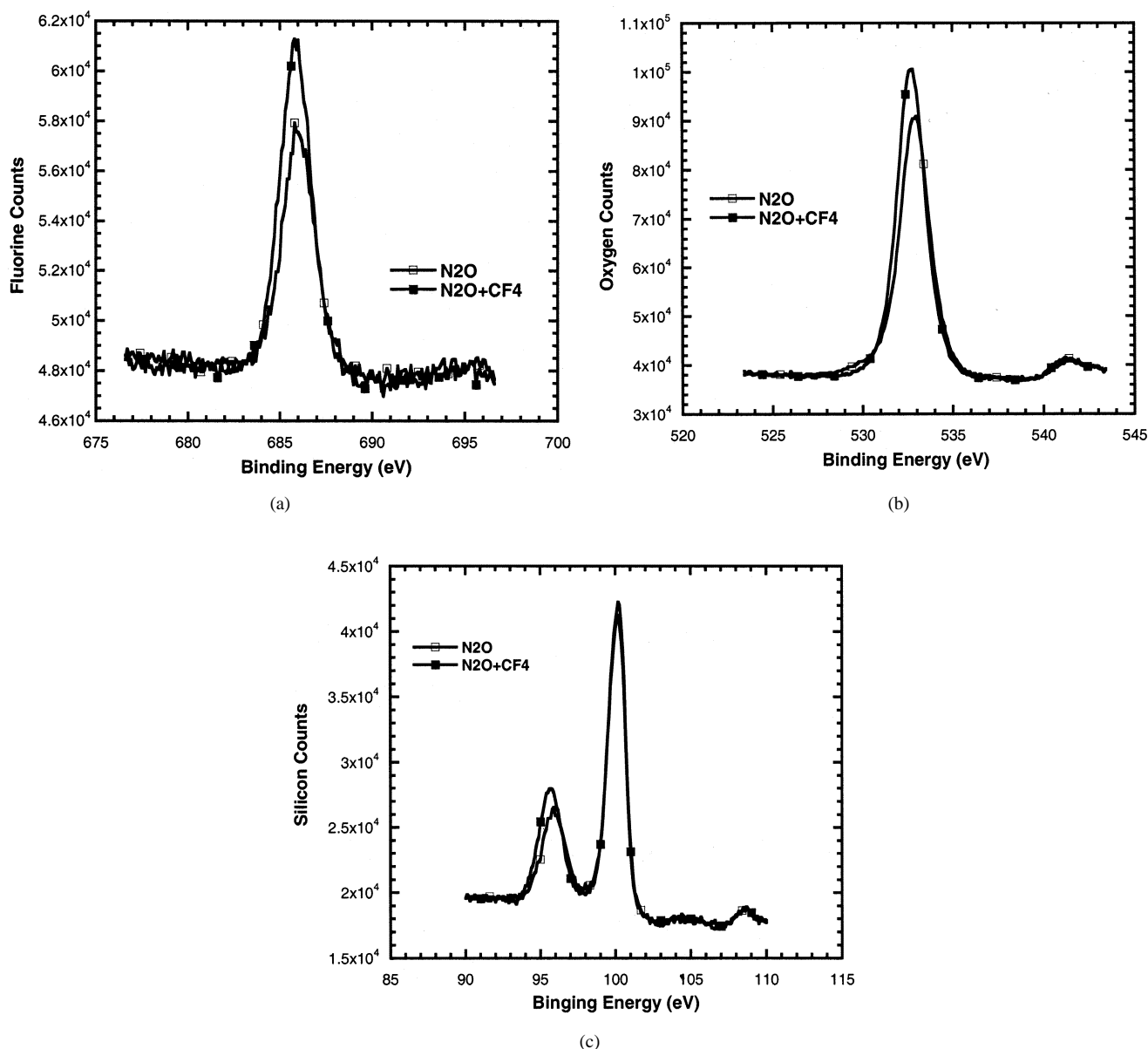


Fig. 7. ESCA spectra of LT oxides with/without CF₄. The amount of F and O increased after CF₄ pre-treatment. (a) Fluorine peak. (b) Oxygen peak. (c) Silicon peak.

formation of Si-F bonds can reduce the number of interface traps between Si and the oxide interface, and improve the reliability of the LT oxides. Breakdown charge is one specification of the quality of a gate insulator. Breakdown charge is defined as constant stress current density multiplied by the time to breakdown. Fig. 5 exhibits that charge to breakdown (*Q_{bd}*) distribution of LT oxides with/without CF₄. The breakdown charge can be increased by a single order of magnitude by additional CF₄ pre-treatment. Restated, CF₄ pre-treatment can effectively increase the incorporation of fluorine into oxide regimes and improve the integrity of the LTO.

Nevertheless, CF₄ plasma is one kind of etching processes. The atomic force microscope (AFM) was used to measure the surface morphology of all samples and thus determine the effect of CF₄ on the silicon surface. Fig. 6(a) presents the AFM image of the sample after standard cleaning, (b) is the sample using N₂O 90 s formation without CF₄, and (c) is the sample using

N₂O 90 s formation with CF₄. The RMS roughness of (a), (b), and (c) are 3.4 Å, 1.8 Å, and 1.3 Å, respectively. These values show that CF₄ pre-treatment smooths the silicon surface morphology, without further damaging it. Consequently, low power CF₄ plasma treatment does not cause etching during LT oxides formation.

Electron Spectroscopy for Chemical Analysis (ESCA) was applied to samples with/without CF₄ treatment to identify the incorporation of fluorine during CF₄ treatment. Fig. 7(a)–(c) present the intensities associated with fluorine, oxygen and silicon, respectively. Further CF₄ pretreatment not only increases the incorporation of fluorine but also increases the number of Si-O bonds. Moreover, the Si peak is shifted in Fig. 7(c) due to the incorporation of fluorine. Restated, CF₄ treatment can improve low temperature LT oxide by replacing dangling bonds with stronger Si-F or Si-O bonds. Table II is the quantify table of LT oxides with/without CF₄ treatment. Additional CF₄ pre-

TABLE II
QUANTIFICATION TABLE OF LT OXIDES WITH/WITHOUT CF₄

Atom %	N ₂ O oxide without CF ₄	N ₂ O oxide with CF ₄
F 1s	4.166	5.933
O 1s	32.689	37.963
N 1s	1.265	< 1%
C 1s	15.692	11.342
Si 2p	46.188	44.762

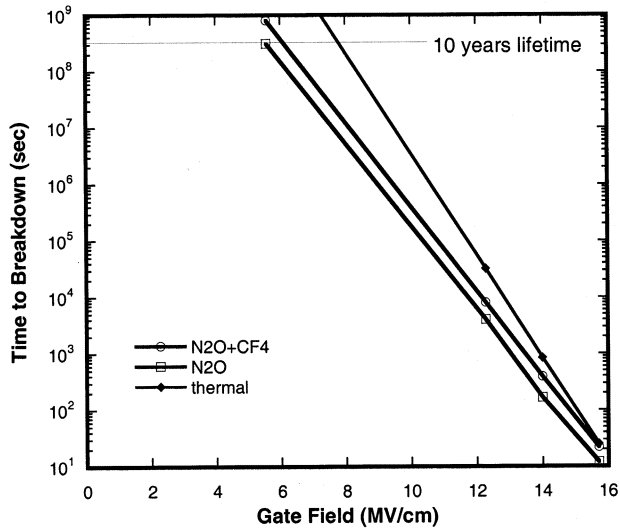


Fig. 8. TDDB plot of LT oxides with/without CF₄ treatment.

treatment reduces the amount of nitrogen and carbon, demonstrating that the improvement in I - V characteristics was due to the replacement of Si-C and Si-H with stronger Si-F bonds.

Time-dependent dielectric breakdown (TDDB) is one characteristic used in determining the lifetime of a device. Three different high fields are applied to measure the time to breakdown (pad area = 3×10^{-4} cm²); the operating field for a lifetime of 10 years can be determined by extrapolation [14]. According to our results (Fig. 8), the operating field of the LT oxide is 5.5 MV/cm for a lifetime of ten years. Moreover, the CF₄-treated sample has an increased operation field of 6.2 MV/cm, confirming that the proposed method of CF₄ treatment can improve the integrity of LT oxides. However, the reliability of thermal oxides exceeds that of CF₄-treated low temperature oxides. The low temperature process (<350 °C) can not anneal defects or traps during plasma fabrication and degrades the reliability of the oxide. However, low temperature oxides with CF₄ treatment are highly promising for low temperature applications.

B. Electrical Characteristics of MOSFETs

The exact effect of the proposed CF₄ pre-treatment method on the performance of devices is described when NMOSFETs are fabricated by the replacement gate process. Fig. 9 shows the V_g - I_d characteristics of 10 μ m/1 μ m NMOSFETs using LT oxides with/without CF₄ pre-treatment. Samples without CF₄ treatment have inferior characteristics because of a large gate

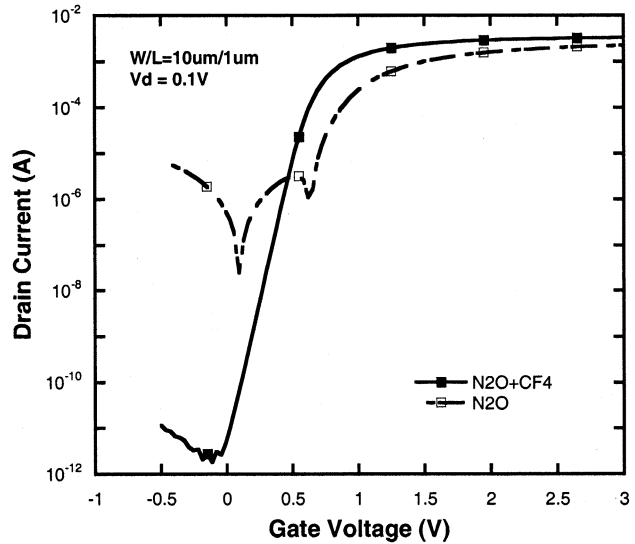


Fig. 9. V_g - I_d characteristics of LT oxides with/without CF₄ pre-treatment.

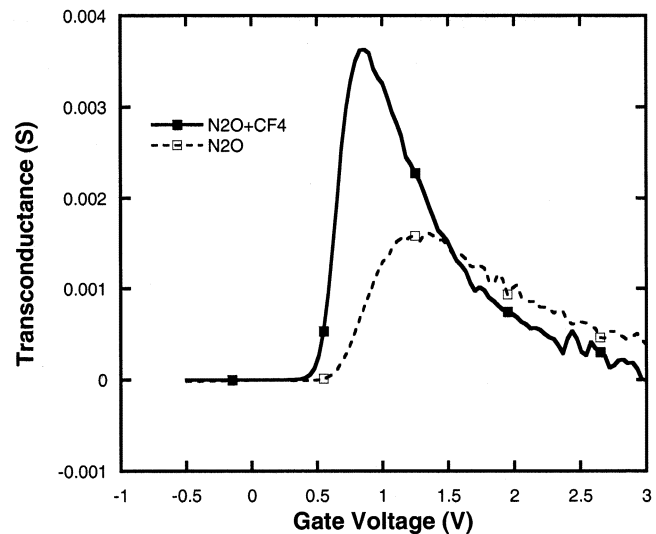


Fig. 10. Transconductance (G_m) of LT oxides with/without CF₄ pre-treatment.

current, and the I_d distortion is also caused by gate leakage. For samples that had undergone CF₄ pretreatment, a 70% improvement in drain current is observed. Restated, CF₄ pretreatment can effectively improve device performance. Fig. 10 shows the transconductance (G_m) of LT oxides with/without CF₄ pre-treatment. The maximum G_m value of a sample with CF₄ is 3.5 mS, and its V_{th} (threshold voltage) is 0.8V. A sample without CF₄ has a lower G_m value of 1.6 ms, and its V_{th} is shifted to 1.25 V. We posit that additional CF₄ pre-treatment can reduce the number of interface states and maintain higher mobility. A higher G_m is associated with an electrically superior Si/SiO₂ interface. Fluorine incorporation increases the number of Si-F bonds and efficiently suppresses the surface scattering effect. Moreover, the difference in the threshold voltage is related to the plasma-induced charge generation, as confirmed by Fig. 2.

Fig. 11 plots the V_d - I_d characteristics of samples with/without CF₄ pre-treatment. The gate voltage step is

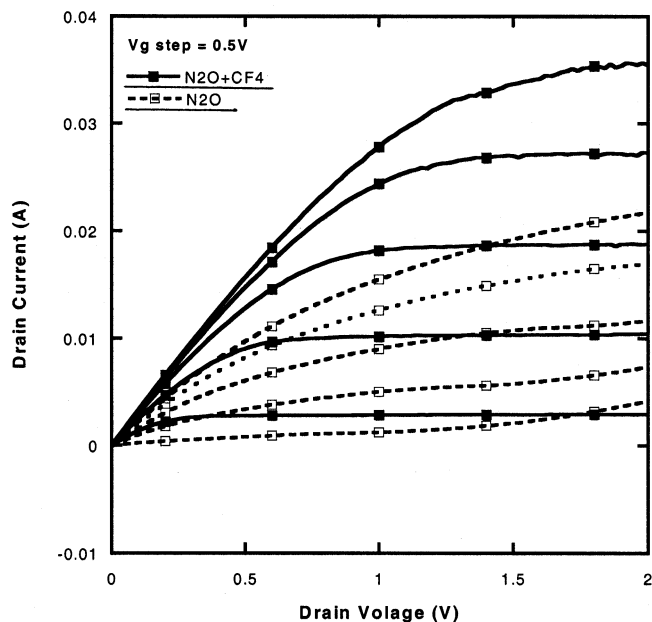


Fig. 11. V_d - I_d characteristics of LT oxides with/without CF₄ pre-treatment.

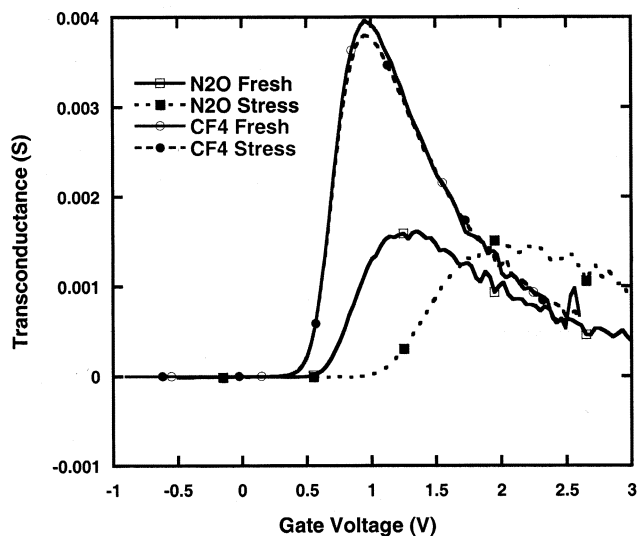


Fig. 12. G_m degradation of LT oxides with/without CF₄ after 100 s stress.

0.5 V and the W/L dimensions of the measured MOSFETs are 10/1. No saturation region of N₂O samples is observed to be caused by increasing the gate leakage current. Additional CF₄ pre-treatment can further improve the carrier mobility and drivability. Not only can the surface scattering effect be suppressed, but also the surface morphology can be improved. Restated, CF₄ pretreatment can increase interface quality and reduce the roughness of the surface.

Hot carrier lifetime is an important issue in device operation, especially when the device is stressed under drain avalanche hot carrier (DAHC) conditions. Fig. 12 illustrates the G_m degradation after DAHC stressing ($V_d = 3$ V, $V_g = 1.5$ V) LT oxides with/without CF₄ treatment for 100 s. The degradation of both these samples is minor, but the N₂O sample exhibits a V_{th} shift after stress. Given the poor interface quality (even bulk) of LT

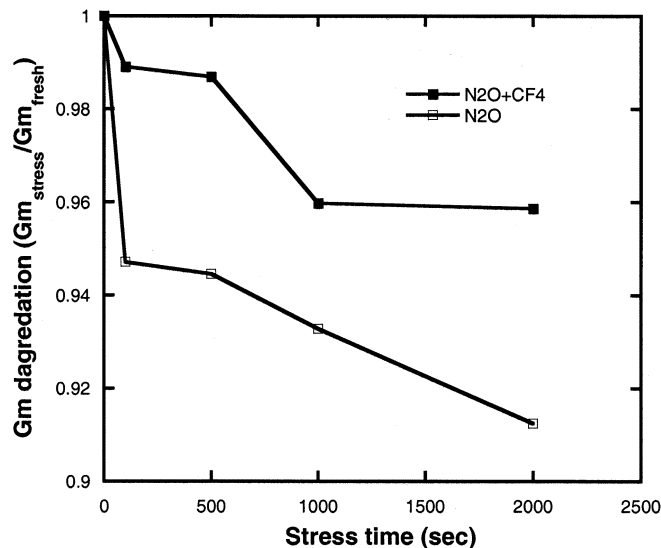


Fig. 13. Time dependence of G_m degradation after DAHC (drain avalanche hot carrier) stress.

oxides, many hot carriers destroy the film's structure and introduce traps. CF₄ pre-treatment increases the incorporation of fluorine and effectively increases resistance against hot carrier stress. Fig. 13 plots the time-dependence of G_m degradation after DAHC stress of N₂O oxide with/without CF₄ pre-treatment. Under fixed hot carrier stress conditions, CF₄ treatment reduces the hot carrier effect, yielding stronger Si-F bonds that increase the ability of the oxide to resist hot carrier stress.

IV. CONCLUSIONS

Results in this study demonstrate that additional CF₄ treatment improves the I - V characteristics of the low temperature oxide, which performs similar to the thermal oxide. CF₄ pre-treatment improves gate oxide integrity (GOI) and the reliability of LTO, because Si-F bonds replace dangling bonds between the oxide/Si interface, and fluorine can enhance re-oxidation to make strengthen the oxide. LTO with CF₄ treatment has excellent leakage, breakdown, Q_{bd} , TDDDB, and SILC properties, as well as MOSFET characteristics.

REFERENCES

- [1] T. Ohmi, "Trend of future silicon technology," *Jpn. J. Appl. Phys.*, vol. 33, p. 6747, 1994.
- [2] K. Ino, T. Ushiki, K. Kawai, I. Ohshima, T. Shinohara, and T. Ohmi, "Highly-reliability, low-resistivity bcc-Ta gate MOS technology using low-damage Xe-plasma sputtering and Si-encapsulated silicidation process," in *VLSI Tech. Dig.*, 1999, pp. 186-184.
- [3] D. H. Lee, S. H. Joo, G. H. Lee, J. Moon, T. E. Shim, and J. G. Lee, "Characteristics of CMOSFETs with sputter-deposited W/TiN stack gate," in *VLSI Tech. Dig.*, 1995, p. 119.
- [4] H. Yang *et al.*, "A comparison of TiN processes for CVD W/TiN gate electrode on 3 nm gate oxide," in *IEDM Tech. Dig.*, 1997, pp. 459-462.
- [5] A. Chatterjee *et al.*, "CMOS metal replacement gate transistors using tantalum pentoxide gate insulator," in *IEDM Tech. Dig.*, 1998, pp. 777-780.
- [6] J. M. Hergenrother *et al.*, "The vertical replacement-gate (VRG) MOSFET: A 50-nm vertical MOSFET with lithography-independent gate length," in *IEDM Tech. Dig.*, 1999, pp. 75-78.
- [7] C. P. Chang *et al.*, "SALVO process for Sub-50 nm low-Vt replacement gate CMOS with KrF lithography," in *IEDM Tech. Dig.*, 2000, pp. 53-56.

- [8] H. R. Soleimani, B. S. Doyle, and A. Philipossian, "Formation of ultrathin nitrated SiO_2 oxides by direct nitrogen implantation into silicon," *J. Electrochem. Soc.*, vol. 142, no. 8, p. 132, 1995.
- [9] A. Kamgar *et al.*, "Reduced electron mobility due to nitrogen implant prior to the gate oxide growth," *IEEE Electron Device Lett.*, vol. 21, May 2000.
- [10] A. Kamgar *et al.*, "Impact of nitrogen implant prior to the gate oxide growth on transient enhanced diffusion," in *IEDM Tech. Dig.*, 1997, p. 695.
- [11] G. O. Lo *et al.*, "Thin fluorinated gate dielectrics grown by rapid thermal processing in O_2 with diluted NF_3 ," *IEEE Trans. Electron Devices*, vol. 35, p. 148, 1992.
- [12] T. K. Nguyen *et al.*, "Effects of fluorine implants on induced charge components in gate oxides under constant current Fowler–Nordheim stress," *IEEE Trans. Electron Device*, vol. 44, p. 1432, 1997.
- [13] T. Y. Chang *et al.*, "Improvement of low temperature gate dielectric formed in N_2O plasma by an additional CF_4 pretreatment process," *IEEE Electron Device Lett.*, to be published.
- [14] J. McPherson, V. Reddy, K. Banerjee, and L. Huy, "Comparison of E and 1/E TDDB models for SiO_2 under long-term/low-field test conditions," in *IEDM Tech. Dig.*, 1998, pp. 171–174.



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