Active Devices Under CMOS I/O Pads

Kuo-Yu Chou, Ming-Jer Chen, *Senior Member, IEEE*, and Chi-Wen Liu

***Abstract*—Active devices, including electrostatic discharge protection devices and ring-oscillator circuits, under CMOS I/O pads are investigated in a 130 nm full eight-level copper metal complementary metal–oxide-semiconductor process, using fluorinated silicate glass (FSG) low-k inter-metal dielectric. The high current I–V curve measured in the second breakdown trigger point (V_{t2}, I_{t2}) of ESD protection devices under various metal level stack structures, shows that i) I_{t2} depends very weakly on the number of metal levels used, as expected given specific junction power dissipation criteria; and ii) V_{t2} increases with the number of metal level stacks of I/O pads because of increased dynamic impedance due to the presence of more metal levels, as clarified by a simple RC model. Moreover, no noticeable degradation in the speed of the ring-oscillator circuit, as measured for a variety of test structures subjected to bonding mechanical stress, thermal stress by temperature cycling and dc electrical stress by transmission line pulse, as well as ac electrical stress by capacitive-coupling experiments. Accordingly, active devices under CMOS I/O pads is independent of bonding pad metal level structures.**

***Index Terms*—CMOS, copper, ESD, FSG, IMD, I/O bonding pad, low-k, propagation gate delay, ring-oscillator, second breakdown trigger point, SOC, transmission line pulse.**

I. Introduction

THE AGGRESSIVE development of semiconductor technology [1] in the field of very large scale integration (VLSI) has enabled *state-of-the-art* chips to integrate entire electronic systems on a single chip. Today's systems on chips (SOC) can be designed to incorporate mixed-technology, including high-performance/low-power logic, analog, embedded SRAM/DRAM, radio frequency (RF), microelectromechanical systems (MEMS), and optical electronic systems [2]. However, this development is associated with problems. For example, a significant manufacturing issue surrounds the reliability of large-die-size chip assembly; that is, a large-die-size chip is rather prone to thermo-mechanical stress-induced failure, a phenomenon that involves interactions between packaging and silicon die, caused by thermo-mechanical stresses during manufacturing and packaging [3], [4]. Additionally, SOC's that incorporate all VLSI systems into a single system would have more than 100 million transistor gates, requiring up to 1000 input/output and power/ground pads. Consequently, more bonding pads occupy more area on the chip. The situation is worse for next-generation nodes, as the size of the chips stops according to the International Technology Roadmap for Semiconductors (ITRS) [5]. Trimming the bonding pad pitch help to maintain the used chip area, but a smaller bonding pad causes much more damage under the mechanical stress involved in bonding.

Accordingly, this work introduces a configuration scheme of active devices under CMOS I/O bonding pads [6], [7] in the 130 nm full eight-level copper metal/FSG low-k IMD CMOS process [8], thus increasing chip area usage without applying pretreatments, including additional insulating films [9] and buffer metal layers [10], [11]. An optimum 1.2 μm thick aluminum metal film, deposited on the top copper metal pad, serves as a bonding mechanical stress buffer layer to protect active devices under CMOS I/O pads from bonding mechanical stress.

Designs of SOCs can take advantage of active devices under CMOS I/O pads. Therefore, both I/O and core devices placed under bonding pads must be investigated. ESD protection device and ring-oscillator circuit are used especially to represent I/O and core devices, respectively. Furthermore, ESD protection devices cannot be scaled in proportion to internal core devices. Accordingly, it is imperative to examine ESDs under I/O pads because ESD protection devices in the I/O circuit continue to occupy a relatively large active region on the chip. Also, the ring-oscillator that is a very sensitive circuit for measuring the speed performance of CMOS core devices is a good qualified test circuit to sense mechanical and electrical performance of active devices under pads. Various test structures of which EDS protection device and ring-oscillator circuit combine a variety of bonding pad structures for this study are subjected to different bonding power and force stresses, temperature cycling (TC) thermal stress as well as *dc* and *ac* electrical stresses, to elucidate thoroughly their manufacturability and reliability.

II. Experimental

Aluminum metal film formed on the top copper metal film serves as a buffer layer against bonding stress; its thickness is crucial to effective buffering. A bonding mechanical stress simulation was performed, involving tensile stress (Sx), normal stress (Sz), shear stress (Sxz), arbitrary angle tensile and normal stress (Sl), and total equivalent shear stress (Seqv), all evaluated on the etching stop layers, to determine the required thickness of the aluminum buffer layer prior to manufacturing. Simulation results presented in Fig. 1 revealed that all stresses decline with as the thickness of the aluminum metal film increases, as expected. Moreover, Cu metal is easily oxidized if exposed in the air. Therefore, a minimum necessary thickness of aluminum metal film is required to cover the top most Cu metal. However, aluminum metal film on the top most Cu metal facilely

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K.-Y. Chou and M.-J. Chen are with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

C.-W. Liu is with Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan, R.O.C.

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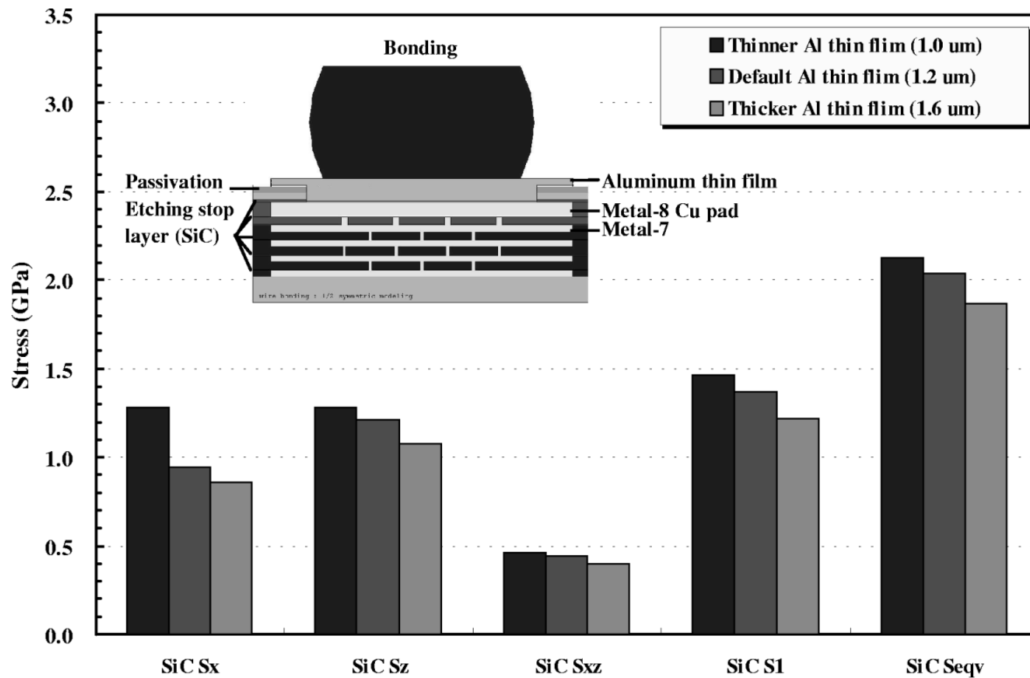


Fig. 1. Bonding mechanical stress simulation results for bonding pads with various thickness of aluminum metal films. All results are for the etching stop layers, **SiC**. **Sx** is tensile stress; **Sz** is normal stress; **Sxz** is shear stress; **Sl** is arbitrary angle tensile and normal stress, and **Seqv** is total equivalent shear stress.

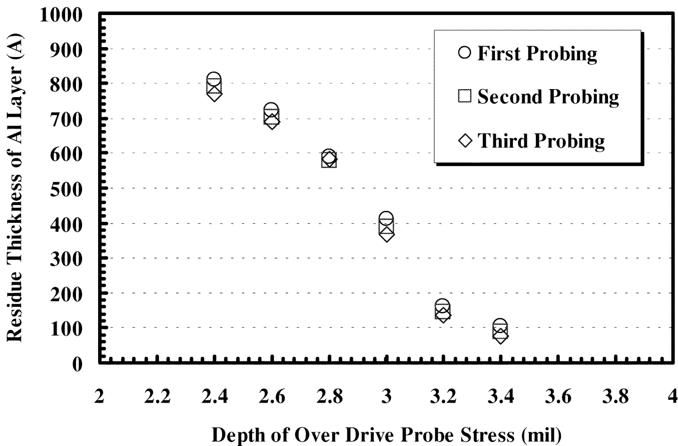


Fig. 2. Residue thickness of aluminum metal film on the top most copper metal under probing test by various depth of over drive probe stress in three-time operations.

suffers damage from probing test to expose Cu metal layer. Accordingly, from Fig. 1, we select the smallest 1.0 μm thickness aluminum metal film to deposit on the top most Cu metal for probing test. Fig. 2 shows the residue thickness of aluminum metal layer after samples are probed by various depth of over drive probe stress in three-time operations. When the depth of over drive probe stress has been increased up to 3.4 mil at the third probing test, Cu metal almost is exposed due to only about 50 Å residue thickness of aluminum metal film on the top most Cu layer. Therefore, 1.2 μm aluminum metal on the top most Cu metal can be regarded as a minimum necessary thickness for safe probing test. Although a thickness of 1.6 μm aluminum metal film was suggested to protect completely from damage during the bonding process at room temperature, 1.6 μm was too thick to etch in the manufacturing process. Thus, only an aluminum metal film only of 1.2 μm was deposited on the 1.0 μm top most copper metal layer, metal-8, to study aluminum wire bonding in relation to bonding power and force stresses during bonding. A 130-nm full eight-level Cu metal/FSG low-k IMD CMOS process technology [8] can yield various assemblies of multimetal levels for a variety of CMOS I/O bonding pad structures, such as a full eight level metal bonding pad and a single level metal bonding pad.

ESD protection devices used here were simple 4-shunted-2-cascaded NMOS transistors, each with $W/L = 15$ μm/0.4 μm. A series of test structures of ESD protection devices under bonding pads were designed. They included i) ESD protection devices with no bonding pad on top, connected to a nearby conventional full eight-level metal bonding pad, as schematically depicted as configuration (a) in the inset of Fig. 4; and ii) ESD protection devices each under various metal stack structures of bonding pads, with different numbers of metal levels. The size of the pads was 70 μm $\times$ 70 μm, as in configurations (b) to (g) in the insert of Fig. 4. In this study, 104 samples from two pieces of wafers manufactured in 130 nm full eight-level Cu metal/FSG low-k IMD CMOS process are under open/short test, and then only 20 good samples with low leakage current, about under 1 pA, are selected for transmission line pulse (TLP) measurement. Each sample contains all ESD protection test structures, the (a) to (g) inset of Fig. 4. TLP with a 100 ns pulse width, was applied to ESD devices, which were packaged as in a dual in-line package (DIP), using aluminum wedge wire bonding with a bonding power of 100 mW and a bonding force of 20 g, to generate a high current I–V curve from which the

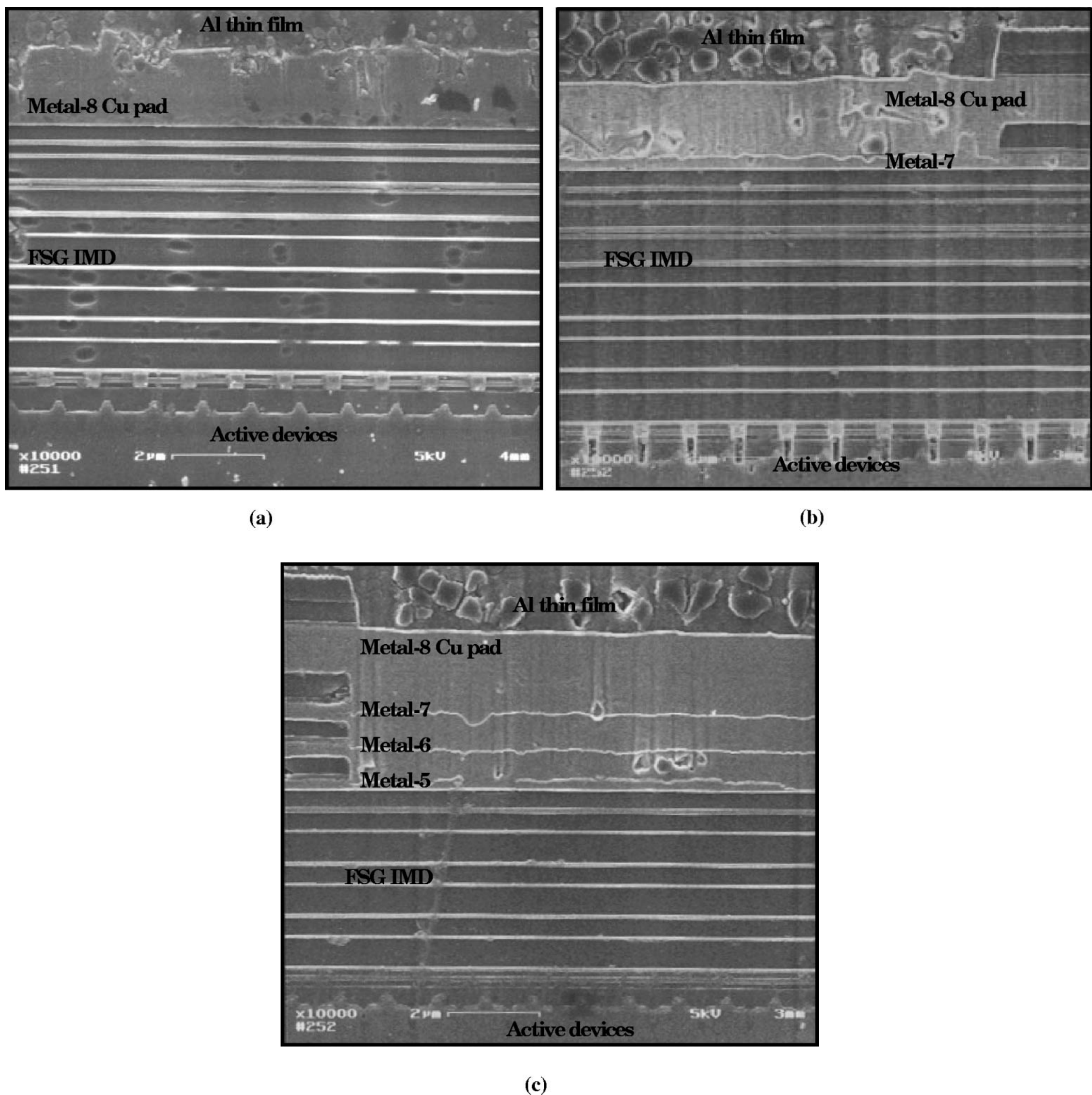


Fig. 3. SEM image of cross section of (a) Structure A, the ring-oscillator under CMOS bonding pad/metal-8, (b) Structure B, the ring-oscillator under CMOS bonding pad/metal-8/via-7/metal-7, and (c) Structure C, the ring-oscillator under CMOS bonding pad/metal-8/via-7/metal-7/via-6/metal-6/via-5/metal-5.

second breakdown trigger current I_{t2}, a measure of ESD robustness, and the second breakdown trigger voltage V_{t2}, can both be obtained.

A 1.2 V, 201-stage inverter-type ring-oscillator with a gate oxide thickness of 2 nm and an aspect ratio of $W_p/L_p = 1.8$ μm/0.13 μm and $W_n/L_n = 1.2$ μm/0.13 μm was fabricated in a 130 nm eight-level Cu metal/FSG low-k IMD CMOS process. Four kinds of ring-oscillator circuit are designed. i) Structure A, the ring-oscillator under the bonding pad/metal-8, shown in Fig. 3(a); ii) Structure B, the ring-oscillator under the bonding pad/metal-8/via-7/metal-7, shown in Fig. 3(b); and iii) Structure C, the ring-oscillator under the bonding pad/metal-8/via-7/metal-7/via-6/metal-6/via-5/metal-5, shown in Fig. 3(c), and iv) the Standard Structure, the ring-oscillator that does not underlie the bonding pad. Aluminum wedge wire bonding, which yields greater bonding stresses than Au–ball bonding with different bonding powers and forces, was used to package Structures A, B, and C. The bonding pad pitch was 95 μm. Similar to ESD experiment, 104 samples processed in 130 nm full eight-level Cu metal/FSG low-k IMD CMOS technology are under open/short test, and then 80 good samples with under pA level leakage current are selected for aluminum wire bonding mechanical stresses experiment with different bonding power and force, thermal mismatch stresses with 500 temperature

Fig. 4. Transmission line pulse with a 100 ns pulse width, was applied to the seven ESD protection devices, the conventional Structure and structures A to F, to determine the high current I–V curve from which the second breakdown trigger current I_{t2} and the second breakdown trigger voltage V_{t2}, can be measured.

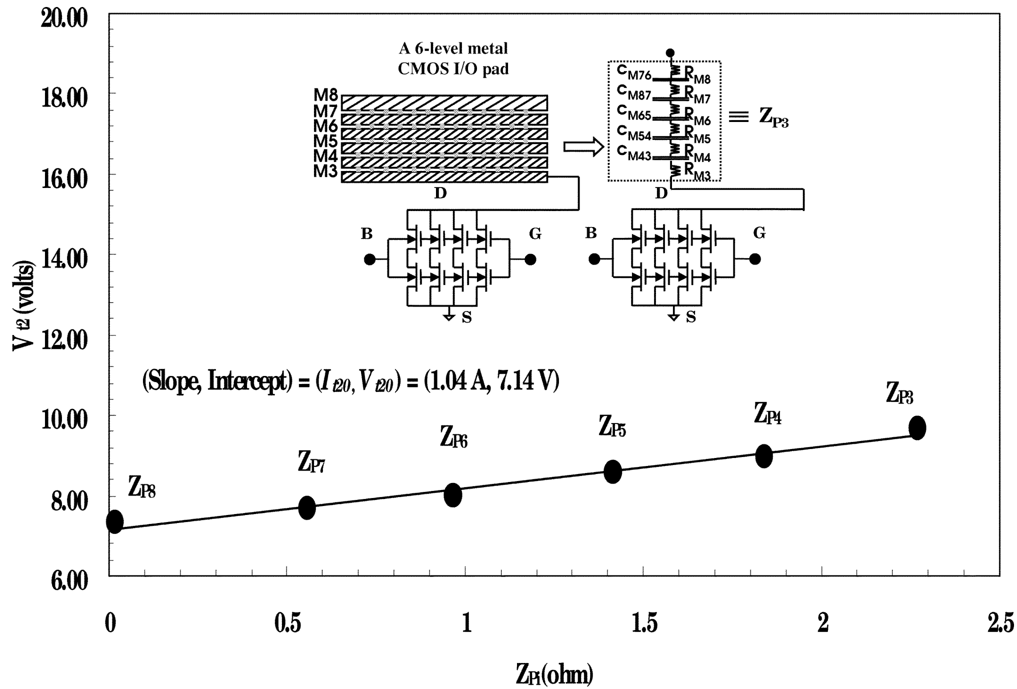


Fig. 5. Measured V_{t2} versus impedance calculated from (1) for structures A to F. I_{t20} and V_{t20} represents the intrinsic second breakdown trigger current and voltage, respectively.

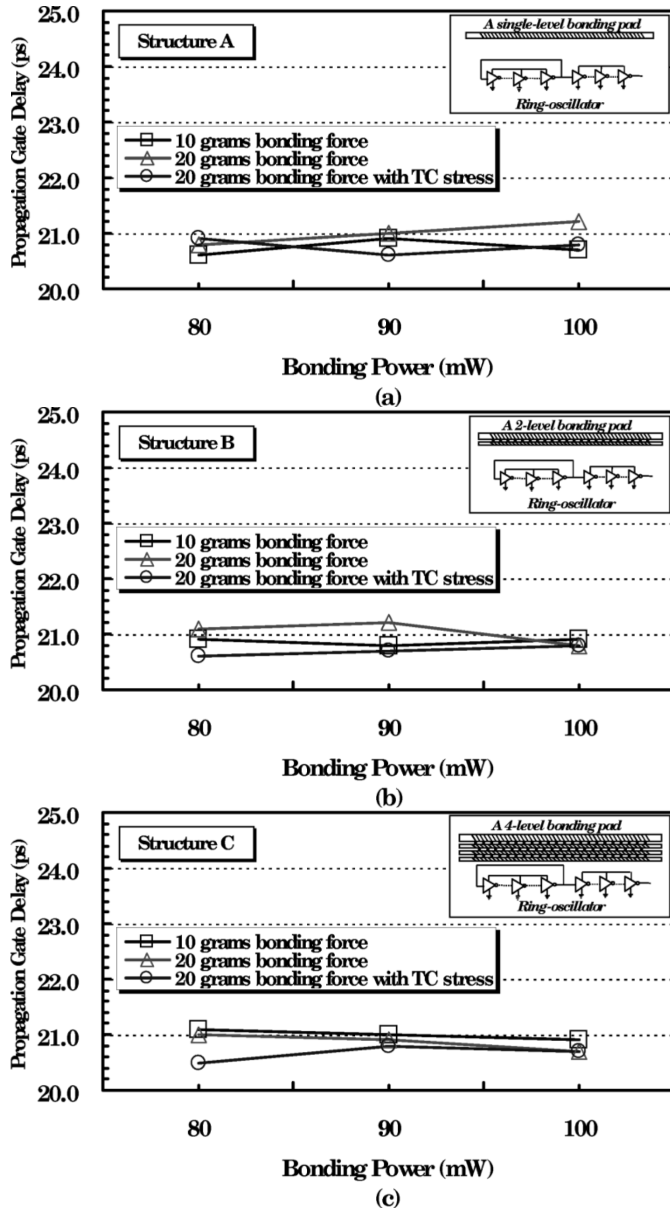


Fig. 6. Measured post-bonding propagation gate delay time versus bonding power for (a) Structure A, (b) Structure B, and (c) Structure C, at different bonding forces and 500 temperature cycling of thermal stress. The insets schematically depict cross sections of the structures.

cycling (TC), *dc* electrical stresses by transmission line pulse as well as *ac* electrical stresses by capacitive-coupling experiment. Each sample comprises all ring-oscillator test structures, Standard, and A, B, and C in Fig. 3. The packaged structures A, B, and C were exposed to a TC of -65° to 150° with a maximum of 500 cycles, to elucidate the damage due to thermal mismatch stresses among aluminum metal, the top copper metal, the inter-metal dielectric films and the devices. Then, TLP with a 100 ns current pulse, was applied, followed by leakage testing of all of the structures. Finally, a 1.2 V, 50% duty cycle voltage pulse with a frequency of up to 100 MHz, was applied to structures A, B, and C, to evaluate the sensitivity of the capacitive coupling.

III. Results and Discussion

ESD protection devices under CMOS I/O pads experienced a high bonding power and force during aluminum wedge wire bonding. They were then involved in a TLP experiment. A current pulse generated by discharging a charged transmission line was forced to enter the device under test. Monitoring the current that flowed through, and the voltage on the bonding pad, a high current I–V point was determined. Adjusting the pulse amplitude of the current generated more such points for all structures, as shown in Fig. 4. The I–V line (below the second breakdown trigger point) of Structure F devices under the single level metal CMOS I/O bonding pad, is similar to that of the conventional ESD protection devices [with no bonding pads above, as shown in configuration of Fig. 4(a)]. Even their second breakdown trigger points are very close to each other, apparent evidence that neither the bonding power nor force changes the underlying (lateral bipolar snapback high current properties). Further analyzes point out that i) I_{t2} depends very weakly on the number of metal levels used and ii) V_{t2} increases with the number of metal levels. Thus, the constant I_{t2} is solely determined by the number of underlying protection devices, independently of the bonding pad structures used. Particular junction power dissipation criteria may be the reason for such a relationship. The significant dependencies of V_{t2} on the bonding pad structures used does not imply that the ESD protection devices under the bonding pads were degraded. The mechanism responsible for the change in V_{t2} involves the presence of the dynamic impedance of the metal level of the bonding pad structures: more metal levels yield more impedance. With reference to the equivalent *RC* circuit model of I/O bonding pads, the impedance of a specified CMOS I/O pad, Z_{pi}, can be written as

$$Z_{pi} = \sum_{n=i}^{8} R_{M_n} + \sum_{m=i+1}^{8} \int_0^t dt / C_{M_{m,\, m-1}} \qquad (1)$$

where R_{Mn} is the level metal resistance, $C_{Mm,\, m-1}$ is the capacitance between two metal levels, and the current pulse width is 100 ns in this work. The resulting impedance values are very low, between 0.02 Ω and 2.27 Ω. Fig. 5 plots the measured V_{t2} versus calculated impedance for structures A to F. Strikingly, a linear relationship exists between the two. In particular, the slope and intercept of the line yield relevant information concerning the underlying ESD protection devices: the intrinsic second breakdown trigger current $I_{t20} = 1.04$ A and the voltage $V_{t20} = 7.14$ V. I_{t2}, a measure of ESD robust ability, weakly depends on the number of bonding pad metal layers. Therefore, structure A to F have comparable ESD immunity, indicating that moving ESD protection devices under CMOS I/O pads proves reliable in this study. Consequently, not only can occupation of chip area be avoided, but also design constraints for CMOS I/O bonding pads can be substantially relaxed, allowing much more flexible and robust ESD schemes, such as those that involve a distributed ESD protection device [12]. Such high-level ESD protection is essential in microprocessor and ASIC applications [13].

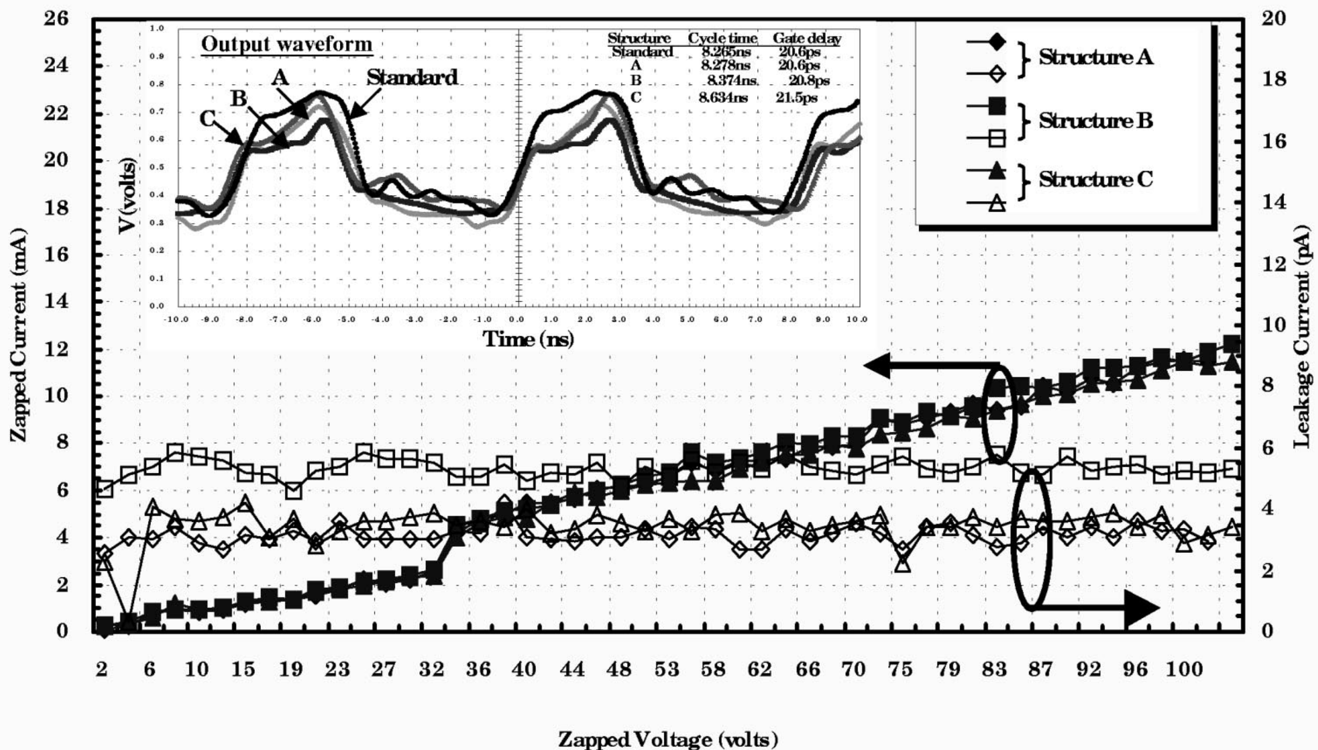
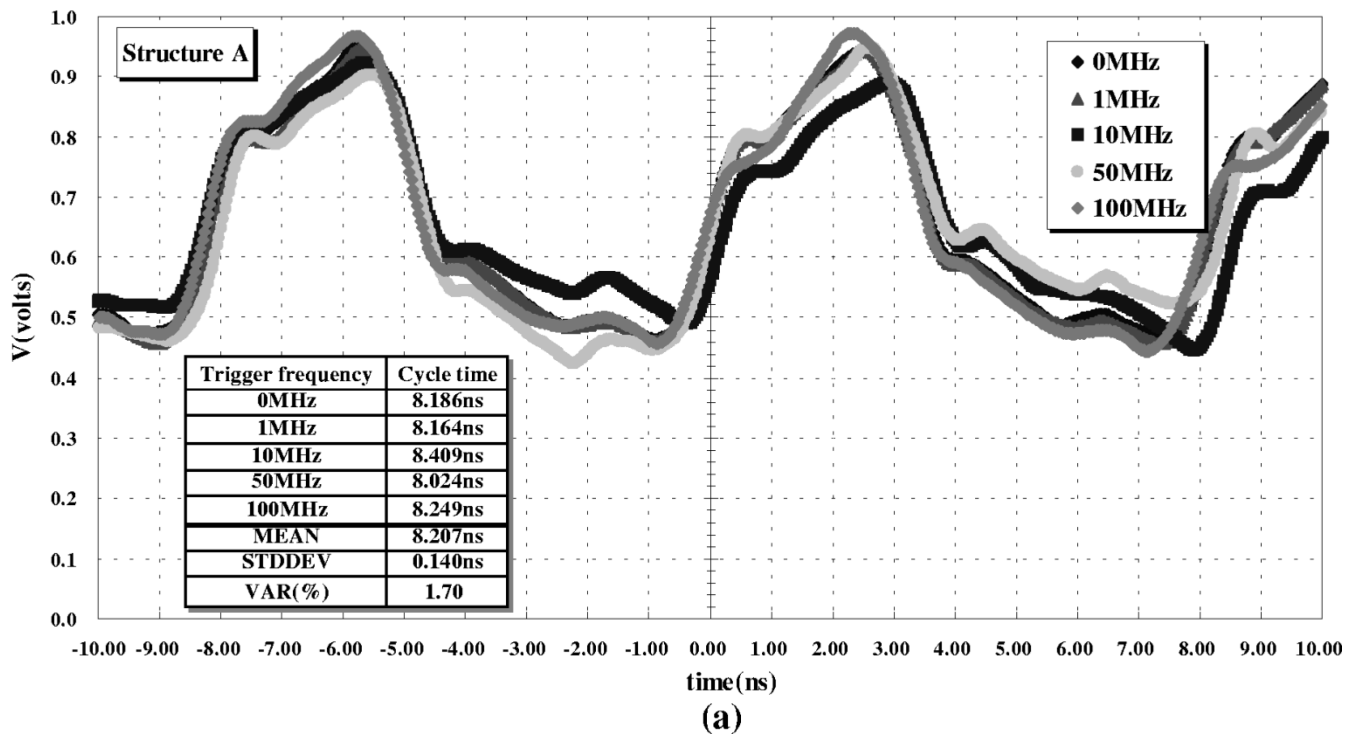


Fig. 7. Measured I–V characteristics for structures A, B, and C under transmission line pulse zapping. The monitored leakage versus applied voltage curve for each structure is also plotted. The inset shows output waveforms and cycle times (oscillating periods) and the propagation gate delay in each stage for the Standard Structure and structures A, B, and C, zapped by TLP.

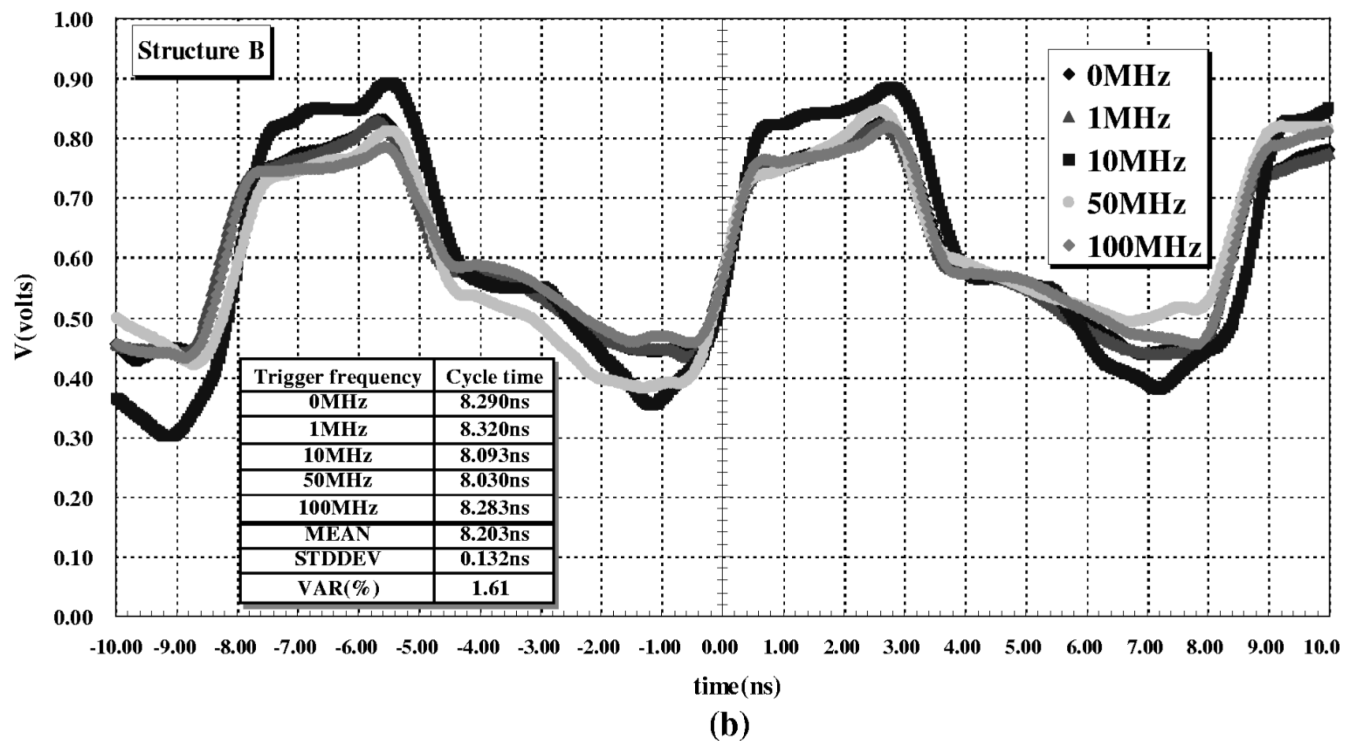
The propagation gate delay at each stage of the Standard Structure, measured prior to bonding was 20.9 ps, while the propagation gate delay per stage was 20.9 ps, 20.6 ps and 21.0 ps for structures A, B, and C, respectively. The speeds of all pre-bonding structures are similar to each other, and thus all the involved structures can be considered as "Control" samples, independently of the number of metal levels used. Fig. 6(a)–(c) plot the measured propagation gate delay time versus the bonding power for structures A, B, and C, respectively, with different bonding forces and 500 TC stress cycles. Cross section views of the corresponding ring-oscillator circuit under CMOS bounding pads are also shown. The bonding mechanical and thermal cycling stresses are seen to not to degrade significantly the electrical properties of these devices in relation to the "Control" samples, confirming the feasibility of the 130 nm full eight-level Cu metal/FSG low-k IMD CMOS process technology in fabricating active devices under CMOS I/O bonding pads, without using any extra mechanically firm insulating films [9] or buffer metal layers [10], [11]. This finding thus indicates that the goal of recovering chip area utility is reached.

During the TLP experiment on zapping, that is, electrically sudden stressing structures A, B, and C, the transient waveforms of the current and voltage on the bonding pads were recorded, A steady-state zapped current was thus measured in relation to voltage zapping. Adjusting the amplitude of the pulse current to approximately 12 mA (at a corresponding monitored pad voltage exceeded 100 V), yielded more such I–V data, as displayed in Fig. 7. After each TLP stress, the leakage was characterized. The measured leakage versus applied voltage is together plotted on the same figure. Leakage currents between the bonding pads and the ring-oscillator devices are relatively very low, 2 to 6 pA, in all structures. The insets in Fig. 7 plot the ring-oscillator output waveforms of the Standard Structure as well as of zapped structures A, B, and C. The corresponding cycle times and the propagation gate delay time per stage are also labeled. Apparently, TLP stresses do not noticeably degrade the performance of the ring-oscillator circuit under the bonding pads.

In fact, an operation signal of the active devices under CMOS I/O pads could suffer from disturbance or coupling due to a signal running over I/O bonding pads. Accordingly, the oscillating periods of structures A, B, and C, to which different frequencies of up to 100 MHz were applied, were measured for capacitive coupling. Fig. 8(a)–(c) show the transient waveforms for structures A, B, and C, respectively, under a 1.2 V, 50% duty cycle voltage pulse triggering frequencies of up to 100 MHz. Insets in Fig. 8(a)–(c) reveal the cycle times that correspond to the different triggering frequencies. They also present statistical data for structures A, B, and C, respectively. The experimental results indicate no appreciable signal distortions. Furthermore, from statistical data in Fig. 8(a)–(c), Structure A has a mean cycle time of 8.027 ns, Structure B has a mean cycle time of



Trigger frequency	Cycle time
0MHz	8.186ns
1MHz	8.164ns
10MHz	8.409ns
50MHz	8.024ns
100MHz	8.249ns
MEAN	8.207ns
STDDEV	0.140ns
VAR(%)	1.70



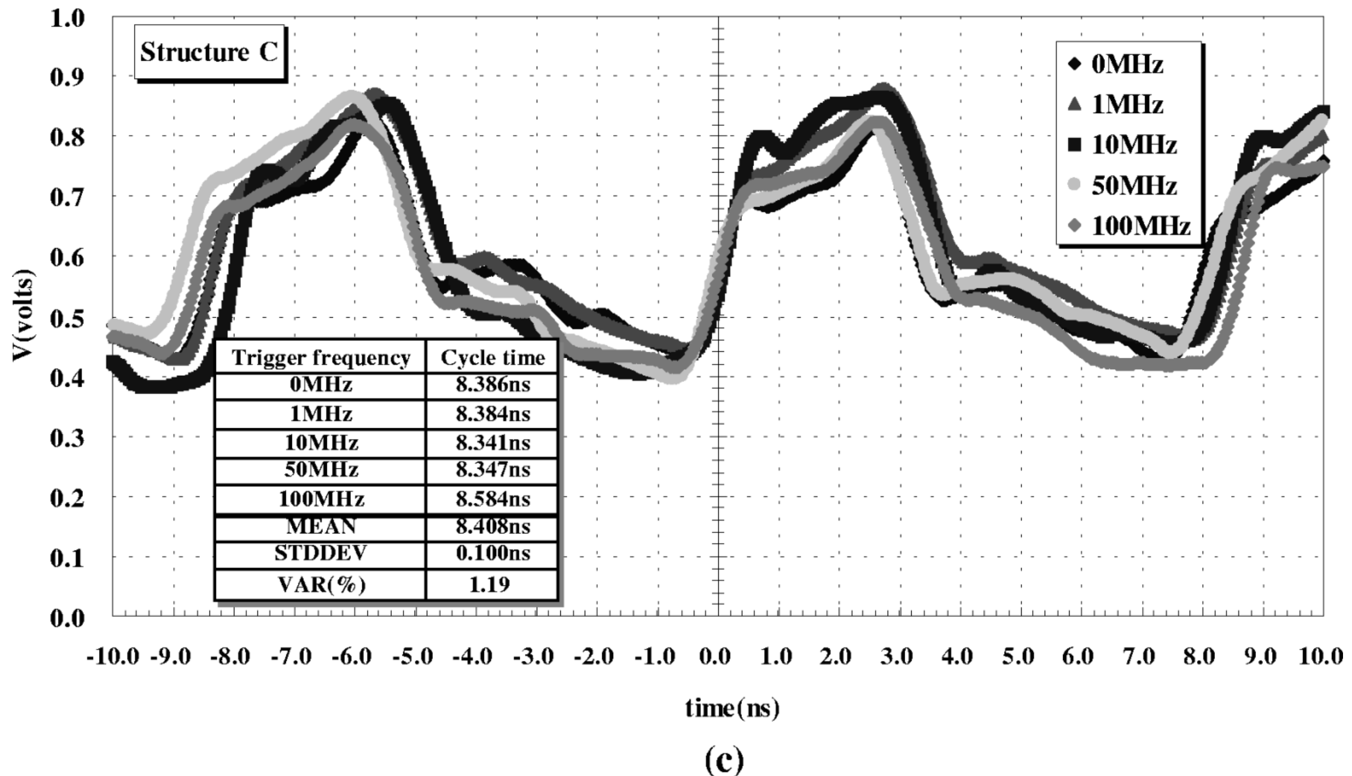
Trigger frequency	Cycle time
0MHz	8.290ns
1MHz	8.320ns
10MHz	8.093ns
50MHz	8.030ns
100MHz	8.283ns
MEAN	8.203ns
STDDEV	0.132ns
VAR(%)	1.61

Fig. 8. Output waveforms for (a) Structure A, (b) Structure B, and (c) Structure C, measured by an oscilloscope, while a 1.2 V, 50% duty cycle voltage pulse at frequencies of 0, 1, 10, 50, and 100 MHz is applied. Insets are cycle times that correspond to triggering frequencies, as well as their mean values, standard deviations. These data do not significantly differ from each other.

8.203 ns and Structure C has a means cycle time of 8.408 ns. Even the standard deviations in the cycle time are the same for all structures. Thus, these ring-oscillator devices under CMOS I/O bonding pads are concluded to be insensitive to signal coupling from the disturbance running through I/O bonding pads and are independent of the number of bonding pad metal levels.

IV. Conclusion

The 1.2 μm aluminum metal film, formed on the top copper metal film, serves as a very effective buffer layer against bonding stress, supporting the implementation of active devices under CMOS I/O bonding pads using 130 nm full eight-level



Trigger frequency	Cycle time
0MHz	8.386ns
1MHz	8.384ns
10MHz	8.341ns
50MHz	8.347ns
100MHz	8.584ns
MEAN	8.408ns
STDDEV	0.100ns
VAR(%)	1.19

Fig. 8. *(Continued.)* Output waveforms for (a) Structure A, (b) Structure B, and (c) Structure C, measured by an oscilloscope, while a 1.2 V, 50% duty cycle voltage pulse at frequencies of 0, 1, 10, 50, and 100 MHz is applied. Insets are cycle times that correspond to triggering frequencies, as well as their mean values, standard deviations. These data do not significantly differ from each other.

copper metal/FSG low-k IMD CMOS technology. Also, active devices under CMOS I/O bonding pads have substantially eliminated the conventional I/O bonding pad design constraints, and can improve the usage of chip area in future SOC designs.

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Kuo-Yu Chou is currently pursuing the Ph.D. degree in electronic engineering at National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

From 1996 to 2001, he was with the Research and Development Department, Taiwan Semiconductor Manufacturing Company, Hsinchu. His research interests include test chip and test structure designs for evaluating the development of the advanced CMOS technologies and reliability of the deep-submicron CMOS devices. He holds one U.S. patent and one Taiwanese patent in CMOS technology.

Ming-Jer Chen (S'78–M'79–SM'98) received B.S. degree in electrical engineering (with highest honors) in 1977 from National Cheng-Kung University, Taiwan, R.O.C., and the Ph.D. degree in electronics engineering in 1985 from National Chiao-Tung University (NCTU), Hsinchu, Taiwan.

In 1985, he joined the faculty of the Department of Electronics Engineering, NCTU, where he became a full Professor in 1993. From 1987 to 1992, he was a principal consultant for TSMC, where he led a team from NCTU and ERSO/ITRI to build up a series of process window and design rule. In 1996 and 1997, he critically enabled the ERSO/ITRI video A/D converter and TSMC mixed-mode CMOS processes, respectively. In the 2000–2001 academic year, he was a Visiting Professor at the Department of Electrical Engineering and Center for Integrated Systems, Stanford University, Stanford, CA. His research interests have long focused on technology reliability physics and currently on nanoscale electronics. He has graduated ten Ph.D. students and 80 M.S. students, and has been granted six U.S. patents and six Taiwanese patents in the above areas.

Dr. Chen received the 1992 and 1993 Chinese Young Engineering Paper Award and the 1996 Acer Distinguished Dissertation Award. He is a member of Phi Tau Phi.

Chi-Wen Liu received the B.S. degree in materials engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C, in 1988 and the M.S. degree in mechanical engineering and the Ph.D. degree in electronic engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1990 and 1996.

Since 1994, he was with the Research and Development Department, Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan. He is currently a Senior Engineer in Fab III with TSMC and is also teaching semiconductor engineering and electronic materials courses in the Department of Electrical Engineering, National Chi-Nan University, Nan-Tou, Taiwan. His current research interests include copper-related modules, low-k materials, and interconnection reliability. He has authored eight papers and holds nine patents on wafer clean, implant, Cu surface protection, CMP, FSG, and barrier materials.