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# The performance of GaAs power MESFET's using backside copper metallization

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## Abstract

The performance of GaAs power MESFET's using backside copper metallization has been evaluated. 10 nm Ta metal was used as the diffusion barrier between GaAs and Cu for copper film metallization in this study. Microstructural characterization shows that the Cu/Ta films with GaAs remained stable up to 400 °C, indicating that Ta is a good diffusion barrier for Cu in GaAs MESFET's. A copper metallized 6 mm power MESFET was thermal stressed to test the device stability. After annealing at 200 °C for 3 h, the devices showed very little degradation in power performance, and the thermal resistance of the device was 65 °C mm/W with 1.4 W/mm DC input power. Results in this study demonstrate that the feasibility of using Cu/Ta films for the backside metallization of GaAs power devices with stable electrical and thermal characteristics.

*Keywords:* Copper metallization; GaAs power MESFET; Thermal resistance

## 1. Introduction

Copper metallization has been extensively used in silicon IC technology to improve circuit performance. GaAs device with Cu metallization using Ta or TaN as a diffusion barrier have been recently reported [1–3]. Conventionally, GaAs FET's and MMIC's used Au as the metallization metal for transmission lines and ground plane metallization. Use copper as the metallization metal instead of gold has the following advantages: (1) a lower resistivity, (2) higher thermal conductivity, (3) lower cost, and (4) better mechanical properties when plated more thickly, made possible by the lower cost. Copper diffuses very fast into GaAs and is a deep acceptor, so copper metallization of GaAs devices without a diffusion barrier degrades their electrical properties. In our previous studies [1,2], 40 nm Ta metal was used as the diffusion barrier to Cu and the material system exhibited good thermal stability up to 500 °C. MESFET's metallized using this Cu/Ta layers showed small changes in electrical parameters after annealing at 300 °C for 2 h. The magnitude of the changes of the electrical parameters and RF characteristics of the devices including source saturation current ($I_{\mathrm{dss}}$), transconductance ($G_{\mathrm{m}}$), pinch off voltage ($V_{\mathrm{p}}$), cut off frequency ($f_{\mathrm{T}}$) and maximum oscillation frequency ($f_{\max}$) is of the same order as that for devices without copper metallization. Thus the deterioration of the characteristics after annealing is caused primarily by the thermal effect on the properties intrinsic to the device itself, and backside copper metallization negligibly affects the performance of a GaAs device. This study examines the stability of the materials system and performance of the copper metallized power MESFET's devices using a thin 10 nm layer of Ta. (In our previous studies [1–3], the

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individual device were neither sliced nor packaged). To our knowledge, this study describes the power performance, including the thermal stability and the thermal resistance for the first time.

## 2. Device fabrication and metallization

The MESFET's used were typical epitaxial-material based power MESFET's. The fabrication of the MESFET's included mesa isolation, Au/Ge/Ni ohmic metallization, recessed gate with Au/Pt/Ti metals, plasma enhanced chemical vapor deposition silicon nitride passivation and the Au plated air bridges. 3 in. GaAs MESFETs wafer was mounted on a 4-inch quartz plate, and then mechanically thinned to only 75 μm before metallization. Backside copper metallization of the power MESFET's was performed in a DC multitarget magnetron sputtering system. A 10 nm thick Ta film, followed by a 3 μm Cu film was sputtered onto the GaAs substrate, without breaking the vaccum. The base pressure was $2.6 \times 10^{-5}$ Pa before sputtering, and the total sputtering gas pressure was 0.8 Pa during the deposition of the films. The backside copper was then patterned with photoresist, and the cutlines of each device were etched away using $HNO_3$ solution ($HNO_3$:$H_2O$ = 1:3). The wafer was then demounted from the quartz plate and the individual device was sliced apart by a dicing saw. Finally the devices were packaged (as in traditional Au metallization) and were annealed at 200 °C for 3 h in vacuo for power performance and thermal resistance testing. Fig. 1 schematically depicts the structure of the MESFET's with copper backside metallization.

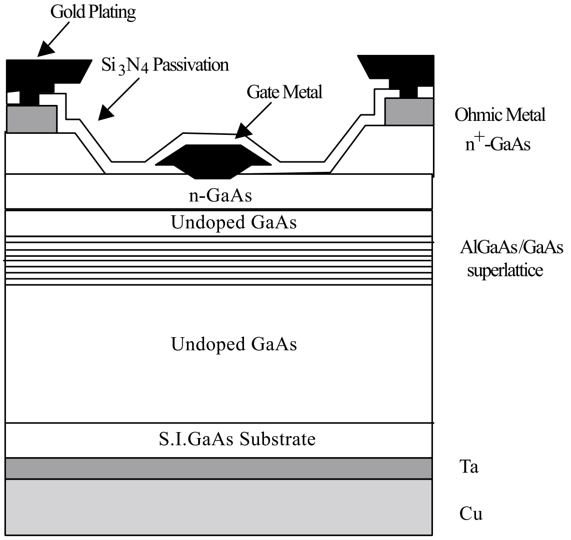

Fig. 1. Structure of the GaAs power MESFET with backside Cu metallization.

## 3. Thermal stability of Cu/Ta/GaAs multilayers

A blank GaAs wafer with Cu/Ta films was used for materials characterization. Before metal film deposition, the GaAs substrates were cleaned with boiling acetone and isopropyl alochol each for 5 min and dipped with $HF$:$H_2O_2$:$H_2O$ (1:2:20) for 20 s and $HCl$:$H_2O$ (1:4) for 1 min. The blank wafer was sputtered at the same time as the processed MESFET wafer. Fig. 2 shows the X-ray

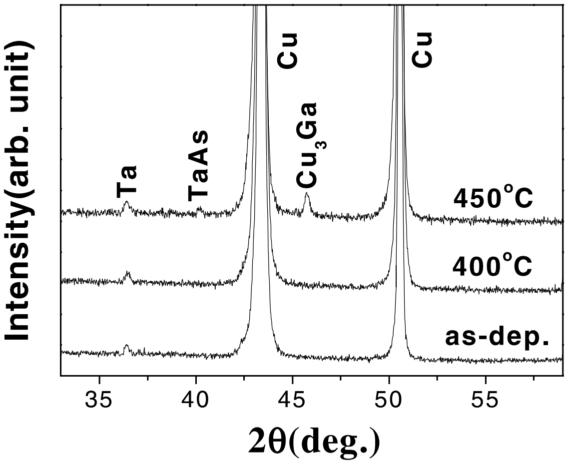

Fig. 2. XRD pattern of the samples as-deposited and annealed at various temperatures.

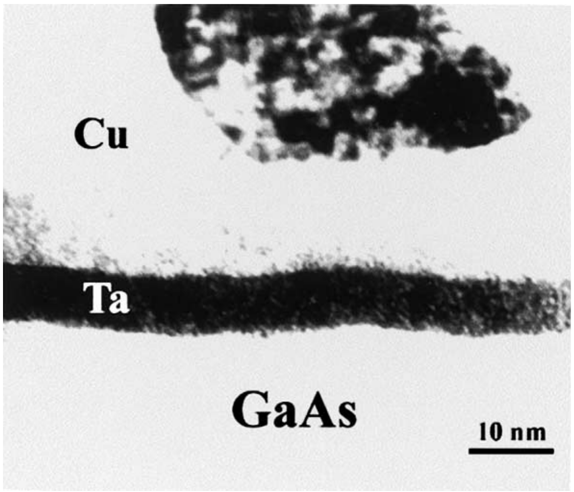

Fig. 3. Cross-sectional TEM micrograph of Cu/Ta/GaAs multilayers after 400 °C annealing.

diffraction (XRD) results of the Cu/Ta/GaAs samples as-deposited and annealed for 30 min in vacuo at temperatures ranging from 400 to 450 °C. The XRD data clearly show that the peaks of Ta and Cu remain unchanged until the temperature reaches 400 °C, indicating that the Cu/Ta/GaAs structure remains quite stable up to 400 °C. After annealing at 450 °C, new phases of TaAs and $Cu_3$ Ga are identified, suggesting that reactions between the substrate and the metallization layers occurred. Fig. 3 presents a cross-sectional transmission electron microscopy (TEM) micrograph of the Cu/Ta/GaAs structure after 400 °C annealing. The micrograph shows that grain growth of the Cu and Ta occurred, and that the interfaces between Cu, Ta and GaAs were still quite sharp without intermixing of the Cu and Ta barrier layers with the GaAs substrate.

## 4. Power performance

The power performance of the MESFETs was measured at 1.9 GHz with a drain bias of 7 V before annealing. Thermal stability testing was performed on the devices annealed at 200 °C for 3 h. Fig. 4 plots the output power, power-added efficiency and power gain as functions of input power for a 6 mm-wide device before and after annealing. The device was operated under class AB condition with a bias drain current of 600 mA and was tuned for maximum output power. Before annealing the maximum output power was 28.53 dBm and the power added efficiency of the device at the maximum output power was 59.55%. The linear gain was 16.48 dB. After the device was annealed at 200 °C for 3 h, the maximum output power was 30.21 dBm and the power added efficiency of this device at the maximum output power was 61.05%. The linear gain was 15.94 dB. The degradation in power performance of the power MESFET after thermal annealing is seen to be very slight.

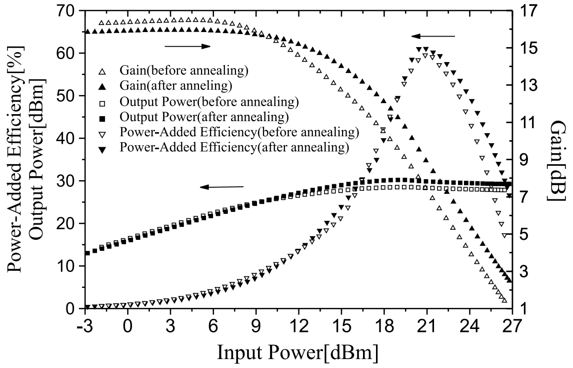

Fig. 4. Output power and power added efficiency and gain as a function of input power for 6 mm power MESFET at 1.9 GHz with drain bias of 7.0 V.

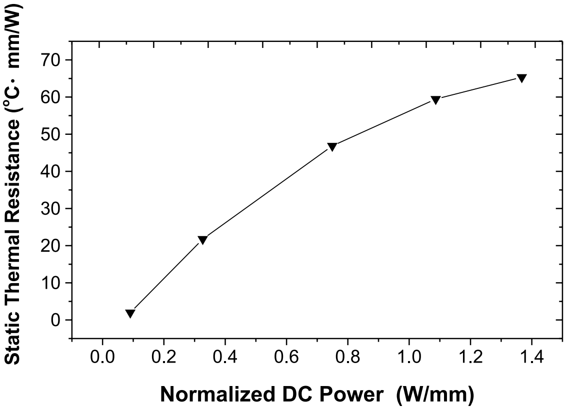

Fig. 5. Thermal resistance data at different DC power levels for 6 mm copper metallized MESFET.

## 5. Thermal resistance

The heat transport characteristics of the backside copper metallized MESFET were elucidated using the thermal resistance method. The backside of the device was placed in contact with a heat sink maintained at room temperature. The surface temperature was measured using an infrared thermal image system which was operated at a fixed DC input power. The temperature of the surface of the MESFET varied according to the DC input power at which it was operated. The static thermal resistance is defined as $\Theta = T - T_0/P_{\mathrm{dc}}$ [4], where $P_{\mathrm{dc}}$ is the dc power dissipation, and $T_0$ is the reference temperature. Fig. 5 shows the calculated static thermal resistance over a range of input power. The thermal resistance increased with input power. The 6 mm-wide MESFET with backside copper metallization had a thermal resistance of 65 °C mm/W when the DC power was 1.4 W/mm. The data show that the thermal performance is similar to that of the MESFET metallized using Au [4]. The results demonstrate that the Cu/Ta films can be used for backside metallization on GaAs devices with good thermal stability.

## 6. Conclusions

Backside copper metallization with Ta as the diffusion barrier layer was successfully applied to GaAs power MESFET's. The 10 nm Ta barrier for Cu metallization was very stable up to 400 °C. MESFET's metallized using Cu/Ta layers exhibited good power performance and thermal conductance and demonstrated excellent thermal stability after thermal stress. To our knowledge, this study examines the thermal stability of backside copper metallized power MESFET's for the first time. Results in this study demonstrate that Cu/Ta layers are thermally stable and can be used in GaAs power device metallization.

## Acknowledgements

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