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# Structural Fault Based Specification Reduction for Testing Analog Circuits

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**Abstract.** Specification reduction can reduce test time, consequently, test cost. In this paper, a methodology to reduce specifications during specification testing for analog circuit is proposed and demonstrated. It starts with first deriving relationships between specifications and parameter variations of the circuit-under-test (CUT) and then reduces specifications by considering bounds of parameter variations. A statistical approach by taking into account of circuit fabrication process fluctuation is also employed and the result shows that the specification reduction depends on the testing confidence. A continuous-time state-variable benchmark filter circuit is applied with this methodology to demonstrate the effectiveness of the approach.

**Keywords:** analog test, test cost reduction, specification-based test, fault-based test

## 1. Introduction

Analog circuit testing has been a difficult problem, primarily due to the non-deterministic nature of component parameters and limited accessibility of internal nodes for the CUT. Analog testing techniques are traditionally classified into two categories, i.e., structural (fault)-oriented testing and functional (specification)-based testing. For the structure-oriented testing, a fault model, usually at the circuit level, is adopted and patterns (signals) are applied to the CUT to exploit the specific structural difference between the defective and non-defective circuits. However, there are no universally accepted fault models for analog circuits because the nature of analog faults is not constant and cannot be definitely and precisely modeled. For the functional-based testing, it is to measure some specified performance specifications of the CUT, such as DC gain, cut-off frequency, and slew rate, etc., and to determine "pass" or "fail" of the CUT based on whether the measured results are within specified ranges. This test approach is straightforward and is easy to be applied. However, it lacks precise metrics to indicate the structural fault coverage and is inherently expensive since it involves expensive dedicated test equipment and long testing time.

Several researches [1, 10, 17] that alleviate the difficulty of test generation, fault classification, test quality improvement for analog and mixed-signal testing have been presented by linking the information of structural fault and circuit specifications. One important goal on testing research is to reduce the test time. In the digital

domain, this corresponds to deriving the efficient test set which maximizes fault detection. In the analog domain, due to the difficulty in defining faults as mentioned above, there were only a few works on this topic. Huss et al. [4] studied the problem by ordering specification tests so that faulty circuits are detected early in the test sequence to reduce the average test time. This approach is efficient to reduce test time if a CUT is defective but does not gain advantage when the circuit is normal. Milor and Sangiovanni-Vincentelli [9] also proposed an algorithm for finding an ordering of specification tests to increase the efficiency of the functional testing. This algorithm eliminates the non-critical specifications based on the yield prediction but it is hard to derive the accurate yield and it is time-consuming when correlations between specifications are considered. Souders and Stenbakken [15] presented an approach to select a minimal set of basis vector to calculate the entire behavior for analog-to-digital converter. This method reduces the test time but needs extra internal test points for the CUT. Lindermeir et al. [7] proposed a characteristic observation inference test design approach for analog circuit. For the approach, for each given specification, it simulates training samples and computes a test inference criterion based on a logistic discrimination analysis. With obtained test criteria, satisfaction or violation of the original circuit specifications are inferred from characteristic observations of the circuit under test.

In this paper, we approach this problem by studying the relationship between the performance specifications with component parameters of the analog CUT and reaching the conclusion that some of specifications of the circuit can be removed for the testing purpose. By removing the specification, the testing time can be reduced. Also, a statistical approach is employed by taking into account of circuit fabrication process fluctuation to show that the specification reduction depends on the testing confidence.

The paper is organized as follows: The fault model and the procedure to derive the relationships between analog faults and specifications are first presented with a simple low pass filter as an illustration example. Then, Monte Carlo simulation is used to find the effect of the manufacturing process fluctuation on the above relationships, and a specification reduction procedure is described. An illustrative case study on the continuous-time state-variable filter benchmark circuit [6] is included to demonstrate the effectiveness of the approach.

## 2. Mapping Between Faults and Specifications

As mentioned previously, there is no universal and well-defined fault model for testing analog circuits. A common practice is to resort to the circuit level to define a fault to be an "open" or "short" of a circuit component such as a resistor, capacitor or a transistor etc. (catastrophic faults), or a deviation on the value of the above circuit components (parametric faults). These faults are used because they generally can be clearly attributed from physical manufacturing defects and deduced from the computer-aided analysis such as Inductive Fault Analysis (IFA) [8, 11, 14, 18]. They are relatively well defined and easier to be handled. They can be served as a metric for evaluating the testing coverage and the effectiveness of tests for testing analog circuits. It has been shown [9, 16] that parametric faults are significantly more important to be considered since they dominate catastrophic faults and are harder to be detected. In this work, specifications are studied to be reduced while considering parametric faults as the metric. Circuit parameters such as resistances, capacitances, inductances passive components and $V_T$ (threshold voltage), $W$ (channel width) and $L$ (channel length) of the MOS transistors are within their allowable range, i.e. within specified fluctuations of the manufacturing process. When a parametric fault occurs, possibly caused by a local defect or manufacturing equipment error, the value of the circuit parameter is outside of the range of the specified range.

### 2.1. Mapping Specifications to Circuit Parameters

Consider a circuit of $\boldsymbol{m}$ parameters, $\boldsymbol{P} = [p_1, p_2, \ldots, p_m]$, where $p_i$ could be resistances of resistor, capacitance of capacitor, $W/L$ ratio of transistor, and $V_T$ of transistor, etc. The performance of the circuit is bounded by $\boldsymbol{n}$ specifications, $\boldsymbol{S} = [s_1, s_2, \ldots, s_n]$. $\boldsymbol{S^u} = [s_1^u, s_2^u, \ldots, s_n^u]$ and $\boldsymbol{S^l} = [s_1^l, s_2^l, \ldots, s_n^l]$ are denoted to the upper and lower bounds for these specifications. For the design with the nominal $\boldsymbol{P}$ value: $\boldsymbol{P^0} = [p_1^0, p_2^0, \ldots, p_m^0]$, we can find a corresponding point, $\boldsymbol{S^0} = [s_1^0, s_2^0, \ldots, s_n^0]$, in the specification space. Fig. 1 shows the abstract graph of mapping between the parameter space and the specification space. Also, it is an aim to conversely find the accepted tolerances of parameters from the allowed ranges of specifications.

Under the single fault assumption, the accepted tolerance of each parameter can be obtained through deduction if the relationship between specifications and

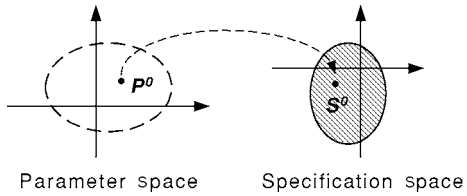



*Fig. 1.* Mapping between the parameter and the specification space [10, 17].

parameters are explicit and simple or through simulation combined with back-inference. A simple example will be used to explain this later.

For a specification, say, the $j$th specification $s_j \in \boldsymbol{S}$, it is a function of all parameters $p$'s. If, under the single fault condition, we consider parameter $p_i$, $s_j$ can be represented as $s_j(p_i) = f(p_1, p_2, \ldots, p_{i-1}, p_i, p_{i+1}, \ldots, p_m)$ where all $p_i$'s are fixed except $p_i$ which is allowed to vary. We assume that $s_j$ is bounded by $s_j^u$ and $s_j^l$, the accepted process tolerance range of $p_i$ for $s_j$ can be deduced by solving the inequalities:

$$s_j(p_i) = f\left(p_1^0, p_2^0, \ldots, p_{i-1}^0, p_i, p_{i+1}^0, \ldots, p_m^0\right) \le s_j^u$$
$$s_j(p_i) = f\left(p_1^0, p_2^0, \ldots, p_{i-1}^0, p_i, p_{i+1}^0, \ldots, p_m^0\right) \ge s_j^l$$

We denote the obtained upper and lower bounds of accepted range of $p_i$ for $s_j$ to be $p_{ij}^u$ and $p_{ij}^l$ respectively.

A simple low pass filter of Fig. 2 is used as the example to explain as follows:

The transfer function of the low pass filter is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-R_2/R_1}{1 + sCR_2}$$

Assume that the parameters we consider are $R_1$, $R_2$, and $C$ and the specifications are DC gain $A_0$, cut-off frequency $f_c$, input resistance $R_{in}$, respectively. For $R_1 = 2\,(\mathrm{M}\Omega)$, $R_2 = 2\,(\mathrm{M}\Omega)$, and $C = 100\,(\mathrm{pF})$, $A_0 = |\frac{-R_2}{R_1}| = 1$, $f_c = \frac{1}{2\pi R_2 C} = 795.8\,(\mathrm{Hz})$ and $R_{in} = R_1 =$ 2 (MΩ). The ranges for each specification are as shown in the figure. By solving $0.8 \le s_1(p_1) = |\frac{-2\,(\mathrm{M}\Omega)}{R_1}| \le 1.2$, we obtain that the accepted range of $p_1$ for $s_1$ is $1.667\,(\mathrm{M}\Omega) \le R_1 \le 2.5\,(\mathrm{M}\Omega)$, i.e., $p_{11}^u = 2.5\,(\mathrm{M}\Omega)$ and $p_{11}^l = 1.667\,(\mathrm{M}\Omega)$. The upper and lower bounds of accepted range of $R_1$ for $s_2$ is $p_{12}^u = \infty$ and $p_{12}^l = -\infty$ since $s_2(p_1) = \frac{1}{2\pi R_2 C}$ is independent of $R_1$. Similarly, we can obtain $p_{13}^u = \infty$, and $p_{13}^l = 1\,(\mathrm{M}\Omega)$ by solving $s_3(p_1) = R_1 \ge 1\,(\mathrm{M}\Omega)$.

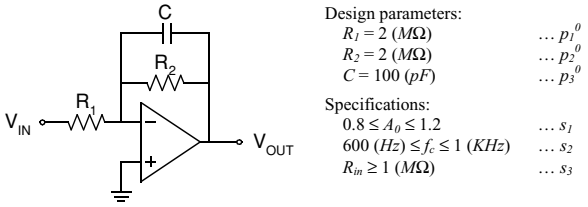



*Fig. 2.* A low pass filter example to explain the deduction of relationship between parameters and specifications.

The above deductive approach is efficient if the relationships between parameters and specifications are explicit and simple. However, these relationships are usually implicit and hard to be derived when circuits are large and active components are involved. For these cases, simulation-based approach needs to be used. That is: the deviations of specifications w.r.t. parameters are directly simulated. The relationships between specifications and parameters can be obtained in table or curve forms and bounds of the parameters can be found by applying the constraints of specifications on these relationships. Fig. 3 shows such a curve of specification $A_o$ of the low pass filter circuit of Fig. 2 w.r.t. parameter $R_1$. The upper and lower bounds for $R_1$ for this specification $A_o$ can be extracted to be 2.5 and 1.67 (MΩ) respectively. In a similar way, the bounds of all other parameters w.r.t. the respective specifications can be derived and are shown in Table 1.

### 2.2. *Procedure of Specification Reduction*

A circuit is defined as "*fault-free*" if it satisfies all the constraints of specifications. Thus, the *final* upper ($p_i^u$)

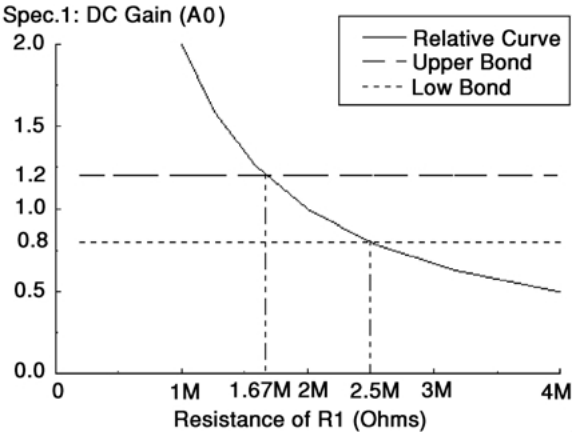



*Fig. 3.* Relationship curve of specification $A_o$ w.r.t. parameter $R1$ of the example circuit of Fig. 2.

*Table 1*. Upper and lower bounds of $R_1$, $R_2$ and $C$ w.r.t. specifications $A_0$, $f_c$ and $R_{in}$.

| | $A_0$ | | $f_c$ | | $R_{in}$ | |
|---|---|---|---|---|---|---|
| | LB | UB | LB | UB | LB | UB |
| $R1$ (Ω) | 1.67 M | 2.5 M | $-\infty$ | $\infty$ | 1 M | $\infty$ |
| $R2$ (Ω) | 1.6 M | 2.4 M | 1.58 M | 2.65 M | $-\infty$ | $\infty$ |
| $C$ (F) | $-\infty$ | $\infty$ | 79.3 p | 133 p | $-\infty$ | $\infty$ |

UB: upper bound. LB: lower bound.

*Table 2*. Tolerance range and the most significant specifications for decreasement and increasement faults of each parameter.

| | FLB | $ELBS_i$ | FUB | $EUBS_i$ |
|---|---|---|---|---|
| $R1$ (Ω) | 1.67 M | $s1$ | 2.5 M | $s1$ |
| $R2$ (Ω) | 1.6 M | $s1$ | 2.4 M | $s1$ |
| $C$ ($F$) | 79.3 p | $s2$ | 133 p | $s2$ |

FLB: final lower bound; FUB: final upper bound.

and lower bounds ($p_i^l$) of accepted range for $i$th parameter should be:

$$p_i^u = \text{minimum}\left(p_{i1}^u, p_{i2}^u, \ldots, p_{in}^u\right)$$
$$p_i^l = \text{maximum}\left(p_{i1}^l, p_{i2}^l, \ldots, p_{in}^l\right)$$

For the low pass filter example shown above, the final upper and lower bounds of $R_1$ should be given to be minimum(2.5 MΩ, $\infty$, $\infty$) $\Rightarrow$ 2.5 (MΩ) and maximum(1.67 MΩ, $-\infty$, 1 MΩ) $\Rightarrow$ 1.67 (MΩ) respectively. Hence, if the resistance deviation, caused by a defect, of $R_1$ is within the range of 2.5 (MΩ) and 1.67 (MΩ), the circuit will pass all specifications $s1$, $s2$ and $s3$ and will be considered to be good.

In the above, $s1$ is the most significant specification in determining the lower bound for the $R_1$ decreasement fault since it is the specification which determines the lower bound for $R_1$. This specification is the "Essential Lower Bound Specification for parameter $i$", denoted to be $ELBS_i$, which is given by the general form:

$$ELBS_i = s_j|_{p_{ij}^l = p_i^l,\ \forall j}$$

Similarity, the "Essential Upper Bound Specification for parameter $i$", the most significant specification for $i$th parameter increasement fault, denoted by $EUBS_i$, is given by:

$$EUBS_i = s_j|_{p_{ij}^u = p_i^u,\ \forall j}$$

As a result, the "Essential Test Specifications", the indispensable specifications for all parameter faults, denote by $ETS$, will be the union of all ELBSs and EUBSs:

$$ETS = \bigcup_{i=1}^{m} \{ELBS_i \cup EUBS_i\}$$

Table 2 summarizes the tolerance range of all parameters and the most significant specifications for the decreasement and the increasement faults of each parameter. From the table, apparently, $s1$ and $s2$ are the essential test specifications which need to be considered in testing as all the parameters: $R1$, $R2$, and $C$ are considered, but $s3$ can be ignored. That is: specifications are reduced from $s1$, $s2$, and $s3$ to $s1$ and $s2$.

## 3. The Impact of Manufacturing Process Fluctuations

As feature size of MOSVLSI moves into the deep submicron range, the device characteristics and yield become more sensitive to manufacturing process fluctuations. When there are variations in the parameter space due to the process fluctuation, correspondingly, there will be variations on the specification space of the circuit. The specification and the parameter relationship such as that of Fig. 3 will become a band instead of a single curve due to value variations, which are caused by the process fluctuation, of all parameters as shown in Fig. 4. If the variations of all parameters are assumed to be random, the distribution of the band will be Gaussian [2]. There may be a probability, which is small, that the circuit, originally considered to be good, will not pass the specification due to the process fluctuation. If there is a fault on $R_1$, i.e., it deviates to a value, for example, 1.67 (MΩ), the probability that the circuit will not pass $A_0$ becomes even larger. However, there may be also a small probability that the circuit still pass $A_0$ due to value variations of other parameters caused by the process fluctuation even though $R_1$ is faulty.

The above is explained in Fig. 5 for a general case: Generally, specification $s_j$ has a distribution, due to the process fluctuation, with respect to parameter $p_i$, in the

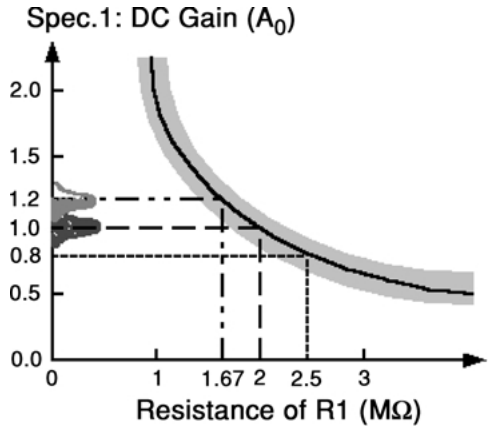



*Fig. 4.* The relationship between specification $A_0$ and parameter $R_1$ becomes a band due to the process fluctuation.

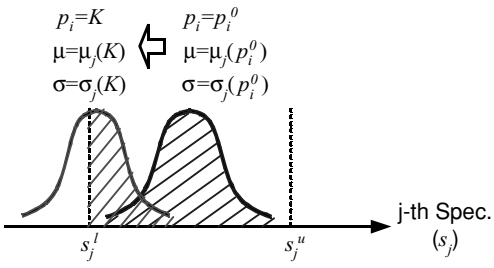



*Fig. 5.* The distributions of a specification due to parameter variations for the normal circuit ($p_i = p_i^0$) and the faulty circuit ($p_i = K$). There is probability that the normal circuit does not pass the specification due to the parameter variations, and for the faulty circuit, there still also exists a small probability that the circuit pass the specification.

following form:

$$s_j(x, p_i) = \frac{1}{\sqrt{2\pi}\sigma_j(p_i)} e^{\frac{-(x-\mu_j(p_i))^2}{2\sigma_j^2(p_i)}} \tag{1}$$

where $x$ is the value of specification $s_j$ located, $\mu_j$ is the mean value and $\sigma_j^2$ is the variance of specification $s_j$. If there is a fault on $p_i$, i.e., $p_i$ deviates to a new value, $K$, $s_j$ will have a new distribution but with a form similar to that of Eq. (1). That the circuit passes specification $s_j$ is $s_j^l \le s_j(x, p_i) \le s_j^u$. Hence, the probability that the circuit passes $s_j$ when $p_i = K$, represented as $Prob(p_i = K \xrightarrow{pass} s_j)$, is:

$$Prob\big(p_i = K \xrightarrow{pass} s_j\big) = \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{s_j^l}^{s_j^u} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx \tag{2}$$

And, the probability of failing to pass $s_j$ is

$$\begin{aligned} &Prob\big(p_i = K \xrightarrow{fail} s_j\big) \\ &\quad = \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{-\infty}^{s_j^l} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx \\ &\qquad + \frac{1}{\sqrt{2\pi}\sigma_j(K)} \int_{s_j^u}^{\infty} e^{\frac{-(x-\mu_j(K))^2}{2\sigma_j^2(K)}} dx \end{aligned} \tag{3}$$

Naturally,

$$Prob\big(p_i = K \xrightarrow{pass} s_j\big) + Prob\big(p_i = K \xrightarrow{fail} s_j\big) = 1 \tag{4}$$

The above probabilities can be obtained either directly from the relationship between the specification and the parameter of the circuit or computed through Monte Carlo simulation. In the previous low pass filter circuit, if $\mu$ and $\pm 3\sigma$ of $R_1$ distribution are 2 (MΩ) and $\pm 10\%$ respectively, the probability curves, computed both from equation derivation (solid line) and computer simulation (dotted line), of the circuit to pass specification ($0.8 \le A_0 \le 1.2$) are shown in Fig. 6 with respect to the value of $R_1$.

In the above curves it can be seen that, when $R_1$ equals to its nominal value (=2 MΩ) and all other

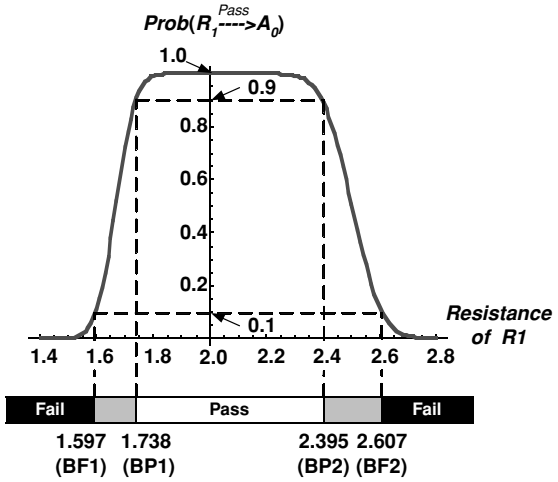



*Fig. 6.* Probability of the low pass circuit to pass specification $A_0$ with respect to the value of $R_1$, where the nominal value is 2.0 (MΩ). Bounds for parameter $R_1$ to pass or fail $A_0$ during testing for a 90% confidence level are shown. The central region is the pass region, the two outside regions are fail regions, and the two gray regions are uncertain regions.

parameters vary randomly within their respective $\pm 3\sigma$ around their nominal values, the filter always pass specification $A_0$, but will only "partially" pass $A_0$ if $R_1$ is smaller than 1.8 (MΩ) or larger than 2.3 (MΩ). For example, if $R_1 = 2.4$ (MΩ), the circuit has an approximate 90% probability to pass $A_0$, and if $R_1 = 1.6$ (MΩ), it only has an approximate 10% probability to pass this specification. If $R_1$ is greater than 2.7 (MΩ) or smaller than 1.5 (MΩ) the circuit will definitely fail to pass $A_0$.

The bounds of accepted and rejected range for parameters can be obtained by solving Eqs. (2) and (3) under a given testing confidence (that is, after the testing, even if the circuit passes all specification tests, the circuit still has a certain probability of not working). For example, if the testing confidence is 90%, four bounds solved for $R_1$ for $A_0$ are shown in Fig. 6. They are BF1 = 1.597 (MΩ), BP1 = 1.738 (MΩ), BP2 = 2.395 (MΩ) and BF2 = 2.607 (MΩ) respectively, where BF1 and BF2 are the lower and upper boundary values respectively of the fail band, and BP1 and BP2 are lower and upper boundary values respectively of the pass region. The circuit will pass $A_0$ (the DC gain specification) with over a 90% probability when $R_1$ is between BP1 = 1.738 (MΩ) and BP2 = 2.395 (MΩ), and will fail, with over a 90% probability, if $R_1$ is below BF1 = 1.597 (MΩ) or over BF2 = 2.607 (MΩ). Within the two gray regions, i.e., BF1 = 1.597 (MΩ) and BP1 = 1.738 (MΩ), and BP2 = 2.395 (MΩ) and BF2 = 2.607 (MΩ), the circuit cannot be determined to be "pass or fail" due to random variations, which are caused by the process fluctuation, of other parameters. If we reduce the testing confidence, these two regions will shrink. For example, if we only ask for a testing confidence of 50%, these two regions will shrink to zero and the problems of setting the fault boundaries, consequently the specification reduction, will be simplified to that as stated previously in Section 2.

For the general $i$th parameter ($p_i$) for the $j$th specification, we denote the above four bounds to be $BP1_{ij}$, $BP2_{ij}$, $BF1_{ij}$, and $BF2_{ij}$ respectively. If a circuit is fault-free, it should satisfy "all" specifications, and the bounds of the accepted range for the $i$th parameter are given by:

$$BP1_i = \text{maximum}(BP1_{i1}, BP1_{i2}, \ldots, BP1_{in})$$
$$BP2_i = \text{minimum}(BP2_{i1}, BP_{i2}, \ldots, BP2_{in})$$

On the other hand, a circuit is considered to be faulty if it violates one of specifications. Hence, the bounds

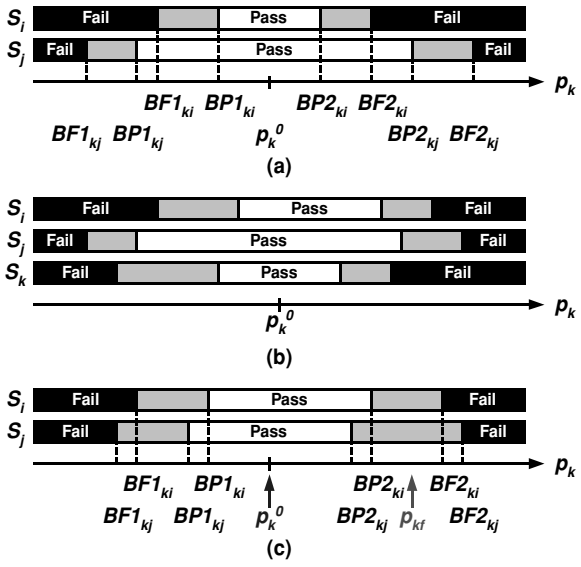



*Fig. 7.* Elimination of specifications based on the locations of pass, fail, and uncertain regions between specifications for a parameter $p_k$.

of rejected range for the $i$th parameter are:

$$BF1_i = \text{maximum}(BF1_{i1}, BF1_{i2}, \ldots, BF1_{in})$$
$$BF2_i = \text{minimum}(BF2_{i1}, BF2_{i2}, \ldots, BF2_{in})$$

Hence, a specification $S_i$ can be neglected, for a parameter $p_k$, when its bounds of pass range are outside bounds of another specification $S_j$ since a circuit which passes $S_j$ will always pass $S_i$ as shown in Fig. 7(a). For the case in Fig. 7(b), $S_j$ can be ignored because it is "dominated" by $S_i$ for $p_k$ lower bound fault and, on the other hand, "dominated" by $S_k$ for $p_k$ upper bound fault. However, for the case of Fig. 7(c), neither $S_j$ nor $S_k$ can be neglected since there are overlap between their respective gray regions. When the parameter value, for example, $p_{kf}$, falls into these gray regions, there is always a probability that the CUT will not pass either of the specifications.

Hence, for the testing purpose, we can define "redundancy" for specifications as following:

*Definitions.*

(a) A specification $S_j$ is "lower bound redundant" for a parameter $p_k$, if a specification $S_{i,i\neq j}$ exists such that $BF1_{ki} \geq BP1_{kj}$.
(b) A specification $S_j$ is "upper bound redundant" for a parameter $p_k$, if a specification $S_{i,i\neq j}$ exists such that $BP2_{kj} \geq BF2_{ki}$.

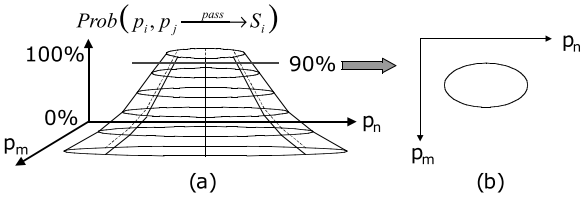



*Fig. 8.* (a) The 2-dimensional probability bell for passing specification $S_j$ test for the double-parameters ($p_m$, $p_n$) fault; (b) The circlet, which is cut from the 2-dimensional cone of (a) for a test confidence of 90%.

(c) A specification is "redundant" for testing, i.e., it can be removed, if it is both lower bound redundant and upper bound redundant for all parameters.

In above, we presented the approach of specification reduction based on soft (parametric) faults. However, the above approach also applies to hard faults since when a hard fault occurs, the circuit often fails at least one specification.

In the above, in order to obtain the probability curves, Monte Carlo simulation needs to be done, which is a time consuming process. Time complexity may be a problem large size circuits are considered. One approach to alleviate this difficulty is to partition the CUT into several small blocks and the simulation is done hierarchically [3].

Also, in the above, we deal with only single parameter fault [5, 13]. When more than two parameter faults are considered, the case will be more complex. To explain, for simplicity, a double fault ($p_m$, $p_n$) case is used as an example. When a double parameters fault is considered, the probability curve for one specification, say $S_i$, will become a three-dimensional cone as shown in Fig. 8(a) rather than the two-dimensional curve of Fig. 6. For a given confidence level, a circlet will be cut on the cone as shown in Fig. 8(b). Similarly, when another specification, saying $S_j$ is also considered for reduction, another circlet can also be obtained. If the circlet of $S_j$ covers the circlet of $S_i$, then $S_j$ is dominated by $S_i$ for this double ($p_m$, $p_n$) fault. As a result, $S_j$ can be neglected when testing for the double-parameter fault.

## 4. Example

To further illustrate the above specification reduction approach, a benchmark continuous-time state-variable filter circuit [6], as shown in Fig. 9(a), is used to demonstrate the procedure, as well as its efficiency.

For this circuit, the band-pass output (BPO) is taken as the output and R1 = R2 = R3 = R4 = R6 = 1 M, C1 = C2 = 200 p, R6 = 300 K, and R7 = 700 K. The central frequency for the band-pass output (BPO), $f_c = (2\pi\sqrt{R3C1R4C2})^{-1} = 795$ Hz with a gain equal to 1.11. The frequency response of the circuit is shown in Fig. 9(b). The operational amplifiers in this circuit are the benchmark operational amplifier [6], as shown in Fig. 10. It is adopted for the purpose to make the study more practical. The technology file used for all computer simulation in the study is TSMC CMOS 0.8 um SPDM technology file of under a $\pm$2.5 V supply voltage. The specifications of the filter are shown in Table 3.

With the fault model described previously, the number of parameters ($R$, $C$, and $W/L$ and $V_T$ of each transistor) is 66. To study the effects on specifications of all the faults of parameters, a Monte Carlo simulation by considering a 10% ($=3\sigma$) variation on parameter values has been performed. Table 4 summarizes the simulated results where the mean and variance of each specification are listed. The results are in two groups: one group is for parameters in operational amplifiers, and the other group is for passive component parameters outside operational amplifiers. In the table, the variance of each specification caused by the parameters inside operational amplifiers is much smaller than that caused by the passive components outside operational amplifiers. This is obvious since devices and components in an operational amplifier are insensitive to the characteristics of the operational amplifier due to negative feedback. Hence, in the forgoing study, only the passive components (R1–R7, C1, C2) outside operational amplifiers are considered.

Table 5 shows the bounds (BF1, BP1, BP2, BF2) obtained from simulations for all specifications w.r.t. C1 under 99%, 90% and 50% testing confidence. From the table, it is seen that C1 is insensitive to specifications 1 and 7 because, even if a large deviation occurs in C1, the circuit always passes testing for these specifications. Also, decreasing the testing confidence reduces the uncertain ranges (BF1–BP1 and BP2–BF2) and a 50% testing confidence gives a zero uncertain range. The essential lower bound specification (*ELBS*) and essential upper bound specification (*EUBS*) for C1 are also derived. For the 99% testing confidence case, the maximum{BF1's} is 154 (pF) from specification S2 (this means that if a defect causes C2 smaller than 154

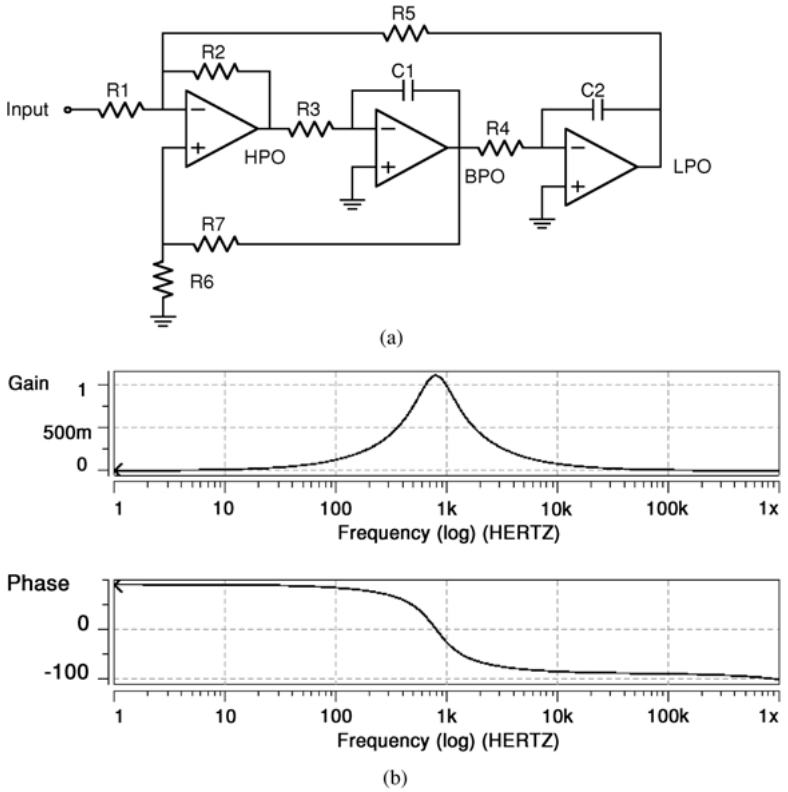
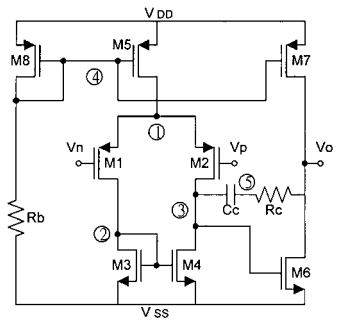



*Fig. 9.* (a) The circuit of the benchmark continuous-time state-variable filter. (b) Frequency response of band-pass output.

(pF), there is a 99% probability that the circuit will fail the test). However, for S1, S3, S6, S7, S9 and S10, their BP1 values are all smaller than 154 (pF), i.e., these specifications can be ignored when considering the C1 decrease fault. Hence, the *ELBS*'s are S2, S4, S5 and S8. On the other hand, the EUBS's are S2, S4, S5, S6 and S9 because their BF2 values are smaller than the minimum$\{$BF2's$\} = 260$ (pF), which is derived from




| Compenent | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | Cc | Rc | Rb |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Width (μm) | 60 | 60 | 27.5 | 27.5 | 35 | 300 | 200 | 15 | 1.27 pF | 8.75 k | 110 k |
| Length (μm) | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | | | |

*Fig. 10.* Schematic representation and element values of benchmark CMOS operational amplifier.

*Table 3.* Specifications of the filter circuit and their nominal values (NV), lower bounds (LB), and upper bounds (UB).

| Specifications | NV | UB | LB |
|---|---|---|---|
| S1: Gain @ $f_c$ | 1.11 | 1.3 | 1 |
| S2: Central frequency ($f_c$) | 794 | 900 | 700 |
| S3: Low cutoff frequency | 515 | 600 | 400 |
| S4: High cutoff frequency | 1231 | 1400 | 1000 |
| S5: 3 dB bandwidth | 716 | 1000 | 500 |
| S6: Quality factor | 1.11 | 1.3 | 0.9 |
| S7: Gain @ 100 Hz | 0.13 | 0.2 | 0 |
| S8: Gain @ 700 Hz | 1.07 | $\infty$ | 0.9 |
| S9: Gain @ 900 Hz | 1.07 | $\infty$ | 0.9 |
| S10: Gain @ 10 KHz | 0.08 | 0.2 | 0 |

*Table 4*. Means and variances of specifications caused by variations of device parameters inside operational amplifiers and by passive component parameters outside operational amplifiers.

| | Caused by the variations of device parameters in opamps | | Caused by the variations of passive $R$ and $C$ outside opamps | |
|---|---|---|---|---|
| Specifications | Mean | Variance | Mean | Variance |
| S1: Gain @ $f_c$ | 1.11 | $2.19 \times 10^{-9}$ | 1.10 | $2.19 \times 10^{-3}$ |
| S2: Central frequency ($f_c$) | 794 | $6.40 \times 10^{-25}$ | 793 | 1150 |
| S3: Low cutoff frequency | 515 | $7.82 \times 10^{-5}$ | 512 | 555 |
| S4: High cutoff frequency | 1231 | $5.17 \times 10^{-4}$ | 1228 | 3361 |
| S5: 3 dB bandwidth | 716 | $9.71 \times 10^{-4}$ | 716 | 2340 |
| S6: Quality factor | 1.11 | $2.33 \times 10^{-9}$ | 1.11 | $3.60 \times 10^{-3}$ |
| S7: Gain @ 100 Hz | 0.13 | $1.16 \times 10^{-13}$ | 0.13 | $5.64 \times 10^{-5}$ |
| S8: Gain @ 700 Hz | 1.07 | $1.74 \times 10^{-9}$ | 1.06 | $2.41 \times 10^{-3}$ |
| S9: Gain @ 900 Hz | 1.07 | $1.75 \times 10^{-9}$ | 1.05 | $2.46 \times 10^{-3}$ |
| S10: Gain @ 10 KHz | 0.08 | $2.67 \times 10^{-13}$ | 0.08 | $2.6 \times 10^{-5}$ |

*Table 5*. Bounds of pass and fail range for all specifications w.r.t. C1 under 99%, 90% and 50% testing confidence (unit: pF) ($\infty$ : infinity).

| | 99% confidence | | | | 90% confidence | | | | 50% confidence | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Spec. | BF1 | BP1 | BP2 | BF2 | BF1 | BP1 | BP2 | BF2 | BF1 | BP1 | BP2 | BF2 |
| S1 | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ |
| S2 | 154 | 158 | 256 | 260 | 156 | 156 | 256 | 260 | 156 | 156 | 258 | 258 |
| S3 | 74 | 152 | 278 | 586 | 92 | 134 | 348 | 518 | 114 | 114 | 432 | 432 |
| S4 | 150 | 184 | 228 | 312 | 158 | 176 | 246 | 294 | 168 | 168 | 270 | 270 |
| S5 | 130 | 156 | 244 | 330 | 136 | 150 | 262 | 310 | 144 | 144 | 286 | 286 |
| S6 | 116 | 148 | 244 | 294 | 122 | 142 | 256 | 282 | 132 | 132 | 270 | 270 |
| S7 | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ | $-\infty$ | $-\infty$ | $\infty$ | $\infty$ |
| S8 | 44 | 176 | 336 | 476 | 74 | 148 | 368 | 444 | 110 | 110 | 406 | 406 |
| S9 | 18 | 90 | 228 | 314 | 28 | 68 | 248 | 296 | 42 | 42 | 272 | 272 |
| S10 | 76 | 84 | $\infty$ | $\infty$ | 78 | 82 | $\infty$ | $\infty$ | 80 | 80 | $\infty$ | $\infty$ |

S2 also. Combining *ELBS*'s and *EUBS*'s, we obtain the essential test specifications (ETS) for the C1 deviation fault are S2, S4, S5, S6, S8 and S9.

In a similar way, the ETS's for all component parameters can be obtained. The final reduced test specification set is a set of the union of the ETS's of all component parameters. Table 6 shows the ETS's for all component parameters, the final reduced test specifications and the ignored test specifications under 99%, 90% and 50% testing confidence, respectively. It can be seen that in general certain number of test specifications can be reduced for a component parameter and when all parameters are considered, there are still some specifications can be ignored. Also, as the testing confidence is decreased, the number of ignored specifications increases.

To study the effect of hard faults, a total of 36 short (bridging) faults between nine circuit nodes (4 internal nodes, HPO, BPO, LPO, input and ground) are simulated. For a short fault, a short resistance of 10 ($\Omega$) is assumed. Table 7 lists the number of short faults detected when all the above specifications are considered. All of 36 short faults can be detected. Even for S1 testing, it can detect 33 faults and for S2 testing, it can detect 32 faults. With S1 and S2 testing simultaneously, all 36 short faults are detected. This demonstrates that

*Table 6*. Essential test specifications for each component parameter under 99%, 90% and 50% testing confidence.

| Component | 99% confidence | 90% confidence | 50% confidence |
|---|---|---|---|
| R1 | 1, 4, 6, 8, 9 | 1, 8, 9 | 1 |
| R2 | 1, 2, 3, 4, 5, 8, 9 | 1, 2, 3, 4, 8, 9 | 4, 9 |
| R3 | 2, 3, 4, 5, 6, 8, 9 | 2, 4, 6, 9 | 2, 4 |
| R4 | 2, 3, 4, 8, 9 | 2, 3, 8 | 2, 3 |
| R5 | 1, 2, 3, 4, 8, 9 | 1, 2, 3, 4, 8 | 2, 8 |
| R6 | 1, 3, 4, 5, 6, 8, 9 | 1, 6, 8, 9 | 1 |
| R7 | 1, 3, 4, 5, 6, 8, 9 | 1, 6, 8, 9 | 1 |
| C1 | 2, 4, 5, 6, 8, 9 | 2, 4, 6, 9 | 2, 4 |
| C2 | 2, 3, 4, 8, 9 | 2, 3, 8 | 2, 3 |
| Final test specs. | 1, 2, 3, 4, 5, 6, 8, 9 | 1, 2, 3, 4, 6, 8, 9 | 1, 2, 3, 4, 8, 9 |
| Ignored test specs. | 7, 10 | 5, 7, 10 | 5, 6, 7, 10 |

*Table 7*. Number of detected hard faults for each specification.

| Specifications | All spec. | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S1 + S2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Detected | 36 | 33 | 32 | 31 | 32 | 31 | 32 | 17 | 32 | 32 | 15 | 36 |

the specification test can easily detect hard faults. If a hard fault can not be detected by all specification test, this fault can be effectively considered as a redundant fault since it does not affect the performance of the circuit.

## 5. Conclusion

In this paper, we have presented an approach to reduce the number of test specifications for analog circuits. The approach starts with derivation of the relationship between specifications and device and/or component parameters then defines upper and lower bounds for parameters to find essential test specifications. Then the variations on component parameters due to fabrication process fluctuations are considered by using a statistical model to reduce test specifications with a testing confidence probability. A continuous time state-variable filter example circuit has been used to demonstrate the specification reduction procedure and it has been shown that 2, 3 or 4 out of 10 specifications can be ignored during specification testing under the 99%, 90% and 50% testing confidence level respectively. The procedure is effective and can be used in manufacturing specification test for analog circuits to reduce test time.

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