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Novel Implantation Method to Improve Machine-Model Electrostatic Discharge Robustness of Stacked N-Channel Metal-Oxide Semiconductors (NMOS) in Sub-Quarter-Micron Complementary Metal-Oxide Semiconductors (CMOS) Technology

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A novel ion implantation method for electrostatic discharge protection, often called as ESD implantation, is proposed to significantly improve machine-model (MM) ESD robustness of N-channel metal-oxide semiconductors (NMOS) device in stacked configuration (stacked NMOS). By using this ESD implantation method, the ESD current is discharged far away from the surface channel of NMOS, therefore the stacked NMOS in the mixed-voltage I/O interface can sustain a much higher ESD level, especially under the MM ESD stress. The MM ESD robustness of the stacked NMOS with a device dimension of $W/L = 300\,\mu\text{m}/0.5\,\mu\text{m}$ for each NMOS has been successfully improved from the original 358 V to become 491 V in a 0.25-μm complementary metal-oxide semiconductors (CMOS) process. [DOI: 10.1143/JJAP.41.L1288]

KEYWORDS: electrostatic discharge (ESD), ESD protection, machine model, ESD implantation, stacked NMOS

Component-level electrostatic discharge (ESD) stresses on IC products had been classified as three models:[1)] the human-body model (HBM), the machine model (MM), and the charged device model (CDM). The ESD voltage ratio between the HBM and MM ESD robustness of complementary metal-oxide semiconductors (CMOS) IC products were around $\sim$10 in the submicron (1.0–0.5 μm) CMOS processes. Typically, a CMOS IC product, which has a HBM ESD robustness of 2 kV, can sustain a MM ESD stress of 200 V. However, this ratio has approached to about 15–20 in the sub-quarter-micron CMOS processes. The MM ESD robustness of IC products has been found to degrade much worse than its HBM ESD robustness in the sub-quarter-micron CMOS processes. How to effectively improve MM ESD robustness of IC products has become a challenge in the sub-quarter-micron CMOS processes.

In order to enhance ESD robustness, some ESD implantations had been reported for including into process flow to modify the device structures for ESD protection.[2–4)] The N-type ESD implantation was used to cover the lightly-doped drain (LDD) peak structure and to make a deeper junction in N-channel metal-oxide semiconductors (NMOS) device for ESD protection.[2)] The P-type ESD implantation with a higher concentration located under the drain junction of NMOS was used to reduce the junction breakdown voltage and to earlier turn on the parasitic lateral BJT of the NMOS.[3)] Moreover, both of the N-type and P-type ESD implantations were used in NMOS device to wish a higher ESD robustness.[4)] The experimental results to compare the effectiveness among those ESD implantation methods had been investigated in a 0.18-μm CMOS process.[5)]

In the mixed-voltage circuit application, the stacked NMOS structure had been widely used in the mixed-voltage I/O buffer[6)] to solve the gate-oxide reliability issue without using the additional thick gate-oxide process (or called as dual gate oxide in some CMOS process), or even used in the power-rail ESD clamp circuit.[7)] Unfortunately, in such mixed-voltage I/O circuits the stacked NMOS often have much lower ESD level, as compared to the buffer with single NMOS.[8,9)] To improve the ESD robustness of the stacked NMOS in the mixed-voltage I/O interface, ESD implantation method is the method without occupied extra silicon area to enhance ESD robustness.

In this letter, a novel ESD implantation method to especially improve machine-model (MM) ESD robustness of stacked NMOS is proposed and verified in a 0.25-μm CMOS process.

The ESD current waveforms through the gate-grounded NMOS (ggNMOS) under 4-kV HBM and 400-V MM ESD stresses are measured in Figs. 1(a) and 1(b), respectively. The measurement setup is shown in the inserted block in Fig. 1(a). Such HBM and MM ESD events are generated by the ZapMaster (from KeyTek Inc.), which is a typical ESD tester widely used to verify ESD robustness of IC products. The measured current peak of 4-kV HBM ESD stress in Fig. 1(a) is 3.54 A, whereas that of 400-V MM ESD stress in Fig. 1(b) is 4.94 A. Comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak and a shorter current pulse width than those of HBM ESD stress. The rise time of MM ESD current is also faster than that in HBM ESD stress. This implies that MM ESD events generate more heat in a shorter time period on the ggNMOS. So, the ggNMOS is easily burned out by such a faster MM ESD current, and cause a much lower ESD robustness. MM ESD robustness of IC products will be degraded much worse than its HBM ESD robustness in the sub-quarter-micron CMOS processes.

In submicron CMOS technology, the NMOS fabricated with LDD structure to overcome the hot-carrier issue often leads to a lower ESD robustness. To improve ESD robustness, the traditional ESD implantation with n-type impurity on the stacked NMOS is shown in Fig. 2(a), where the N_ESD impurity in sub-quarter-micron CMOS process often has a lower concentration than that of N+ drain/source diffusion to overcome the hot-carrier issue. To significantly improve MM ESD robustness of the stacked NMOS, a new ESD implantation method is proposed in Fig. 2(b), where the spacing "S" is the

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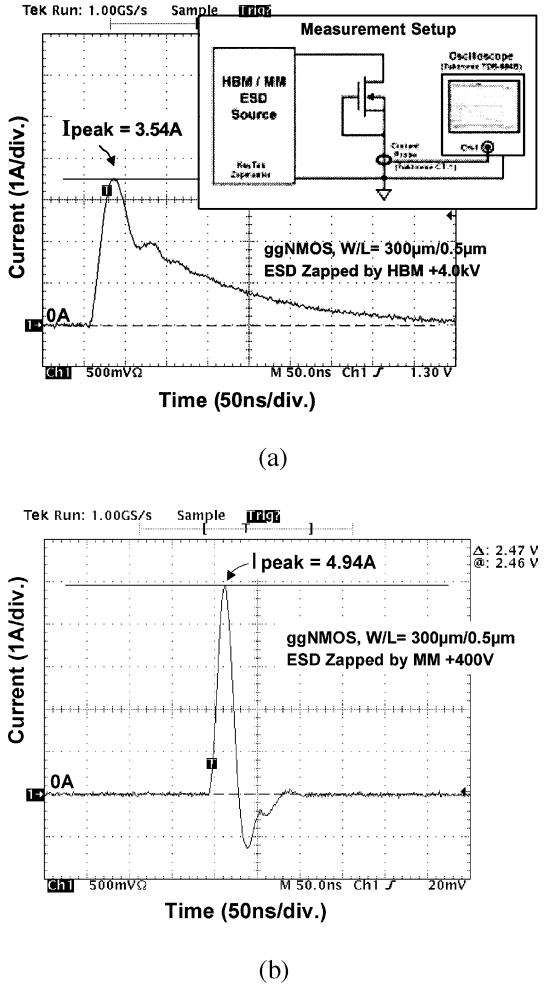

Fig. 1. The measured ESD current waveforms through a ggNMOS ($W/L = 300\,\mu$m$/0.5\,\mu$m) zapped by (a) the human-body-model ESD stress of 4 kV, and (b) the machine-model ESD stress of 400 V.

important layout parameter to be investigated in the 0.25 μm CMOS processes. In Fig. 2(b), the ESD implantation region covers the whole drain region of the stacked NMOS, but except the region around the drain contact. This ESD implantation region in this experimental test chip has a lighter doping dosage of 1×10^{15} ions/cm^2 and a junction depth of $\sim0.2\,\mu$m. The drain/source N+ diffusion for the normal NMOS device has a doping dosage of 5×10^{15} ions/cm^2 and a junction depth of $\sim0.18\,\mu$m. The junction covered by the proposed ESD implantation method has an increased junction breakdown voltage. But, the region without covering by this ESD implantation has the original junction breakdown voltage.

When a positive ESD voltage is zapped to the pad with the VSS relatively grounded. The drain of stacked NMOS is stressed by the ESD voltage and therefore breaks down to clamp the overstress voltage on the pad. The region, which is not covered by the N_ESD implantation, has a lower junction breakdown voltage. So, the ESD current is first discharged through this region to generate the substrate current (Itrig) to quickly trigger on the parasitic lateral n-p-n BJT in the stacked NMOS structure. ESD current is mainly discharged through this lateral n-p-n BJT in the stacked NMOS, where such ESD current path is far away from the weakest surface channel of the stacked NMOS. With the self-generated substrate triggering current, the lateral n-p-n BJT

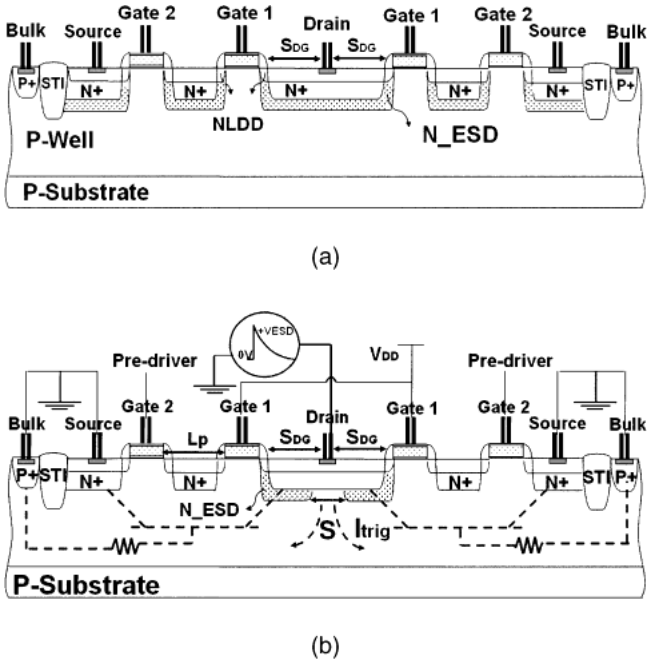

Fig. 2. (a) The traditional ESD implantation with n-type impurity for improving ESD robustness of the stacked NMOS. (b) The new proposed ESD implantation method to significantly improve machine-model ESD robustness of stacked NMOS. The spacing "S" is the important layout parameter to be investigated.

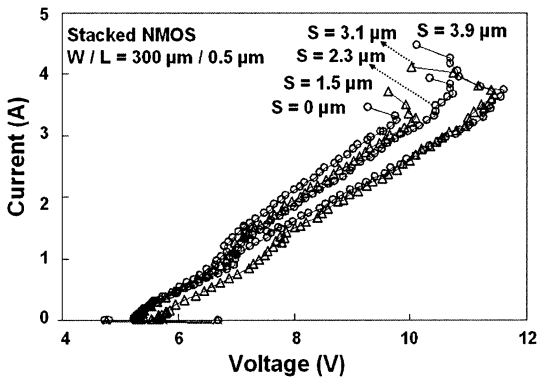

Fig. 3. The TLP-measured I–V curves of the stacked NMOS with the proposed ESD implantation under different layout spacing "S".

in the stacked NMOS structure can be fully turned on more quickly.[10] So, the faster transient current of MM ESD events can be quickly discharged through the lateral n-p-n BJT in the stacked NMOS structure. This causes a significant improvement on ESD robustness of the stacked NMOS in the mixed-voltage I/O interface, especially during the MM ESD zapping.

To investigate the effectiveness of the new proposed ESD implantation method, the stacked NMOS with different layout spacing of "S" in Fig. 2(b) had been fabricated in a 0.25-μm CMOS process with shallow trench isolation. The transmission-line-pulse (TLP) generator[11] with a pulse width of 100 ns is used to measure the secondary breakdown current (It2) of the fabricated stacked NMOS. The TLP-measured I–V curves of stacked NMOS ($W/L = 300\,\mu$m$/0.5\,\mu$m) with the new ESD implantation method are shown in Fig. 3 under different layout spacing "S". While the spacing S is increased, the It2 of the stacked NMOS is increased.

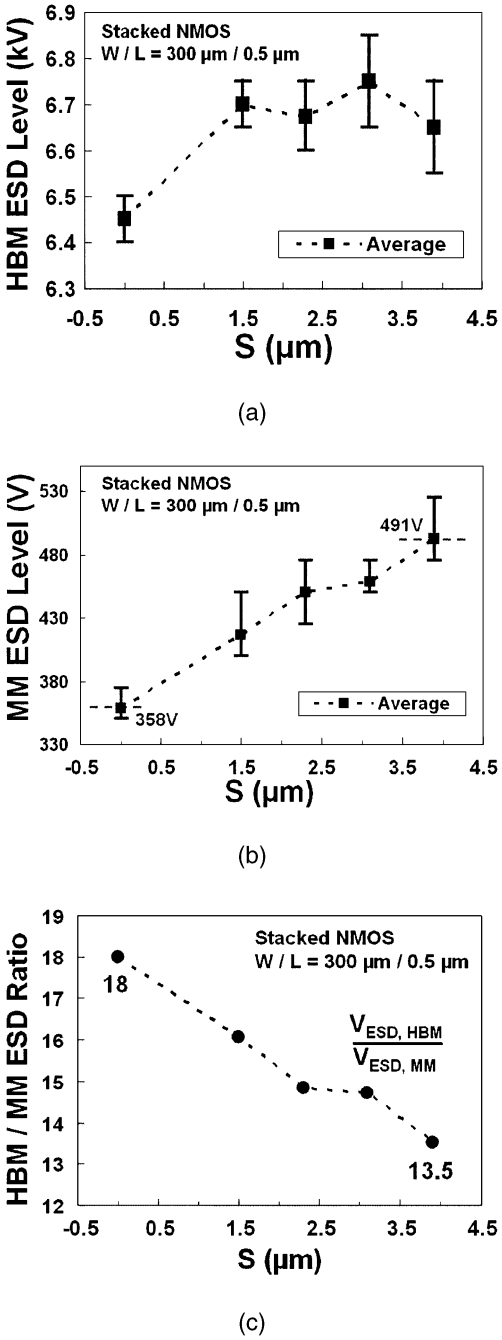

Fig. 4. The dependences of (a) the HBM ESD level, (b) the MM ESD level, and (c) the HBM/MM ratio, on the layout spacing "S" of the stacked NMOS fabricated with the proposed ESD implantation method.

The dependences of HBM and MM ESD levels and the HBM/MM ESD level ratio on the layout spacing "S" are measured by the ZapMaster ESD simulator, and the results are shown in Figs. 4(a), 4(b), and 4(c), respectively. The drain diffusion of the stacked NMOS has a fixed spacing of 5.7 μm for all devices in the experimental test chips. The spacing (S_{DG}) from drain contact to poly gate edge is 2.4 μm, and the spacing (L_p) between poly gate 1 and poly gate 2 is 0.4 μm. While the spacing S is increased, the HBM and MM ESD levels of stacked NMOS are also increased. The HBM/MM ESD level ratio shown in Fig. 4(c) has verified that the MM ESD robustness of the stacked NMOS can be significantly improved by this new proposed ESD implantation method under a wider layout spacing S. The MM ESD level of the stacked NMOS with W/L of 300 μm/0.5 μm has been successfully increase from the original 358 V (with $S = 0$) to become 491 V (with $S = 3.9\,\mu$m), where the MM ESD level is improved 37% by this new proposed ESD implantation method. The HBM ESD level of the stacked NMOS is also slightly improved from the original 6.45 kV (with $S = 0$) to become 6.65 kV (with $S = 3.9\,\mu$m) by this method. Consequently, the HBM/MM ESD level ratio can be really reduced to $\sim$13.5 when the spacing S is drawn with 3.9 μm.

The actual ESD current discharging waveforms of HBM and MM ESD events on ggNMOS has been measured and compared to find the difference. A new ESD implantation method is proposed to improve HBM and MM ESD levels of stacked NMOS in the mixed-voltage I/O interface. Especially, this method can significantly increase ESD level of stacked NMOS under the MM ESD zapping. The experimental results shown in this work is the first report in the literature to specially increase MM ESD robustness in CMOS technology. This ESD implantation method is fully processes compatible to general sub-quarter-micron CMOS processes.

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