Role of Positive Trapped Charge in Stress-Induced Leakage Current for Flash EEPROM Devices

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***Abstract*—The transient behavior of hot hole (HH) stress-induced leakage current (SILC) in tunnel oxides is investigated. The dominant SILC mechanism is positive oxide charge-assisted tunneling (PCAT). The transient effect of SILC is attributed to positive oxide charge detrapping and thus the reduction of PCAT current. A correlation between SILC and stress-induced substrate current is observed. Our study shows that both SILC and stress-induced substrate current have power law time-dependence t^{-n} with the power factor n about 0.7 and 1, respectively. Numerical analysis for PCAT current incorporating a trapped charge caused Coulombic potential in the tunneling barrier is performed to evaluate the time- and field-dependence of SILC and the substrate current. Based on our model, the evolution of threshold voltage shift with read-disturb time in a Flash EEPROM cell is derived. Finally, the dependence of SILC on oxide thickness is explored. As oxide thickness reduces from 100 Å to 53 Å, the dominant SILC mechanism is found to change from PCAT to neutral trap-assisted tunneling (TAT).**

***Index Terms*—Flash EEPROM, positive trapped charge, read-disturb, stress-induced leakage current (SILC), substrate current, transient behavior.**

I. Introduction

HIGH-FIELD stressing during program/erase (P/E) cycles in Flash EEPROM operation can lead to a significant increase in low-level leakage current in tunnel oxide. Such stress-induced leakage current (SILC) has received a lot of attention because of its significance to endurance and data retention of a Flash memory cell. Several mechanisms have been proposed for SILC, including positive charge-assisted tunneling (PCAT) [1], [2], neutral trap-assisted tunneling (TAT) [3], and thermally-assisted tunneling at weak spots of the Si/SiO_2 surface due to a barrier height lowering [4]. Despite extensive research on SILC, the role of positive trapped charge in SILC and related read-disturb in a Flash cell is still not clear. DiMaria *et al.* concluded from their experimental result that positive oxide charge plays no part in SILC conduction in oxides by Fowler–Nordheim (FN) stress [5]. Dumin [6] and Ricco [7] showed that neutral TAT is the original cause of SILC for oxide thickness from 40 Å to 130 Å. The concept of inelastic TAT in SILC was proposed by Takagi *et al.* [8] and is supported by the temperature-dependence of SILC [9], the $1/f$ noise of the tunneling current [10], and the energy-loss measurement [11]. On the other side, Teramoto *et al.* claimed that excess leakage current induced by FN stress is attributed to injected holes produced by high-energy electrons [12]. Shuto *et al.* found that hot hole (HH) injection during source-side FN erase is the major cause for read-disturb degradation in Flash cells [13]. Matsukawa *et al.* further showed that SILC caused by positive oxide charge can be reduced by hot electron injection or ultraviolet irradiation [14]. The more recent result of Meinertzhagen *et al.* [15] has revealed that the role of positive oxide charge in SILC changes with stress and measurement polarities.

In addition, Dumin *et al.* found that FN SILC contains a dc component, as well as a transient component [16]. In this work, the dc component is attributed to neutral TAT. The transient part is realized due to oxide trap charging and discharging and can be characterized by $1/t$ time-dependence based on the tunneling front model [16]. A threshold voltage shift of 1.0 V resulting from the transient part of SILC in a Flash cell was reported by Kato *et al.* [17]. Although tremendous efforts have been made to investigate the SILC mechanisms and characteristics, most of previous studies were conducted on a MOS capacitor with uniform FN stress. In order to correlate with edge FN erase-induced degradation in Flash EEPROM cells, the transient behavior of SILC by band-to-band HH stress will be explored.

In this paper, various stacked gate Flash cells and conventional gate nMOSFETs were used. To measure FN SILC and HH SILC directly, nMOSFETs with a long source/drain edge were specially fabricated. The test devices have a gate length of 0.6 μm and a total gate area of 9×10^{-4} cm^2. The gate oxide thickness ranges from 53 Å to 100 Å. In theoretical part, we develop a transient model to calculate the electron and hole leakage components in SILC. In our model, a Coulombic potential caused by a positive trapped charge is included in the tunneling barrier. Image force and surface quantization effects are taken into account. The Wentzel–Kramer–Brillouin (WKB) method is used to evaluate electron and hole tunneling rates. In measurement, a charge separation technique is employed to characterize individual electron and hole components in SILC. The measured HH SILC will be analyzed with respect to time-, field-, and oxide thickness-dependence.

II. Hot Hole SILC Characterization

The transient behavior of SILC by positive FN stress and band-to-band HH stress is shown in Fig. 1. The oxide thickness is about 100 Å. The +FN stress is performed at $V_{\mathrm{gs}} = 9.5$ V for 2000 s. The band-to-band HH stress is at $V_{\mathrm{gs}} = -3$ V and $V_{\mathrm{ds}} = 6$ V for 500 s. Under the two stress conditions, oxide

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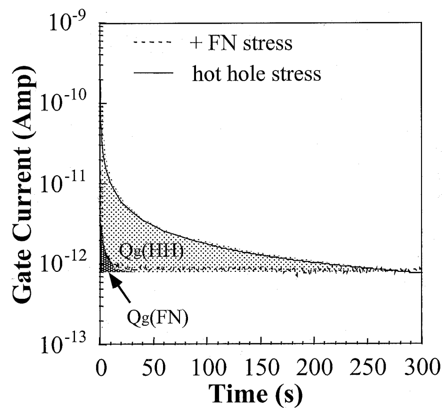

Fig. 1. Measured gate current transients in +FN stressed and HH stressed nMOSFETs. The oxide field in measurement is about 6.5 MV/cm. The shaded areas $Q_g(\mathrm{HH})$ and $Q_g(\mathrm{FN})$ represent total charge flowing to the gate carried by the transient component of the SILC in the measurement period.

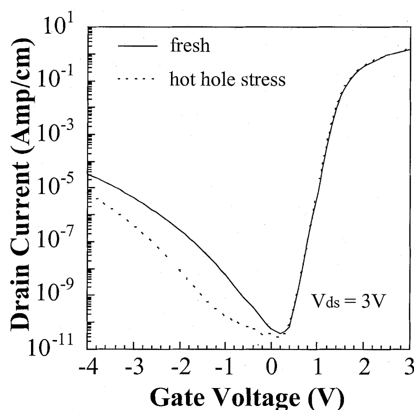

Fig. 2. Drain current versus gate bias in a nMOSFET before and after band-to-band HH stress. After stress, GIDL current shifts to the left due to positive oxide charge creation and V_t is unchanged.

TABLE I
MEASURED Q_g AND Q_{ox} IN HH STRESSED AND FN STRESSED nMOSFETS. Q_g IS NORMALIZED TO A STRESSED GATE AREA. THE HH STRESS REGION IN THE CHANNEL IS ASSUMED TO BE 0.2 μm. e DENOTES AN ELEMENTARY CHARGE (1.6×10^{-19} C)

	Qg (e/cm^2)	Qox (e/cm^2)	$\lvert Qg / Qox \rvert$
HH	$1.35\text{x}10^{13}$	$1.2\text{x}10^{12}$	11.25
FN	$2.1\text{x}10^{11}$	$-1.3\text{x}10^{12}$	0.16

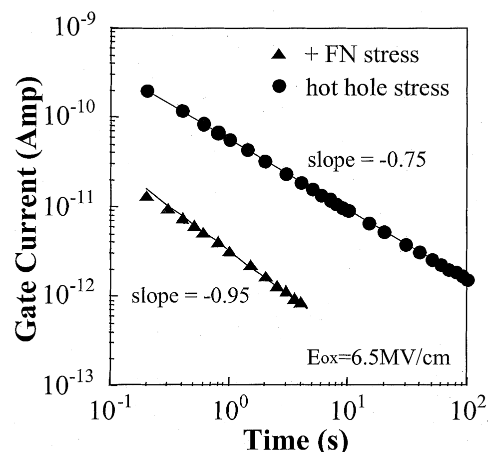

Fig. 3. HH and FN SILC transients plotted on a $\log(I)$-$\log(t)$ scale. The symbols are measurement data points and the solid lines represent a least square error fit.The measurement condition is the same as in Fig. 1.

trap generation is almost saturated. The oxide trapped charge Q_{ox} in the two stressed devices is measured from a threshold voltage method and a GIDL current method [18]. The reason of using a GIDL method for the HH stressed device is that threshold voltage in a nMOSFET is not sensitive to localized positive trapped charge, as shown in Fig. 2. After HH stress, GIDL current shifts to the left due to positive oxide charge creation and threshold voltage is nearly unchanged. In Fig. 1, the HH SILC apparently exhibits a more pronounced transient effect. The transient magnitude is about two orders of magnitude larger than the +FN SILC. The shaded area denoted by $Q_g(\mathrm{FN})$ and $Q_g(\mathrm{HH})$ is an integral of the SILC transient in a measurement interval from 0.1 s to 300 s. The integral represents total charge flowing to the gate carried by the transient component of SILC. The measured Q_{ox} and Q_g in the two devices are compared in Table I. Q_g and Q_{ox} are normalized to stressed gate areas. The HH stress region in the channel is assumed to be 0.2 μm [19]. It is interesting to note that Q_g is less than Q_{ox} in the +FN stressed device while Q_g is about ten times larger than Q_{ox} in the HH stressed device. If the transient component is contributed completely by charge trapping/detrapping, $Q_g(\mathrm{FN/HH})$ should not exceed the total trapped charge in the oxide ($Q_{\mathrm{ox}}(\mathrm{FN/HH})$). The result $Q_g(\mathrm{FN}) < \mathrm{Q_{ox}}(\mathrm{FN})$ can be understood because the FN SILC transient is caused by negative oxide charge detrapping [16]. Thus, $Q_g(\mathrm{FN})$ should not exceed the total trapped charge in the oxide. On the other side, $Q_g(\mathrm{HH}) \gg \mathrm{Q_{ox}}(\mathrm{HH})$ suggests that the HH SILC transient should contain another leakage component in addition to the displacement current resulting from oxide charge trapping/detrapping.

Moreover, we plot the FN and HH SILCs on a *log-log* scale in Fig. 3. Both the SILCs follow a straight line, i.e., power law time-dependence. However, a slight difference in the slope of the transients is noticed. The FN SILC has a slope close to -1, which is in agreement with previously published results [16]. The HH SILC in Fig. 3 was measured for three decades of time. The measured slope significantly deviates from the theoretical value of -1 obtained from the tunneling front model [16]. This significant deviation provides another evidence that the HH SILC transient cannot be explained simply by oxide charge trapping/detrapping.

III. HH SILC MECHANISM

To explain the observed differences between FN SILC and HH SILC, a positive trapped charge-assisted tunneling model is proposed for the HH SILC, as illustrated in Fig. 4. Positive trapped charges are created during HH stress. The HH SILC transient in our model actually consists of two parts, namely, I_h and I_{cat} (see Fig. 4). I_h represents positive oxide charge detrapping current and I_{cat} denotes positive oxide charge-assisted

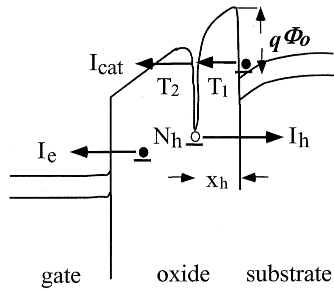

Fig. 4. Illustration of two major SILC transient components, namely, I_h and $I_{\rm cat}$, at a positive measurement gate bias in an HH stressed n-MOSFET. The open circle represents holes. $T1$ and $T2$ are electron tunneling probability.

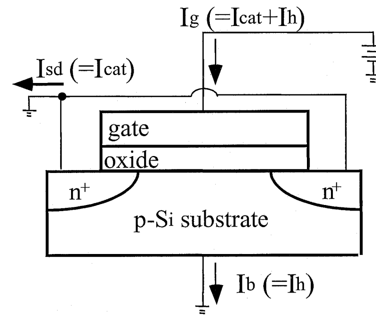

Fig. 5. Illustration of a charge separation technique. I_h represents positive oxide detrapping current, flowing to the substrate. $I_{\rm cat}$ flows to the source and the drain..

electron tunneling current. Note that I_h is a displacement current and $I_{\rm cat}$ is a conduction current. For $Q_g(\rm HH) \gg Q_{ox}(\rm HH)$, the HH SILC is dictated by $I_{\rm cat}$. The transient behavior of $I_{\rm cat}$ arises from that the positive oxide charges helping electrons to tunnel through the oxide are themselves tunneling out to the Si substrate in measurement. An analytical model relating the time-dependence of $I_{\rm cat}$ to positive oxide charge tunnel detrapping was derived in our previous publication [20]. The time-dependence of $I_{\rm cat}$ is expressed as

$$I_{\rm cat}(t) \propto q \frac{N_h}{\tau_{0e}\alpha_h}\left(\frac{\tau_{0h}}{t}\right)^n \Gamma(n) \tag{1}$$

$$n = \left(\frac{m_e(q\Phi_0)}{m_h E_t}\right)^{1/2} \tag{2}$$

where $\alpha_h = 4\pi(2m_h E_t)^{1/2}/h$, N_h represents an average oxide charge volumetric concentration; Γ in (1) denotes the Gamma function; τ_{0e} and τ_{0h} are electron and hole tunneling characteristic times, respectively [21]; $q\Phi_0$ and E_t are effective tunneling barrier heights for electrons and holes, respectively; and other variables have their usual definitions. Similarly, the expression for I_h is given as

$$I_h(t) = qA\frac{N_h}{\alpha_h}t^{-1} \tag{3}$$

where A is the area of the HH stress region. Detailed numerical analysis for the time- and field-dependence of $I_{\rm cat}$ and I_h including positive trapped charge enhanced tunneling will be discussed later.

Since I_h is a hole current and $I_{\rm cat}$ is an electron current, a charge separation technique shown in Fig. 5 can be used to monitor I_h at the substrate and $I_{\rm cat}$ at the source and the drain, respectively. Fig. 6 shows the charge separation measurement result for I_b and I_g before and after HH stress. The pre-stress I_b is negligible until $V_{\rm gs}$ is above 8 V, where anode HH injection is appreciable [22]. After HH stress, remarkable I_b and $I_g(SILC)$ are both observed in the low-field regime. The stress-induced I_b arises from the discharging of hole traps near the substrate. In Fig. 7, we plot the stress-induced I_b versus HH SILC at different stress times and bias conditions. A linear correlation between them is obtained. This correlation provides strong evidence that positive oxide charge plays an important role in HH SILC.

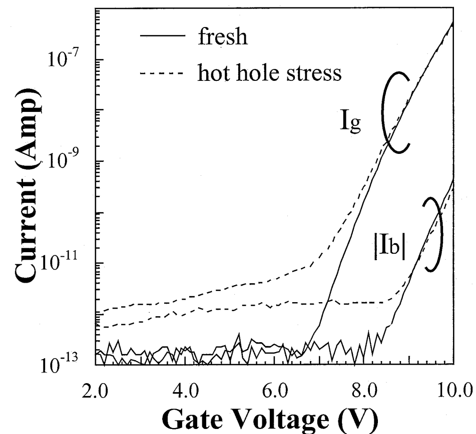

Fig. 6. Gate current and substrate current versus measurement gate bias before and after HH stress.

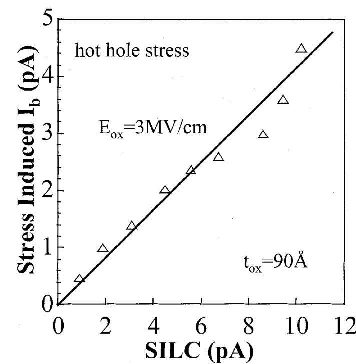

Fig. 7. Stress-induced substrate current versus SILC measured at different stress times and conditions. The oxide field in measurement is 3 MV/cm.

IV. Numerical Simulation of HH SILC

In our calculation, a Coulombic potential well caused by a positive trapped charge is included in the electron tunneling barrier (see Fig. 4). This Coulombic potential acts as a sequential tunneling center and can increase leakage current at localized spots. Although the actual problem is a three-dimensional one, the purpose here is to understand the first-order behavior. Thus, a one-dimensional treatment of the trapped charge effect is adopted as an approximation. The total potential energy Φ as a function of distance x is then given by

$$\Phi(x) = \Phi_0 - E_0 - E_{\rm ox}x - \Phi_{\rm image} - \Phi_{\rm coul} \tag{4}$$

and

$$\Phi_{\rm image}(x) = \frac{q}{16\pi\varepsilon}\left(\frac{1}{x}+\frac{1}{t_{\rm ox}+x}+\frac{1}{t_{\rm ox}-x}\right) \quad (5)$$

$$\Phi_{\rm coul}(x) = \frac{q}{4\pi\varepsilon\,|x-x_h|} \quad (6)$$

where

- Φ_0 Si/SiO_2 interfacial barrier height;
- E_0 first quantization level in the inversion layer [23];
- $\Phi_{\rm image}$ potential lowering due to tunnel electron image force;
- x_h distance of the trapped positive charge from the Si/SiO_2 interface;
- $\Phi_{\rm coul}$ modification of the tunnel barrier by a positive trapped charge.

In Fig. 4, the electron tunneling probability from the conduction band of the Si substrate to the site of the positive trapped charge at x_h is denoted by T_1. The subsequent electron transition probability from x_h to the SiO_2 conduction band is T_2. By using the WKB approximation, T_1 and T_2 can be evaluated as follows:

$$T_1 = \exp\left(-4\pi\int_{x=0}^{x=x_h}\left(\frac{2m_e\Phi(x)}{h^2}\right)^{1/2}dx\right) \quad (7)$$

and

$$T_2 = \exp\left(-4\pi\int_{x=x_h}^{x=t_{\rm ox}}\left(\frac{2m_e\Phi(x)}{h^2}\right)^{1/2}dx\right). \quad (8)$$

Since T_2 is larger than T_1 in our measurement interval, we neglect T_2 for simplification. Thus, the current flow through the modified potential barrier can be expressed as [23]

$$J(x_h) = kE_{\rm ox}^2 T_1(x_h) \quad (9)$$

where $k = 1.44 \times 10^{-6}$ Amp/V^2 in $\langle 100\rangle$ orientation [23]. Since the trapped positive charge is tunneling out through a trapezoid barrier, the tunneling time of the trapped hole to the valence band of the Si substrate is formulated according to the WKB approximation [21]

$$\tau(x_h) = \tau_{0h}\exp\left(\frac{8\pi(2m_h)^{1/2}}{3qh}\frac{E_t^{3/2}-(E_t-qE_{\rm ox}x_h)^{3/2}}{E_{\rm ox}}\right) \quad (10)$$

where E_t is the hole trap energy. The transient behavior of $I_{\rm cat}$ and positive oxide charge detrapping current are then formulated as follows:

$$I_{\rm cat}(t) = AN_h\sigma\int_0^{t_{\rm ox}} J(x_h)\exp\left(\frac{-t}{\tau(x_h)}\right)dx_h \quad (11)$$

$$I_h(t) = qAN_h\int_0^{t_{ox}}\frac{\exp\left(\frac{-t}{\tau(x_h)}\right)}{\tau(x_h)}dx_h \quad (12)$$

where

- τ positive oxide charge tunneling time;
- σ cross section of the PCAT center;

TABLE II
THE PARAMETERS USED IN SIMULATION. E_o IS THE FIRST QUANTIZATION ENERGY IN THE CHANNEL. $\tau_{\rm oh}$ IS HOLE TUNNELING CHARACTERISTIC TIME. Φ_o IS THE SI/SiO_2 INTERFACE BARRIER HEIGHT. E_t IS THE HOLE TRAP ENERGY. σ IS THE CROSS SECTION OF THE PCAT CENTER. m_e AND m_h ARE ELECTRON AND HOLE TUNNELING MASS, RESPECTIVELY, AND N_h IS THE POSITIVE TRAPPED CHARGE DENSITY

$E_0 = 0.2eV$	$k = 1.44x10^{-6}\,Amp/V^2$
$\tau_{0h} = 0.01ps$	$\sigma = 10^{-15}\,cm^2$
$\Phi_0 = 3.2eV$	$m_e = m_h = 0.5m_0$
$E_t = 3.5eV$	$N_h = 5.0x10^{18}\,cm^{-3}$

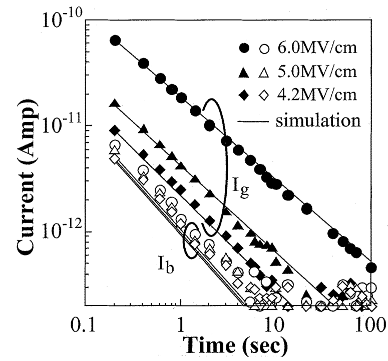

Fig. 8. Simulated and measured I_g and I_b transients in an nMOSFET by band-to-band HH stress. $t_{\rm ox} = 90$ Å. The oxide field is 6.0 MV/cm, 5.0 MV/cm, and 4.2 MV/cm. The symbols represent measurement data points and the solid lines are from simulation. The $1/t$ dependence of I_b implies uniform $+Q_{\rm ox}$ distribution in a tunnel detrapping distance.

- N_h volumetric positive oxide charge concentration;
- A area of the HH stress region.

The parameters used in our simulation are given in Table II. The hole trap volume density (N_h) is extracted from the experimental data.

Comparing (11) and (12), the $I_{\rm cat}$ is expected to have a larger field dependence than I_h. The reason is that the electron effective tunneling barrier is smaller and thus the electron tunneling probability $T_1(x_h)$ exhibits a stronger field dependence than hole tunneling probability $\tau_{0h}/\tau(x_h)$. In addition, the supply function term ${E_{\rm ox}}^2$ of (9) that is contributed by the surface quantization effect [23] is also a factor.

V. RESULTS AND DISCUSSION

A. Time- and Field-Dependence

The measured and calculated time-dependence of I_g and I_b at different oxide fields is shown in Fig. 8. The symbols represent measurement data and the solid lines are from simulation. A close look reveals that the HH SILC and I_b exhibit a slightly different slope, i.e., $I_b \propto t^{-1}$ and $I_g \propto t^{-n}$ with $n < 1$. As shown in (2), the factor n is related to electron and hole tunneling masses and barriers. The t^{-n} dependence of I_g was also noticed by other groups ($n = 0.7$) [15]. The field-dependence of the HH SILC and I_b is plotted in Fig. 9. The SILC and stress-induced I_b are measured at $t = 0.2$ s. Two distinguished features are noted.

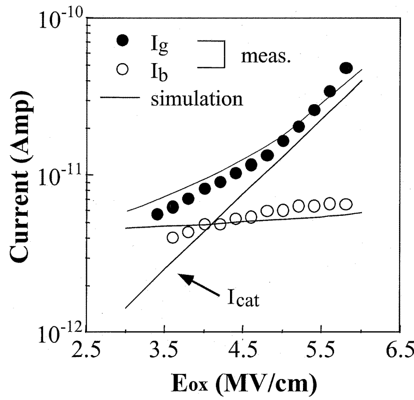

Fig. 9. Field-dependence of electron tunneling current ($I_{\rm cat}$), substrate current (I_b), and gate current ($I_g = I_{\rm cat} + I_h$). The symbols represent measurement data at $t = 0.2$ s and the lines are from simulation.

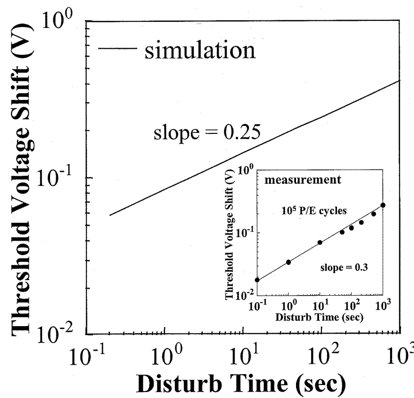

Fig. 10. Simulated threshold voltage shift versus read-disturb time from the SILC in Fig. 8. $E_{\rm ox} = 5$ MV/cm. The measured threshold voltage shift versus read-disturb time in a stacked gate Flash EEPROM after 10^5 P/E cycles is shown in the inset. The applied control gate voltage in read-disturb is $V_{\rm cg} = 6$ V.

First, the measured hole detrapping current (I_b) is nearly independent of an oxide field, which is consistent with the calculated result. As a contrast, the HH SILC exhibits small field dependence in the low-field range ($<$ 3.5 MV/cm) and strong field dependence in the medium field range (3.5 MV $\sim$ 6 MV/cm). The reason is that the major component of the HH SILC is the hole detrapping current (I_h) at low fields and is the electron tunneling current ($I_{\rm cat}$) at higher fields. Our model shows that the larger field dependence of $I_{\rm cat}$ results from a smaller effective tunneling barrier for electrons and the supply function term ${E_{\rm ox}}^2$. The $I_{\rm cat}$ component will become more significant in multi-level cells (MLC) with regard to read-disturb since a larger read gate bias is usually required in MLC.

In Fig. 10, the read-disturb characteristics due to the transient effect of HH SILC are simulated. According to the tunneling front model, threshold voltage shift ΔV_t caused by oxide charge trapping/detrapping should vary linearly with the logarithm of time [24]. Instead, our simulation shows the read-disturb caused ΔV_t has power law time-dependence at an oxide field of 5 MV/cm. The obtained power factor is approximately 0.25, which can be derived from the integration of $I_{\rm cat}$. The measurement result in a stacked gate Flash EEPROM device ($t_{\rm ox} = 90$ Å) after 10^5 P/E cycles are plotted in the inset of Fig. 10 as a reference. The Flash device is programmed by hot electron injection at $V_{\rm ds} = 5$ V and $V_{\rm gs} = 10$ V at the drain side and erased by edge FN injection at $V_{\rm ds} = 6$ V and $V_{\rm gs} = -9$ V at the source side. A linear relationship of ΔV_t versus t in a *log-log* scale is obtained with a slope of 0.3. It is not our intention to compare ΔV_t between measurement and calculation. The calculated ΔV_t is based on the measured SILC in a conventional gate nMOSFET, which has a quite different stress condition from the P/E stress in a Flash cell. Thus, the calculated and measured ΔV_t in Fig. 10 have a large difference in magnitude although they have similar time-dependence. The power law-dependence of ΔV_t on read-disturb time was also found by other groups [17] with a power factor of 0.28 for $t_{\rm ox} = 85$ Å at $V_{\rm cg} = 6$ V.

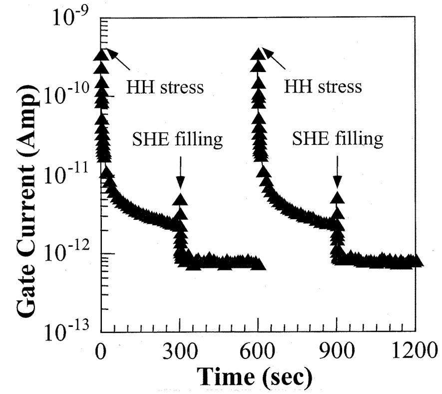

Fig. 11. SHE injection effect on HH SILC. $t_{\rm ox} = 100$ Å.

B. Reduction of HH SILC

HH SILC can be greatly reduced by annealing the positive oxide charges. Here, substrate hot electron (SHE) injection at $V_{\rm gs} = 2.5$ V and $V_{\rm sub} = -7$ V is utilized to neutralize positive trapped charges created by HH stress. Since the substrate injection current is relatively large (2×10^{-4} A/cm^2), positive oxide charge neutralization is achieved via either recombination or compensation by the injected electrons. The electron filling efficiency is strongly dependent on an oxide field and is less dependent on electron injection energy [25]. The filling (recombination) efficiency is better at a lower oxide field. For this reason, a smaller gate bias was chosen in the SHE filling. The effect of positive charge neutralization on HH SILC is shown in Fig. 11. The HH SILC is greatly reduced by the filling. Its steady-state level is below 1 pA after the filling. After subsequent HH stress, the HH SILC transient reappears. The HH stress and SHE filling cycle is repeated in Fig. 11. No noticeable difference is observed between the two cycles, implying that the SHE filling itself does not introduce additional stress effect. Fig. 12 shows the corresponding change in I_b. A reduction of I_b by an order of magnitude is observed after the filling. From this study, it can be concluded that I_b can be used as an effective monitor for PCAT in SILC.

C. Oxide Thickness Dependence

In the above discussion, the role of PCAT in SILC has been substantiated for $t_{\rm ox} = 100$ Å. On the other side, it is also well

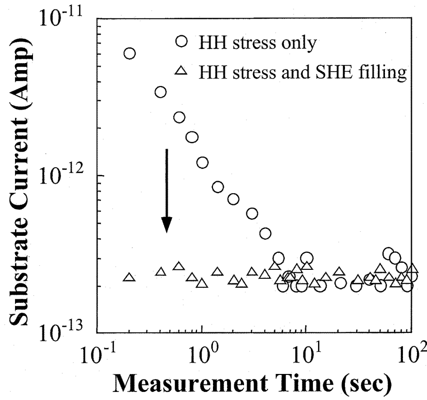

Fig. 12. Transient characteristics of positive oxide charge detrapping current ($|I_b|$) with and without SHE filling.

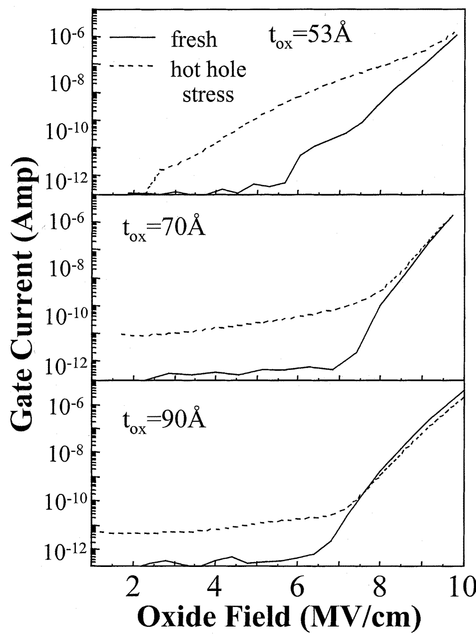

Fig. 13. Gate current versus gate bias in nMOSFETs before and after band-to-band HH stress. $t_{\rm ox} = 53$ Å, 70 Å, and 90 Å.

published that neutral TAT is the dominant SILC mechanism in ultrathin oxides. It is interesting to investigate the transition between these two mechanisms. Stress-induced I_g and I_b in large gate area nMOSFETs with $t_{\rm ox} = 90$ Å, 70 Å, and 53 Å are measured. Negative channel FN stress was performed at $E_{\rm ox} = -10$ MV/cm. Fig. 13 shows pre-stress and post-stress I_g and Fig. 14 shows the corresponding change in I_b. The pre-stress I_b in Fig. 14 is negligible until anode hot hole (AHH) injection for $t_{\rm ox} = 70$ Å and 90 Å and valence electron tunneling for $t_{\rm ox} = 53$ Å occur [22]. After stress, a remarkable I_b appears even at a small gate bias in thicker oxides while this stress-induced I_b vanishes at low fields in the 53 Å oxide. The reduction of I_b in the thinner oxides can be explained as follows. Since a constant voltage stress is applied, the stress gate voltage is smaller for thinner oxides. Thus, the injected electrons have less energy and the creation of trapped holes is reduced [26]. Further characterization shows that the SILC in the 53 Å oxide does not contain a transient component. According to the published results in literature [8], [11], [27], the responsible mechanism

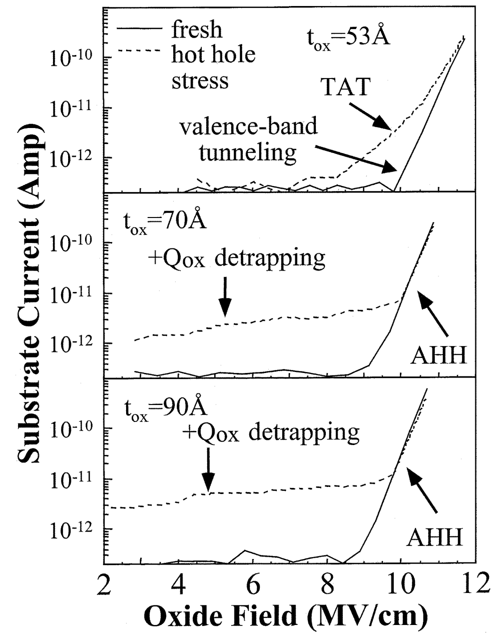

Fig. 14. Substrate current versus gate bias in nMOSFETs before and after band-to-band HH stress. $t_{\rm ox} = 53$ Å, 70 Å, and 90 Å. The stress-induced I_b vanishes at low fields in the 53 Å oxide device. TAT represents TAT and AHH represents AHH injection.

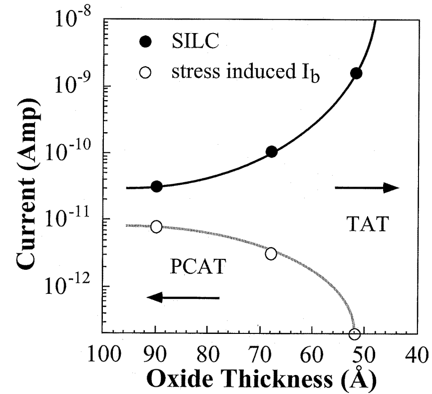

Fig. 15. Oxide thickness dependence of SILC and stress-induced I_b measured at $E_{\rm ox} = 5$ MV/cm. The dominant SILC mechanism changes from PCAT in thick oxides to TAT in thinner oxides.

of the SILC in thinner oxides should be TAT. The TAT current strongly depends on the oxide thickness and increases as the oxide thickness is reduced [27]. In Fig. 15, the oxide thickness dependence of SILC and I_b is shown. The measurement field is at 5 MV/cm. As $t_{\rm ox}$ reduces to 53 Å, the correlation between stress-induced I_b and SILC does not exist. In other words, the dominant SILC mechanism changes from PCAT at $t_{\rm ox} = 100$ Å to TAT at $t_{\rm ox} = 53$ Å.

VI. Conclusion

Positive trapped charges created during edge FN erase play an important role in SILC and related read-disturb in Flash EEPROM cells. A power law dependence of ΔV_t on read-disturb time, resulting from the transient effect of PCAT, is derived from measurement and simulation. Stress-induced low-field I_b can be used as an effective monitor for PCAT effect in

SILC. By using an appropriate hot electron injection technique, the PCAT current can be greatly reduced. In ultrathin oxides (53 Å), the correlation between SILC and I_b no longer exists. We conclude that the dominant SILC mechanism changes from PCAT in thicker oxides (100 Å) to TAT in ultrathin oxides.

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