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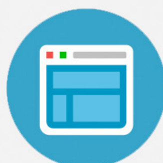

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Investigations of pulse current electrodeposition for damascene copper metals

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The influence of current density, duty cycle, and frequency of the applied pulse current on film qualities of electroplated copper was discussed. With various filled damascene structures, the corresponding filling power was optimized in a range of pulse current frequency. The optimized pulse current plating in conjunction with a leveler-free electrolyte resulted in a defect-free filling in approximate 100 nm damascenes and reduced the resistivity of Cu deposits. © *2002 American Vacuum Society.* [DOI: 10.1116/1.1518974]

I. INTRODUCTION

To enhance filling capability and to reduce surface roughness of electroplated copper in multilevel interconnects, plating electrolytes usually contain proprietary additive chemistries such as brighteners and levelers.[1–5] For the damascene process, the superfilling phenomenon occurs when the adsorption and consumption rates of additives on the cathode are predominantly diffusion controlled.[1] For maintaining transport control of the inhibitor flux, the adsorbate must either consume into the growing film or undergo reductive desorption during metal deposition.[1–4] Therefore, most levelers will react with the metallic Cu resulting in a relatively brittle and high resistivity deposit by facilitating impurity incorporation.[6] Thus it is desirable to reduce the use of additives, then minimize impurity levels in electrodeposited thin films.

In previous studies, the use of pulse current (PC) or pulse reverse current (PRC) deposition has demonstrated many merits such as a more uniform deposit thickness,[7,8] an enhancement of the ''hole throwing power'' in the printed circuit board (PCB) industry,[9] void-free deposits with minimal Cu overplate in copper damascene applications,[10] and a wide tolerance to seed layer morphology.[11] In theoretical investigation, West and co-workers[12] simulated the PRC copper electrodeposition in high-aspect ratio damascenes by a one-dimensional model. However, the application of PC and PRC electrodeposition on submicron Cu electroplating in multilevel interconnects is not fully studied. The pulse current conditions to obtain plated films with desirable performances and to achieve a defect-free filling in various pattern layouts are very critical.

In this work, the influence of current density, duty cycle, and frequency of the applied external pulse current on film qualities of electroplated copper was discussed. Moreover, the maximum filling power for various damascene structures was characterized with PC frequency dependence. By optimizing the pulse current conditions, this pulse current plating in conjunction with a leveler-free electrolyte resulted in a defect-free filling in approximate 100 nm damascenes. Concurrently, the resistivity of the deposited film was reduced due to no additives consisting of sulfur (S) and nitrogen (N) elements in the electrolyte.

II. EXPERIMENT

A blanket wafer was prepared by depositing a 50 nm sputtered TaN diffusion barrier and a 50 nm sputtered Cu seed layer on a SiO_2/Si substrate. A patterned wafer consisted of a 30 nm thick ionized metal plasma (IMP)-TaN layer as a diffusion barrier and a 200-nm-thick IMP-Cu film as a seed layer. The experiments on Cu electroplating were carried out in a tank of nonconducting material. The counterelectrode was a platinum plate with a size of $6\times6\ cm^2$ and the working electrode was a wafer with a size of $1\times3\ cm^2$. The distance from counterelectrode to working electrode was 10 cm. Contact to the electrode was implemented outside of the electrolyte with an alligator clip. In Cu electroplating processes, the standard electrolyte was composed of $CuSO_4\cdot5H_2O$ (purity$>$99%, chloride$<$10 mg/kg), 30 g/l H_2SO_4 (97%, chloride$<$0.1 mg/kg), 275 g/l chloride ions, 50–100 ppm, and deionized water ($\sim$18 MΩ). Moreover, the addition of polyethylene glycols with different molecular weights (PEG2000: 50 ppm and PEG200: 2000 ppm) to the standard electrolyte formed a leveler-free electrolyte. All chemicals used in this work were purchased from Fluka. The films were deposited under galvanostatic control at room temperature. The dc power supply utilized in this work was Keithley model 2400 and the pulse form (square wave) was controlled using a function generator (Instek model GFG-813). The cross-section profiles, the surface morphologies, and the mean grain size of copper films were examined using a field

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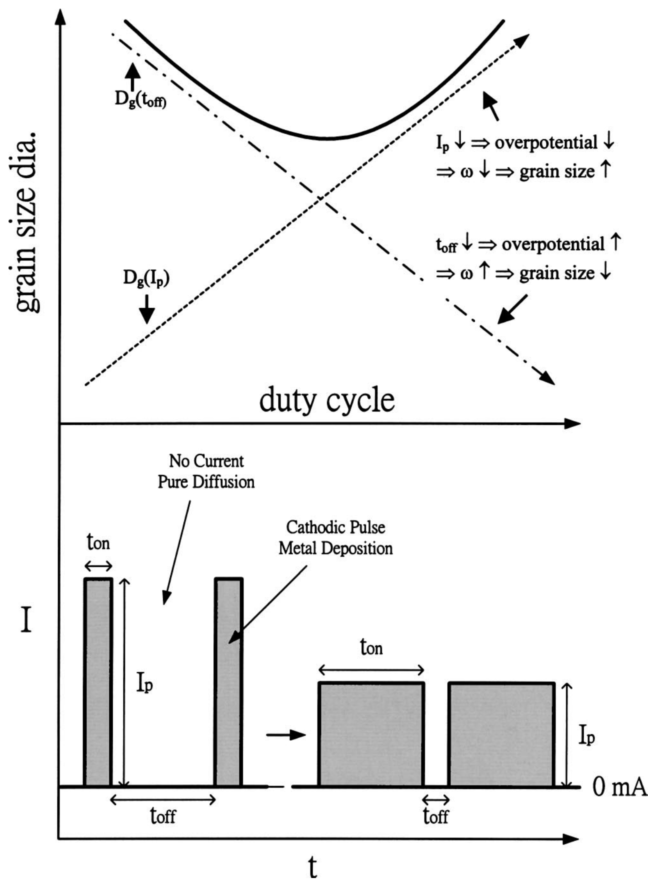


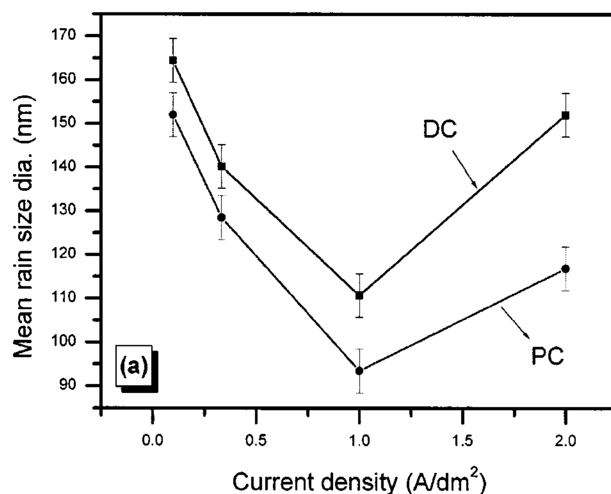
FIG. 1. Proposed model illustrates influences of peak current and duty cycle on qualities of deposits, where D_g is the evolution of grain size with duty cycle, ω is the nucleation rate, I_p is the cathodic peak current, t_{on} is the cathodic on-time, and t_{off} is the off-time between the pulses.

emission scanning electron microscope (FESEM). The specimens were annealed by rapid thermal annealing (RTA) for 30 s in N_2 atmosphere and the sheet resistances of copper deposits were measured by a four-point probe.

III. RESULTS AND DISCUSSION

In general, the pulse current (PC) plating was used to improve the filling capability and achieve smoother Cu deposits. Figure 1 displays the PC wave form in relation to the cathodic peak current I_p; the cathodic on-time t_{on}; and the off-time between the pulses t_{off}. Duty cycle, T, is defined as $T = t_{on}/(t_{on}+t_{off})$. The product of the duty cycle and the cathodic peak current gives the PC average current, $I_{avg} = I_p \times T$. This parameter I_{avg} in direct current (dc) or PC plating determines the deposition rate. As the applied current density increases in both dc and PC plating, Figure 2(a) shows that the grain size became smaller due to an increase of the nucleation rate, resulting in deposits with reduced porosity and finer grains.[5] The deposition time was 5 s for both dc and PC plating in the standard electrolyte, and the frequency and the duty cycle were held at 100 Hz and 50%, respectively, in the PC plating. Too low current density cannot provide significant overpotential to obtain denser deposits; however, when too much current is supplied, cupric ions are reduced too fast and Cu aggregation occurs around the protrusion on the surface under higher electric field, thus leading to deposits with rough and porous structures.[5] Figure 2(b) also shows that the resistivity of those films were consistent with the trend of Fig. 2(a). A longer deposition time of 10 min was performed herein.

The influence of duty cycle on the grain size and resistivity of films deposited by the PC plating is shown in Fig. 3. The frequency and the average applied current density were held at 100 Hz and 0.1 A/dm^2, respectively, in the standard electrolyte. Deposited films electroplated at a duty cycle of 50% exhibited smaller grain size, lower resistivity, and smoother surface than those for other duty cycles. For the PC plating, as the duty cycle increases, the plating characteristic approaches that of dc plating. In comparison, the decrease of duty cycle (T) means an increase of off-time (t_{off}) and in terms of an increase of peak pulse current (I_p) when the



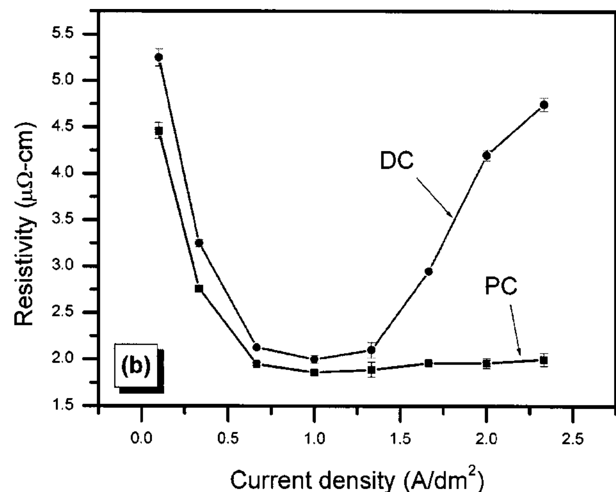


FIG. 2. (a) Effects of applied current density on the grain size of Cu deposits in both dc and PC plating. (b) Effects of applied current density on the resistivity of Cu deposits in both dc and PC plating.

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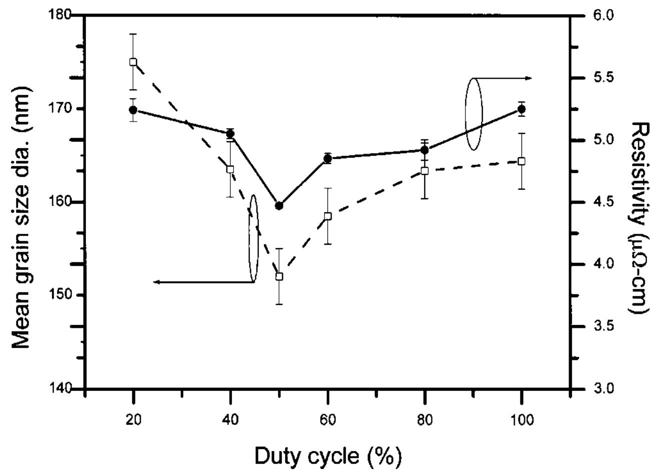

FIG. 3. Grain size and resistivity of deposits as a function of the duty cycle of the PC wave form.

average current density is maintained constant, as shown in Fig. 1. In general, a higher I_p results in finer grains and smoother deposits due to the nucleation rate (ω) increasing exponentially with overpotential.[13] However, a longer t_{off} increases the supply of cupric ions from bulk solution, depressing the effect from higher cathodic overpotential. The proposed mechanism of Fig. 1 illustrates that the evolution of grain size (D_g) increased as off-time increased, but D_g decreased as an increase in peak power. We suggest that these two factors (t_{off} and I_p) determined an optimal duty cycle about qualities of plated films as observed in Fig. 3. This phenomenon was also suggested to explain better performances from PC plating (duty cycle of 50%) than those from dc plating, as shown in Fig. 2(b).

Next we examined the effect of frequency on film quality. The inset of Fig. 4 shows transient cell voltage $V(t)$ of PC plating in the standard electrolyte. For this experiment, the duty cycle and the average applied current density were held at 50% and 0.1 A/dm^2, respectively. For the applied PC wave form with higher frequency, charge and discharge times are too short for the double layer to respond, making the corresponding $V(t)$ (curve 4) behave like that for dc current. This high frequency effect also raised the transient cell voltage (or an effective overpotential), thus resulting in a decrease in the mean grain size of deposits, as shown in scanning electron microscopy (SEM) images of Fig. 4 (the grain size saturated at ~125 nm at 1 kHz). Those films were plated for 5 s. In the previous study, Kristof and Pritzker also showed the microhardness of Cu deposits increased with pulse frequency.[8]

To maximize the electrical conductivity of Cu lines as well as to obtain other desired material properties, voids in deposits should be avoided. This can be achieved if the deposition rate at the bottom is higher than that along the trench sidewall (i.e., the "superfilling" mechanism). The use of a leveler would appear to be ideal for the production of void-free deposits. This, however, conflicts with the industrial desire to reduce additive use. Thus, in this study, the PC plating in conjunction with the leveler-free electrolyte was used to obtain the superfilling and to reduce the resistivity of Cu deposits. After rapid thermal annealing (RTA) at 300 °C for 30 s in N_2 atmosphere, the resistivity of films (average thickness was about 300 nm) deposited by the electrolyte with PEG-Cl (2.09 $\mu\Omega$ cm) were lower than that of the film deposited by the electrolyte containing PEG-Cl-2-mercaptopyridine (2.47 $\mu\Omega$ cm)[4] or PEG-Cl-2-aminobenzothiazole (2.15 $\mu\Omega$ cm).[5]

Figure 5 displays the filling power of PC electroplating in various feature sizes as a function of frequency in the leveler-free electrolyte. The filling power was calculated from the filling ratio $\Delta y/\Delta x$ of "bottom-up" to "side-wall shift" from the cross section of a partially filled copper profile on a SEM image, as shown in the inset of Fig. 5.[4] At the

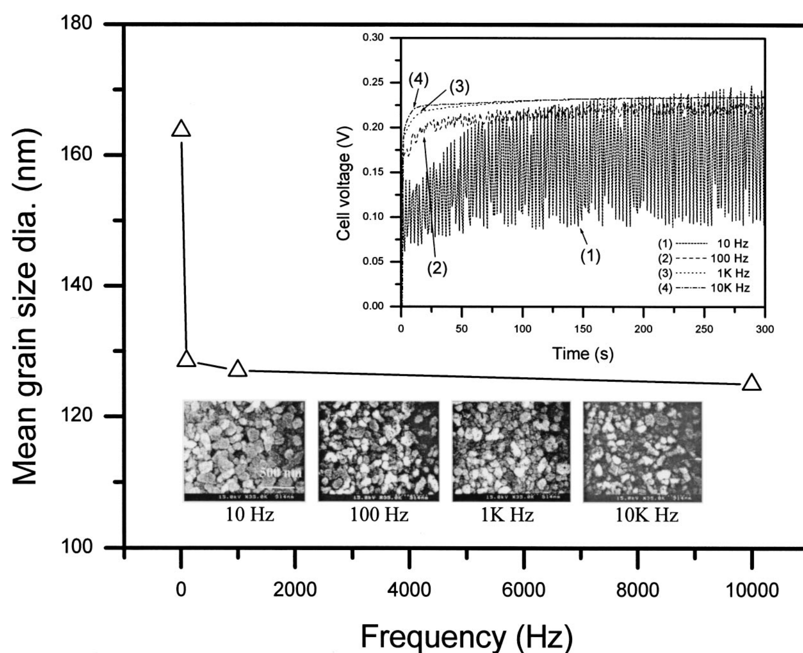

FIG. 4. Effects of PC frequency on the grain size of deposits and the *in situ* voltage-time curves of PC plating systems with different PC frequencies in the standard electrolyte. SEM top-view images of the deposits electroplated by PC plating at 10, 100, 1000 and 10 000 Hz are also shown.

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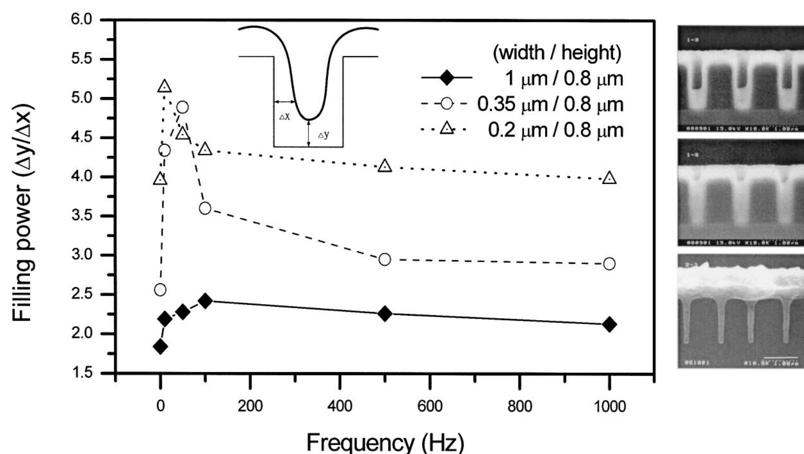

FIG. 5. Effects of PC frequency on leveling power for filled features with various sizes. Inset diagram shows the method to measure the filling power. Upper and central SEM images reveal the bottom-up filling transient in 0.35 μm trenches; the bottom SEM image shows the defect-free filling in approximate 100 nm vias.

same average current density (0.33 A/dm^2) and duty cycle (50%), the maximum filling power was observed at an optimum frequency in the PC plating. In the previous study by West and co-workers,[12] they showed that the off-time should be on the order of the diffusion-time constant ($\tau_d = h_0^2/D$) and that the deposition time should be smaller than the diffusion time constant, where h_0 was the deepness of trenches and D was the diffusivity of cupric ions. In this study, the maximum filling power occurs at about $t_{\mathrm{off}}/t_{\mathrm{on}} \sim 1$. Therefore, the optimized t_{off}, and t_{on} are assumed as the value of τ_d, and then the theoretical value of optimized frequency was about 250 Hz after calculating $\tau_d \sim 2$ ms from $h_0 \sim 0.8$ μm and $D \sim 0.5 \times 10^{-5}$ cm^2 s^{-1}.[12] From the curve (1 μm/0.8 μm) in Fig. 5, the optimized frequency was ~100 Hz and was in the same order as the theoretical value. On the other hand, the peak of the filling power increases and shifts to lower PC frequencies as the aspect ratio of the feature increases. According to the study by Stoychev and co-workers,[9] they rationalized the presence of a frequency optimum as a result of the competition between increasing nuclei formation with decreasing brightener surface concentration as PC frequency increases. Therefore we suggest that when the aspect ratio of features increases, more additive surface concentration must exist to facilitate filling by means of a shift of operated PC frequency to lower frequency. The increase of the filling power with increasing the aspect ratio of the feature may be due to a more apparently additive concentration gradient in higher aspect ratio features. In addition, the longer off-time (lower frequency) was necessary for higher aspect ratio features to alleviate the concentration gradient of cupric ions in the gap. The upper and central SEM images of Fig. 5 reveal the bottom-up filling transient in 0.35 μm trenches. Finally, the defect-free filling of approximate 100 nm damascenes was obtained by the modified PC plating in the leveler-free electrolyte, as shown in the bottom SEM image of Fig. 5.

IV. CONCLUSION

Through optimizing the peak current density, duty cycle, and frequency of the PC wave form, the pulse current plating significantly reduced the additive use and resulted in the defect-free filling in approximate 100 nm vias. A simple model and numerous experiments explored the mechanisms of the duty cycle affecting the grain size and resistivity. On the other hand, in the pulse current plating, the maximum filling power was found to occur at an optimum frequency in relation to the feature size.

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