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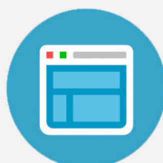

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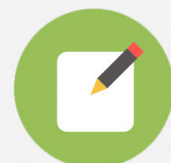

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Single-electron transistor structures based on silicon-on-insulator silicon nanowire fabrication by scanning probe lithography and wet etching*

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We propose a promising fabrication technology for single-electron transistors based on a silicon-on-insulator (SOI) nanowire fabricated by scanning probe lithography and KOH wet etching. The 10-nm-wide and 10-nm-high silicon nanowire is defined by scanning probe lithography and KOH wet etching process technology. Along the [100] direction on a (100) SOI silicon wafer, local oxidation was performed in ambient using highly doped Si cantilevers with a resistivity of 0.01–0.0025 Ω cm and a commercial atomic force microscope/scanning tunneling microscope instrument. Using the oxide pattern as a Si etching mask, the Si substrate was dipped in aqueous KOH solution, in which unoxidized regions are selectively etched by aqueous KOH orientation-dependent etching. The silicon nanowire was obtained by well-controlled overetching of 34 wt % at 40 °C for 50 s. The top gate, back gates and contact pads were defined by photolithography and dry etching. Statistics showing the reproducibility of this technique are also demonstrated. © *2002 American Vacuum Society.* [DOI: 10.1116/1.1523017]

I. INTRODUCTION

Based on enhanced of industrial instruments and new fabrication technology, electron devices designed with quantum effect and several-electron operation can easily be made on the nanometer scale. Single-electron transistors (SETs) that can operate at lower power and high frequency are of great interest currently. The basic single-electron transistor structures are nanowire devices. Several methods have been developed for fabricating silicon nanowires. Electron-beam lithography (EBL) was used to form the nanowire patterns on the electron-beam resist (PMMA), followed by dry reactive-ion etching (RIE) to fabricate 20 nm polysilicon nanowires.[1] The metal particles (Au and Zn) used as catalysts to nucleate whisker growth and the 20–200 nm single-crystal nanowire[2] were deposited by chemical vapor deposition (CVD) in a silicon-containing vapor environment, which is called vapor–liquid–solid (VLS) growth. Similar to VLS growth, laser ablation also can fabricate ~20 nm silicon nanowires.[3] Cui *et al.*[4] employed doped-silicon nanowires to create real-time highly sensitive electrical sensors for chemical and biological applications. It is interesting that the conductance of the silicon nanowires increases nonlinearly when increasing or decreasing the pH values of the solution. Also interesting is that for a biotin-modified silicon nanowire dipped into a treptavidin solution, the conductance of the nanowire changed in real time. The silicon nanowire device includes control gates, nanowires, and source/drain contacts, in which the fabrication of nanowires is the primary process of this device.

Scanning probe lithography (SPL) has become a promising lithography process and it can form oxide nanopatterns (>50 nm) on a sample surface by applying bias between the tip and sample.[5,6] These oxide patterns, ~50 Å thick, can be used as etching masks of the underlying material. Of these methods, EBL is a well-established high-resolution patterning technique that possesses the capability of precise pattern definition, but the high cost is the main disadvantage of this method. VLS growth can provide numerous nanowires, but the method of locating nanowires accurately in a device has been a crucial topic for several researchers.[7] SPL can easily print sub-50 nm features, which is compatible with EBL; but SPL can be used on a wider range of materials.

In this study, SPL is introduced to define the mask pattern of nanowires and the etching process employs KOH solution. For single-crystalline silicon etching, the etching rates of different orientation planes depend on the exposure bond num-

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bers of the orientation plane. The etching-rate ratio of (110):(100):(111) is 1:0.463:0.007 of KOH 40 wt % at 70°C.[8] According to different etching rates of different planes, the morphology of the silicon nanowire is controllably fabricated into a desired shape, which is called orientation-dependent etching (ODE).

We demonstrate a silicon single-electron device based on a silicon nanowire, where the silicon nanowire is 10 nm in both pattern height and linewidth at the bottom of a (100) silicon-on-insulator (SOI) wafer. By combining SPL patterns with well-controlled overetching of KOH ODE, the two processes provide a simple method by which to produce silicon nanowires in a nanoelectronics study.

II. EXPERIMENT AND DISCUSSION

Two methods are included in this key process of fabricating silicon nanowires: (1) SPL can provide a highly repeatable oxide linewidth ranging from 50 to 200 nm and (2) KOH wet etching further shrinks the linewidth to sub-20 nm on a (100)-oriented SOI wafer. For SPL, an excess voltage is applied between a sharp tip and a conductive sample, and an electric field is induced between the tip and sample. The electric field can be expressed as an asymptotic form of a point charge above an infinite conductor plane, and the relationship between the electric field and voltage applied can be expressed as[9]

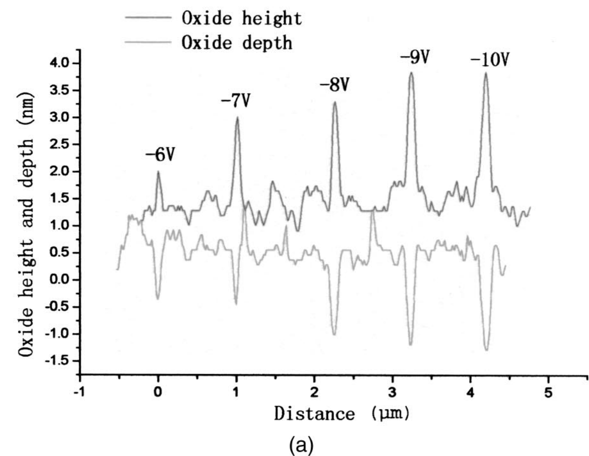
$$E=\frac{a(a+b)(a+2b)}{b[(a+b)^2+\rho^2]^{3/2}}V, \qquad (1)$$

where a is the tip radius, b is the distance between the tip and sample, V is the tip voltage, and ρ is the radial distance between the tip and the sample (with the tip above the origin of the sample plane). Equation (1) shows that the electric field is linearly proportional and increases with an increase in applied voltage. When an induced electric field exists between the tip and sample, negative ions from air, such as O^{-2}, O^{-}, or OH^{-}, will be forced into the silicon and result in volume expansion. This is called "field-induced localized oxidation." Figure 1(a) shows cross-sectional profiles of field-induced localized oxide with an increase in sample voltage. Oxide growth was carried out at 25 °C in ambient humidity 40%, 1 μm/s scanning speed, and tip/sample contact force equal to the distance of the tip/sample maintained at 10 nN. In this experiment, the ~50 nm oxide linewidth was obtained at a tip/sample voltage of −8 V.

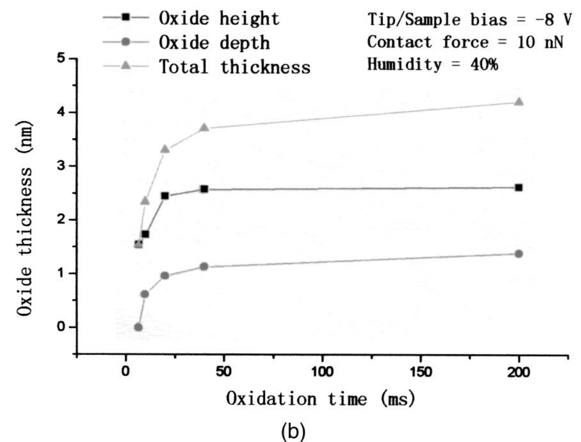
When an applied voltage of 10 V was reached, as shown in Fig. 1, the oxide thickness trended toward saturation. Cabrera and Mott[10] and Ghez,[11] who built the conductor and semiconductor oxidation models, showed the linear relationship of maximum thickness/growth thickness and growth time as

$$\frac{X_1}{X}=-\ln\left(\frac{t}{X^2}\right)-\ln(X_1u), \qquad (2)$$

where t is the growth time (equal to the tip–radius/scanning speed), and u is the velocity of the drift. In Fig. 1(b), the oxide thickness strongly depends on the growth time: the growth time of local oxidation trended toward saturation when the growth time was slower than 20 ms, and this experiment was carried out at 25 °C in ambient humidity of 40%, 10 nN of contact force, and −8 V of tip/sample voltage. This field-induced oxide, generated over different growth times, did not follow the linear relationship between X_1/X and $\ln(t/X^2)$ like the results of the Cabrera–Mott model and Chez models. This discrepancy was because variation of the electric field was neglected during the process of oxide generation. In fact, this electric field changed with an increase in oxide thickness, where as the Cabrera–Mott model postulated that the electric field is fixed during the oxidation process.



(a)



(b)

FIG. 1. (a) Cross-sectional AFM image of the mask oxide profile obtained using the scanning probe microscope with different sample/tip voltages applied. The oxide height is directly measured after local oxidation, and the oxide depth is measured after the sample is dipped in HF solution to remove the mask oxide patterns. (b) Relationship of oxide height, oxide depth, and total thickness of the mask oxide with respect to 50 ms oxidation time.

Figure 2(a) shows a scanning electron microscopy (SEM) image of a silicon nanowire on a (100)-oriented, 60 nm SOI wafer. The nanowire pattern of the mask oxide is defined along the (100) direction and induced by 7 V sample voltage, 35% humidity, 10 nN contact force, and 0.5 μm/s scanning speed. This nanowire was etched in a 34 wt % KOH solution at 50 °C for 30 s. It is found that the shape of the nanowire

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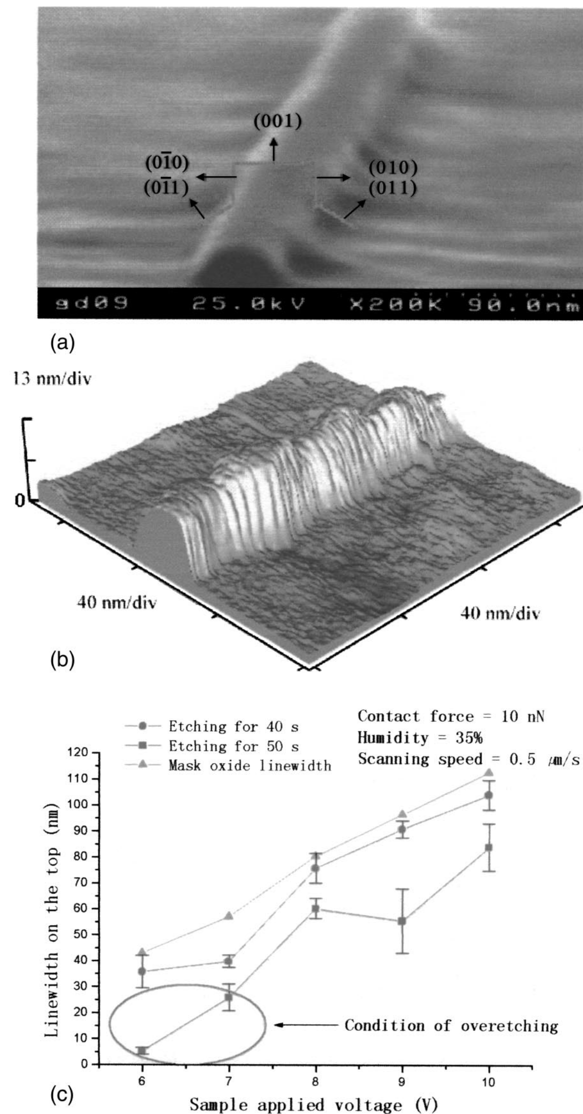

FIG. 2. (a) SEM image of silicon nanowires on a (100) SOI wafer. The height is about 50 nm, and the linewidth at the top is about 30 nm. (b) Statistics of the linewidth with/without overetching. The error bars present the variation in linewidth in each of the experimental groups. (c) AFM image of Si nanowires of 7 V sample voltage and 50 s overetching.

on a (100) SOI wafer [Fig. 2(a)] can be decomposed into two parts: the vertical sidewall and the slope bottom. The orientation of two sidewalls of the nanowire on a (100) SOI wafer is (100) oriented, and the orientation at the bottom plane of this nanowire is (110)-oriented planes. The (110)-oriented plane forms a 45° angle with respect to the vertical (100)-oriented plane and the horizontal (100)-oriented plane. Based on the prior description, the etching-rate ratio of (100)/(110) is 0.5848 at 40 °C, and the calculated height ratio of the vertical part of the (100) plane and the slope part of the (110) plane is ~2. After overetching for 10 s, the heights of the 6 and 7 V nanowires were ~20 nm and the linewidth measured on the top of the nanowire had shrunk ~5 and ~20 nm, respectively, as shown in Fig. 2(c). Figure 2(b) shows an atomic force microscopy (AFM) image of a (100) SOI nanowire of 7 V and etching for 50 s (overetching condition), in which the height and width of the nanowire are ~20 nm. As shown in Fig. 2(c), the linewidth of the mask oxide is the main factor that determined the etched linewidth of the silicon nanowires. If the linewidth of mask oxide is too wide, the final linewidth, even after overetching, will not shrink too much. This is observed for sample voltages of 8, 9, and 10 V in Fig. 2(c). These results are because the etching rate of (100)-oriented planes on silicon is very close to the etching rate of (110)-oriented planes, and the condition of overetching is like isotropic etching when the mask oxide is consumed on the top of the nanowire. Under such conditions, the structure of the nanowire desired can be obtained by controlling the overetching.

III. DEVICE PREPARATION

Currently used fabricating techniques of silicon nanoscale device structures also encompass patterns generated directly by electron-beam and focus-ion-beam lithography, dimensions of devices shrunk by self-limited oxidation, structures deposited by chemical vaporization or physical evaporation, and other means. This study, which provides a low cost highly repeatable technique, uses a combination of optical lithography, scanning probe lithography, and wet anisotropic etching.

Figure 3 shows a process flow chart of a silicon SET using optical SPL. The starting material was a *p*-type, (100)-oriented SOI wafer with a buried isolation oxide layer formed by implanted oxygen [separation by implanted oxygen (SIMOX)]. The SOI layer is 500 Å thick, and the buried isolation oxide layer is 2000 Å thick. First, the SOI wafer was cleaned by the standard RCA clean process. The silicon had been thinned by 900 °C dry oxidation for 11 min, and a 400 Å oxide layer formed that reduced the silicon thickness from 500 to ~300 Å. Then the first mask was introduced to define active areas on the oxide layer. The backside gate pattern was defined by mask 2, and the buried oxide was removed directly by a buffer oxide etching (BOE) solution: the contact pad via then formed. Second, the SPL process was introduced to generate the oxide nanowire as the etching mask, and the 34 wt % KOH wet etching process produced the silicon nanowires. By using photoresist (PR) to protect nanowires, the source/drain metal contacts consisting of a 3000-Å-thick aluminum layer were etched by inductively coupled plasma (ICP). Finally, the passivated oxide was deposited, and the top gate was formed with the same prior process of formation of metal contacts. SPL was introduced to fabricate silicon-oxide (SiO_x) nanowires for the etching mask by localized oxidation on the silicon wafer surface, and these nanowires showed excellent performance, not only with regard to oxide quality for the etching process but also for features of fine linewidth. Local oxidation was performed in ambient using highly doped Si cantilevers with a resistivity of 0.01–0.0025 Ω cm and a commercial AFM/scanning tunneling microscope (STM) (M5 type, Park Scientific Instruments). Using these oxide nanowires as a Si etching mask, the Si substrate was dipped into aqueous KOH solu-

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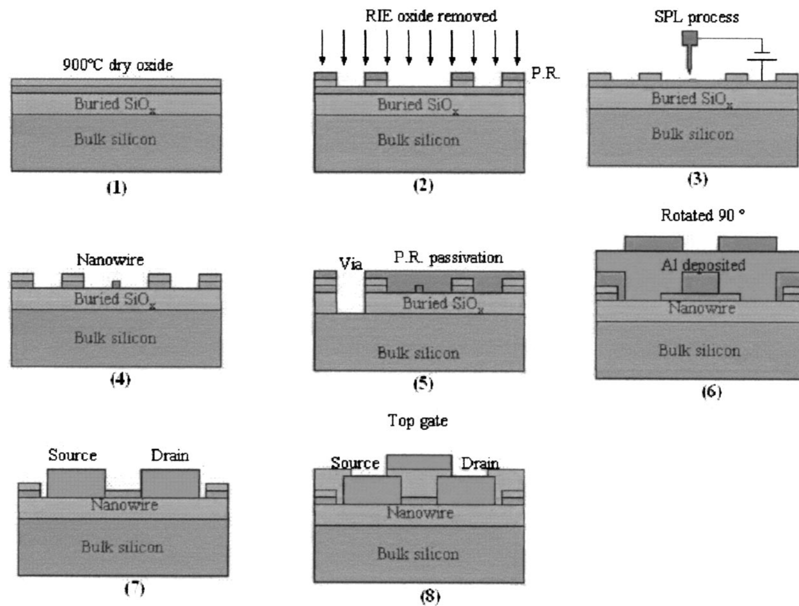

FIG. 3. Schematic of processing steps for the single-electron transistor. (1) A *p*-type Si (100) 60 nm SOI substrate is oxidized at 900 °C for 11 min. (2) Active areas are patterned and etched by a RIE dry-etching system. (3) SPL is introduced into pattern the mask oxide of silicon nanowires. (4) The patterned samples are etched in KOH solution with ODE. (5) Contact windows of the substrate are patterned by optical lithography and etched by BOE. (6) Before contact-metal thermal deposition, photoresist is used to protect the unexposed area of the silicon nanowire. (7) Contact pads are finished by a lift-off process. (8) The gate oxide layer is deposited by plasma-enhanced chemical vapor deposition. After the top gate metal layer is deposited, contact patterns are defined and etched, and the single-electron transistor is complete.

tion, in which the unoxidized regions were selectively etched by aqueous KOH ODE. In applying KOH ODE, however, various orientations of the silicon wafer such as (100)-oriented silicon wafers result in various morphologies of the silicon nanowire. Finally, by combining with the prior process, the SET structure is fabricated, as shown in Fig. 4(a), and includes the top gate, source/drain contact, and connection line, and silicon nanowire. Figure 4(b) shows the contact pads of the source/drain and nanowire. The 10-nm-high and 10-nm-wide silicon nanowire, fabricated by 40 °C and overetching, on a (100) SOI wafer is demonstrated in Fig. 4(c).

IV. CONCLUSIONS

We demonstrated the fabrication of a single-crystal silicon nanowire using scanning probe lithography and KOH wet etching techniques. Single-electron transistors were produced with a mix and match of optical lithography and scanning probe lithography. Using a SPL mask oxide layer of silicon nanowire has the advantage over electron-beam lithography of low cost and higher exposure latitude. The linewidth of the mask oxide can be controlled well to 30–40 nm by applying 6 V sample/tip bias, 1 μ m/s scanning speed, 10 nN contact force (with respect to the tip/sample distance),

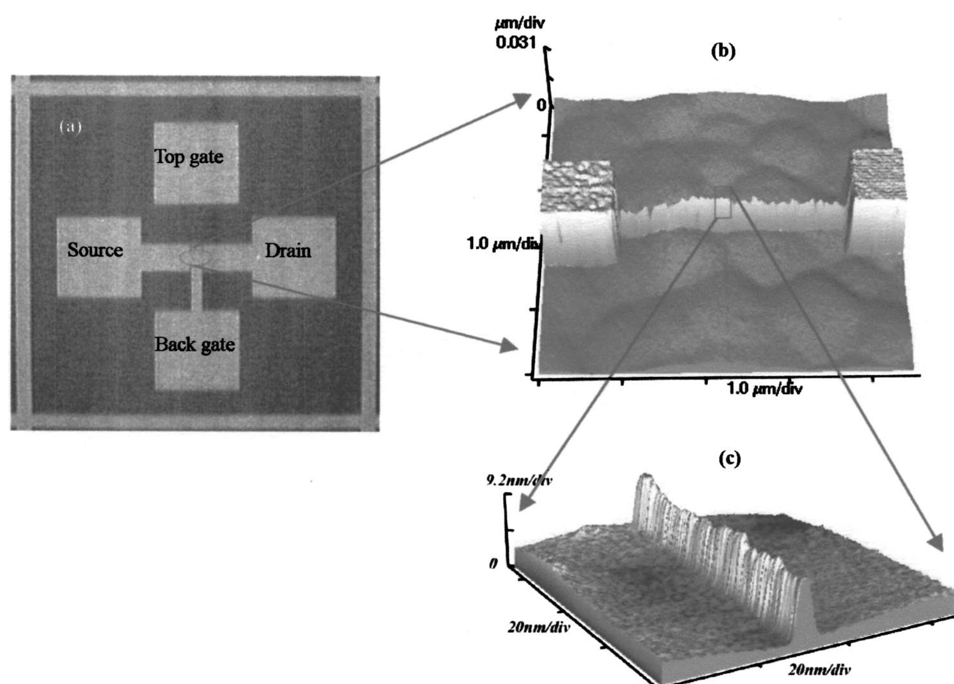

FIG. 4. (a) Top view of a single-electron transistor on a SOI wafer. (b) AFM image of the silicon nanowire and source/drain contact pads fabricated with SPL and KOH wet etching. (c) Detailed AFM image of the silicon nanowire demonstrating the 10 nm $\times$10 nm nanostructure.

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and 40% environmental humidity. The KOH wet etching system provides a method by which to further shrink the linewidth of the silicon nanowire, sub-20 nm of the (100) SOI wafer, from the mask oxide pattern with orientation-dependent etching. We have demonstrated that SPL and KOH wet etching systems can accurately generate oxide patterns and can subsequently fabricate single-electron transistors, which are widely used in biosensor devices, optical devices, and nanoelectronics devices.

ACKNOWLEDGMENT

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