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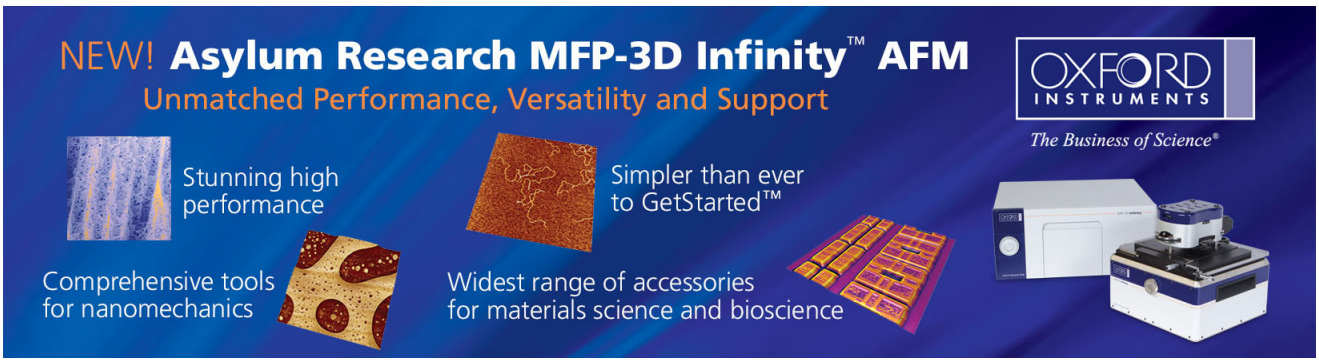

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On–off switching of edge direct tunneling currents in metal-oxide-semiconductor field-effect transistors

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On–off switching behaviors or two-level random telegraph signals (RTS) are measured in the low voltage ($-1.40\ \mathrm{V} < V_G < -0.88\ \mathrm{V}$) edge direct tunneling currents in ultrathin gate stack (10 Å oxide+10 Å nitride) *n*-channel metal-oxide-semiconductor field-effect transistors. The plausible origin is the process-induced defects in terms of localized gate stack thinning (or equivalently the conductive filament). In such extrinsic case, the current trapping–detrapping theories can adequately elucidate the data, particularly the RTS magnitude as large as 18%. The current–voltage characteristic associated with a certain defective spot is assessed straightforwardly, showing remarkable compatibility with existing oxide thinning case. Systematic measurements of RTS in the terminal currents allow for determining the occurrence probability as well as locations of defects, and may be treated as a sensitive process monitor. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1518563]

For ultrathin gate stack metal-oxide-semiconductor field-effect transistors (MOSFETs), the edge direct tunneling (EDT) of electrons or holes from polysilicon to underlying silicon diffusion region has very recently been investigated.[1–3] According to quantum mechanical simulation,[2,3] the EDT spans from the gate edge a range of about 6 nm wide, which exactly falls within the gate-to-diffusion overlap region. Thus, exploration of the noise or fluctuations via EDT currents is highly probable in the presence of such a nanoscale dimension. In this letter we exhibit a two-level random telegraph signals (RTS) phenomenon measured from the EDT currents at low voltages, followed by interpretations and discussion.

The *n*-channel MOSFETs with the gate width and length of 10 and 0.5 μm, respectively were manufactured in a standard process technology. During the gate stack formation, a 10 Å thick SiO_2 layer was thermally grown and underwent rapid plasma nitridation (RPN) treatment, then on which a 10 Å thick nitride film was grown, followed by NO annealing at 950 °C. The devices were characterized by means of a semiconductor parameter analyzer HP4156 with source, drain, and bulk tied to ground. The measured steady-state terminal currents versus negative gate voltage characteristics, as depicted in Fig. 1 for a certain sample, were found to be nearly the same for all samples. From Fig. 1 we drew a certain EDT region of interest throughout the work: $-1.40\ \mathrm{V} < V_G < -0.88\ \mathrm{V}$. In such a low voltage range, the EDT current I_S flowing from source to gate and the other EDT current I_D from drain to gate both dominantly constitute the gate current I_G. Figure 1 further points out that the source and drain currents are comparable each other in the sense of steady-state characterization. To strengthen RTS measurement precision, the integration time in HP4156 for data sampling was changed from a default value of 1 ms down to equipment limit of 8 μs. The measured fluctuations in drain, gate, and source currents for the sample in Fig. 1 are displayed in Fig. 2, looking like those from a two-terminal tunnel gate stack with a percolation path.[4–7] The abrupt transitions between two distinct states occur in gate and source currents whereas being absent in the drain current, suggesting that (i) significant defects exist in the gate-to-source overlap part rather than gate-to-drain overlap; and (ii) they should be localized such as to match above steady-state characterization. Figure 2 also reveals identical RTS parameters between source and gate currents: the same time duration τ_{on} and τ_{off} in the high and low current state I_{on} and I_{off}, respectively, and the same state current change ΔI $(=I_{on}-I_{off})$. This consistency confirms the existence of a two-terminal EDT path.

Figure 3 shows experimental I_{on} and I_{off} of the source current against gate voltage. We also found that (i) the sta-

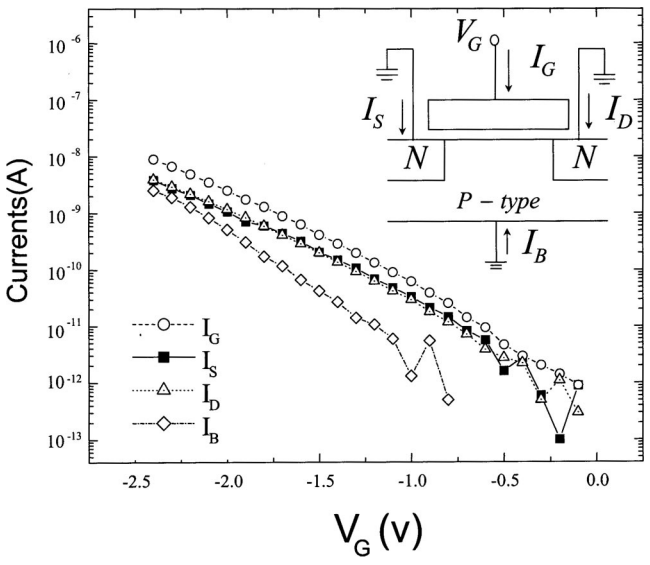

FIG. 1. Measured steady-state terminal currents vs negative gate voltage. The inset shows the connection configuration.

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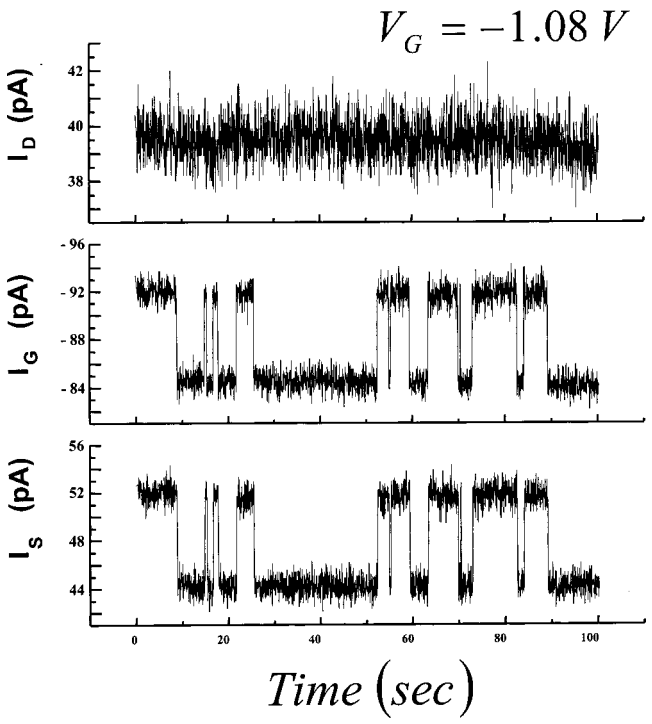

FIG. 2. Time records of drain, gate, and source currents at $V_G = -1.08$ V for the sample in Fig. 1.

tistical distributions of τ_{on}'s and τ_{off}'s indeed obey an exponential behavior with the mean $\overline{\tau}_{on}$ and $\overline{\tau}_{off}$, respectively; and (ii) $\overline{\tau}_{on}$ and $\overline{\tau}_{off}$ each exponentially decrease with increasing magnitude of gate voltage. Finally, repeated RTS measurements yielded the same RTS parameters, indicating that no stress induced defects are encountered, as expected due to low voltage operation.

The above on–off switching phenomenon can be likely ascribed to the manufacturing process induced defects[8,9] as schematically shown in Fig. 4 in terms of localized gate stack thinning, or equivalently the conductive filament[9] defined by the thinning thickness Δt_{ox} and the occupied area ΔA (shaded region; shown only partly). Such a defective

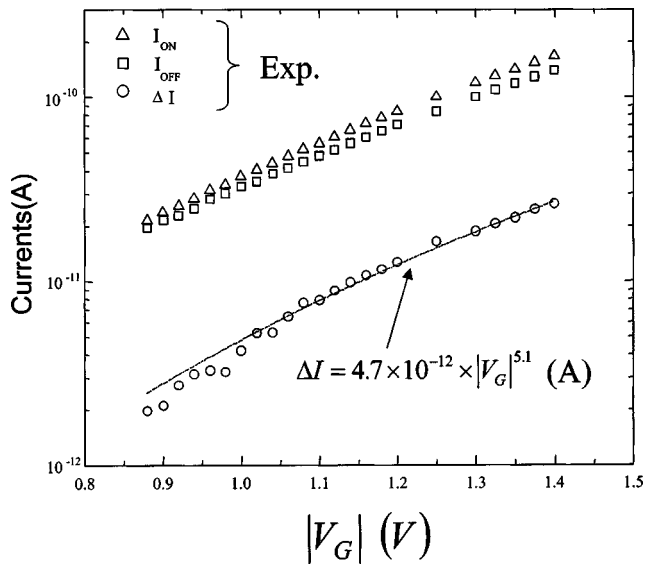

FIG. 3. Experimental high and low state currents vs magnitude of gate voltage for the sample in Fig. 1; also shown is a line for comparison.

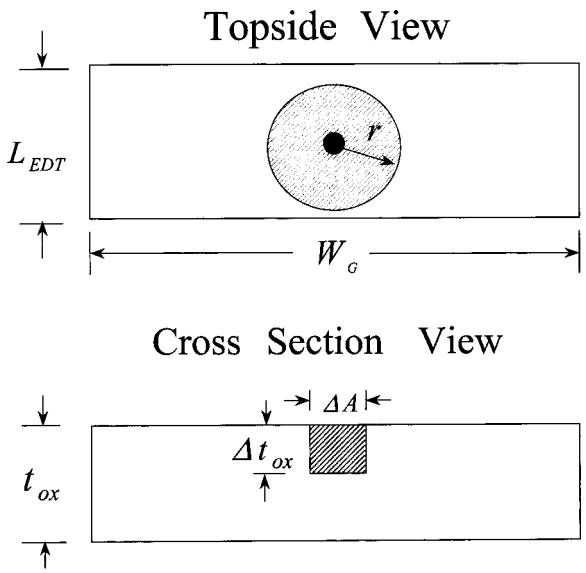

FIG. 4. Topside and cross section views of a gate stack overlap part devoted to the edge direct tunneling operation, defined by the gate width W_G, the effective tunneling size L_{EDT}($\sim$6 nm), and the thickness t_{ox}. On the topside a shaded circle with the trapped electron as the origin is drawn with a radius r. On the cross section part a localized gate stack thinning or conductive filament is drawn in terms of the thinning thickness Δt_{ox} and the occupied area ΔA.

spot can be thought to be a conductive filament connected in series with the remainder (with the net thickness of $t_{ox} - \Delta t_{ox}$) of the gate stack. The conductive filament is also a trap-rich region in nature as characterized by the trapping–detrapping probabilities[7] in terms of both the emission time τ_{off} and the capture time τ_{on} as mentioned above. According to current trapping–detrapping theories,[7] once a single electron is captured in the trap-rich region, the caused Coulomb repulsive force repels subsequently tunneling electrons, thus effectively turning off the influenced area around the trapped electron. This specific area can be represented by a capture cross-section area[10] denoted πr^2 in Fig. 4. Consequently, the EDT current in the filled trap mode can be written as (analogous to Simoen *et al.*'s work[10])

$$I_{off} \approx J_n \times (A_{EDT} - \pi r^2), \tag{1}$$

where J_n is the tunneling current density associated with the gate stack thickness t_{ox} and A_{EDT} is the EDT area. The region πr^2 can be recovered to the on state in the empty trap mode. The corresponding high current state I_{on} can thereby be expressed as

$$I_{on} \approx J_n \times (A_{EDT} - \Delta A) + \Delta J_n \times \Delta A, \tag{2}$$

where ΔJ_n is the tunneling current density for a net thickness of $t_{ox} - \Delta t_{ox}$, indicating that $\Delta J_n \gg J_n$ for considerable Δt_{ox}. The mentioned ''localization'' implies that ΔA can be of comparable order with πr^2.[9] As a result, Eq. (2) minus Eq. (1) produces quantitatively $\Delta I \approx \Delta J_n \times \Delta A$ for the two-terminal characteristic of a defective spot. In Fig. 3 the fractional change $\Delta I / I_{off}$ turns out to be between 12% and 18%. Also plotted in Fig. 3 is a line from an empirical formula of direct tunneling for oxide thinning $\Delta I = a|V_G|^b$,[6] showing not only close agreements with experiment but also reasonable values of a and b compared with the citation.

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Furthermore we carried out a very extensive RTS measurement across the whole wafer. It turned out that about 36% of the samples exhibit two-level RTS only in EDT source currents; 12% only in EDT drain currents; and no noticeable RTS was observed for the rest or for both EDT source and drain currents. Therefore, systematic measurements of RTS in the terminal currents allow for determining the occurrence probability as well as locations of defects, and may be treated as a sensitive process monitor.

In conclusion, a new on–off switching behavior is measured in the gate stack overlap EDT currents. With process defects as the plausible origin, experimental data can be adequately described by current trapping–detrapping theories. Significant efforts are also made: assessing the two-terminal current–voltage characteristic associated with a defective spot; finding the occurrence probability of the defects as well as their locations in a manufacturing process; etc.

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