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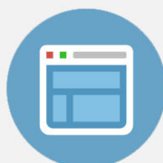

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A physical model for the hysteresis phenomenon of the ultrathin ZrO_2 film

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This work studies and presents an inner-interface trapping physical model for the ultra-thin (effective oxide thickness=15 Å) zirconium oxide (ZrO_2) film to explain its hysteresis phenomenon. The shift of the capacitance–voltage characteristics swept from accumulation to inversion and then swept back with light illumination is about 110 mV, which is larger than the shift without light illumination (~45 mV). The mobile ion effect is obviated using bias-temperature stress measurement. The proposed model successfully explains not only the phenomenon but also the thickness effect for the capacitance–voltage characteristics and the different turn-around voltages of the current density–voltage characteristics of the zirconium dielectrics. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1498964]

I. INTRODUCTION

For the very deep submicron complementary metal–oxide–semiconductor (CMOS) device, the international technology roadmap for semiconductors (ITRS) predicts that a sub-16 Å silicon dioxide gate dielectric is needed for the sub-0.1 μm CMOS device.[1] A SiO_2 gate oxide of that thickness has been shown to have a leakage current of the range of 1–10 A/cm^2.[2,3] Recently, there was much work[4–16] on studying ZrO_2 to replace SiO_2 as the gate dielectric due to its high dielectric constant (~25), wide energy bandgap (~7.8 eV),[8] high stability with the Si surface,[17] and low post deposition annealing temperature (~500 °C).[4] Its electrical properties were also reported to be good enough as the candidate for the gate dielectrics for the deep sub-micron device.

Unfortunately, for ZrO_2, there is the hysteresis phenomenon in its capacitance–voltage (C–V) characteristics.[11,13,14,18] This hysteresis will induce a flat-band voltage shift, consequently a threshold voltage instability when it is applied to the MSO field-effect transistor as the gate dielectrics. It was reported that the hysteresis phenomenon might be due to chemical contaminations, the stress-induced defect formation, or mobile ions.[19] In this article, this phenomenon is studied and an inner-interface trapping model is presented to explain it.

II. EXPERIMENT

Al/TiN/ZrO_2/Zr-silicate/p-Si capacitors with an area of 7.85×10^{-5} cm^2 were fabricated on 8-in. p-type Si wafers. First, the ZrO_2 film of 50 Å was deposited by atomic layer chemical vapor deposition, which was performed at a temperature of 300 °C and a pressure of about 1 Torr. The precursors used for the deposition were $ZrCl_4$ and H_2O. After the gate dielectric was formed, a TiN film of 250 Å was deposited by metal organic chemical vapor deposition. The sample was then annealed in the furnace for 10 min in an N_2 ambient at 400 °C. A 5000 Å Al film was deposited on the wafer by a thermal coater. After that, the gate of the capacitor was defined lithographically and etched. Finally, a 5000 Å Al film was also deposited on the back side of the wafer to form the ohmic contact. The effective oxide thickness (EOT) was estimated by the high frequency (0.1 MHz) C–V in the strong accumulation region without considering quantum mechanical effects. Moreover, the physical thickness was checked by a transmission electron microscopy (TEM) to obtain the dielectric constant. The electrical properties were

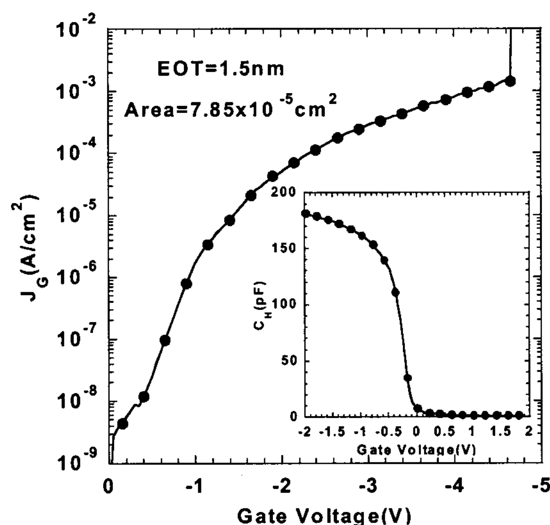

FIG. 1. Plots of negative current density vs voltage characteristics of the zirconium dielectrics, where the inset shows the high frequency capacitance vs voltage characteristics with the voltage swept from inversion to accumulation.

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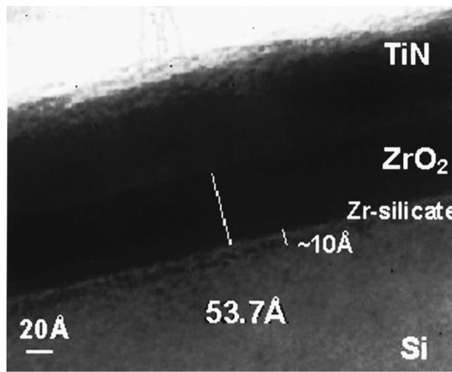
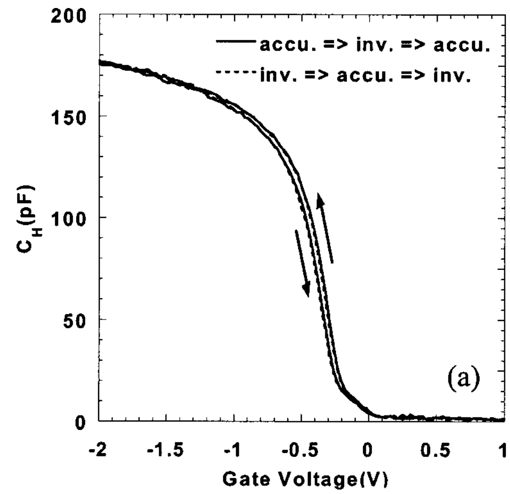


FIG. 2. TEM image of the zirconium dielectrics.

measured by using an HP 4156B semiconductor parameter analyzer and an HP4284A precision LCR meter.

III. RESULTS AND DISCUSSION

Figure 1 shows the negative current density–voltage (J–V) characteristics, where the inset shows the high frequency C–V characteristics swept from inversion to accumulation, of the fabricated ZrO_2 film, for which the EOT value derived is 15 Å. The TEM micrograph of the cross section of the film is shown in Fig. 2, where the physical thickness was measured to be 53.7 Å. In the TEM picture, it is also observed that there exists an interfacial layer of about 10 Å, referred as Zr-silicate,[20] at the ZrO_2/Si interface. It is believed that this silicate layer plays an important role in creating the hysteresis observed in the zirconium dielectrics as explained later. The effective dielectric constant derived based on the physical thickness, including the interfacial Zr-silicate layer, is larger than 20. The sample shows a leakage current density lower than 10^{-6} A/cm^2 at $V_g = -1$ V, which is comparable with the values reported before.[4–7] Figure 3 shows the measured time-to-breakdown (T_{BD}) data of the dielectrics at room temperature and 150 °C respectively, and



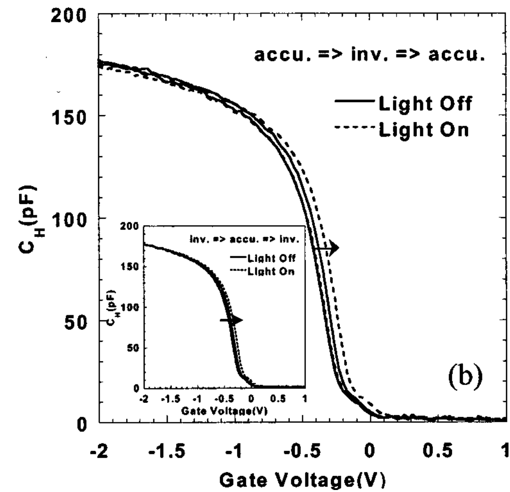


FIG. 4. (a) Hysteresis phenomenon of the zirconium dielectrics sweeping from accumulation (solid line) and from inversion (dashed line) without light illumination. (b) Hysteresis phenomenon of the zirconium dielectrics sweeping from accumulation with (dashed line) and without (solid line) light illumination. The hysteresis phenomenon sweeping from inversion is in inset.

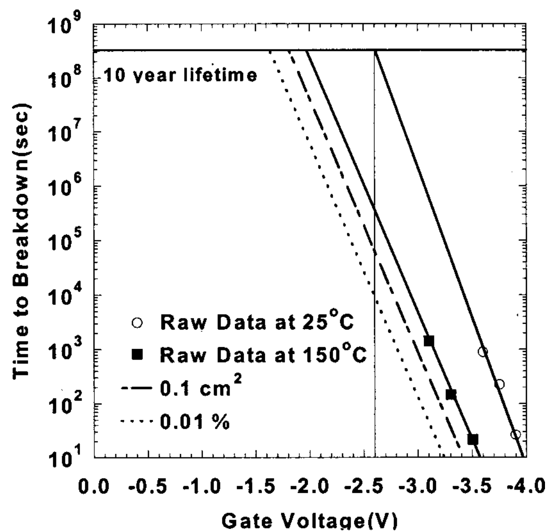


FIG. 3. The measured T_{BD} data of the sample at room temperature and the 150 °C respectively, and the derived T_{BD} data for the scaled area of 0.1 cm^2 and the 0.01% failure rate for the samples.

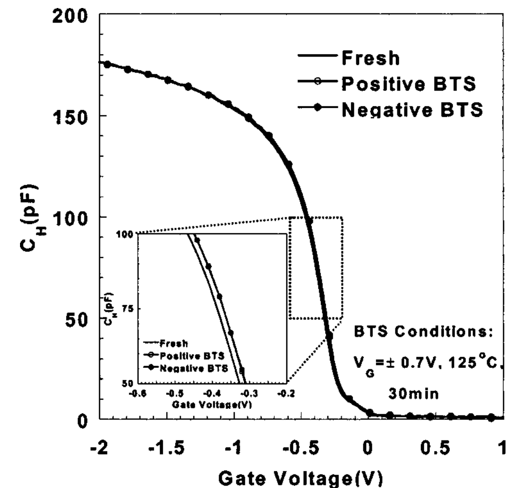


FIG. 5. High frequency capacitance vs voltage distortion under bias-temperature stress of the zirconium dielectrics, where the inset shows the enlargement between 50 to 100 pF.

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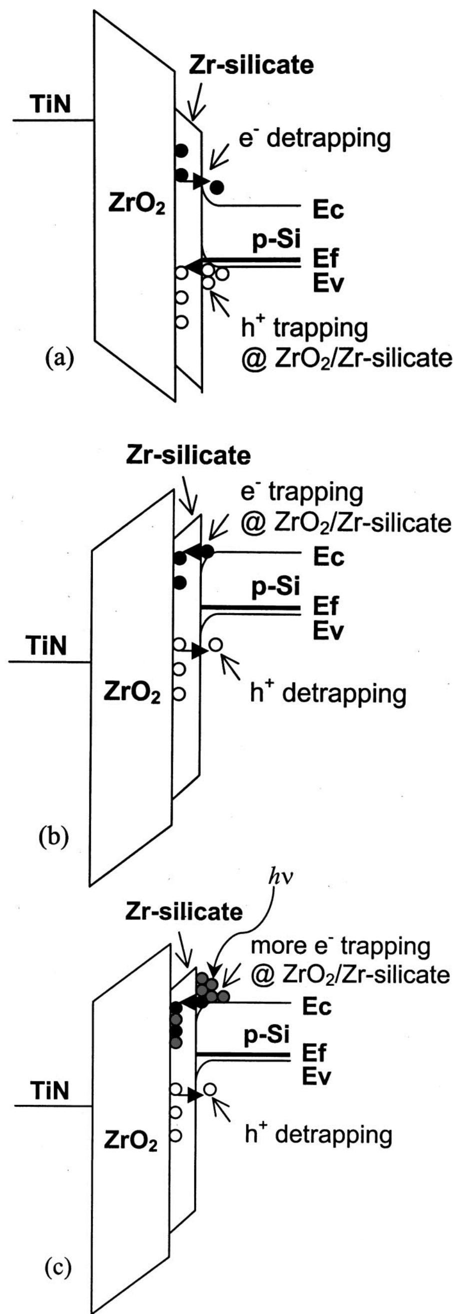

FIG. 6. (a) Inner-interface trapping model of the zirconium dielectrics sweeping from accumulation ($V_g = -2.0$ V) without light illumination. (b) Inner-interface trapping model of the zirconium dielectrics sweeping from inversion ($V_g = +1.0$ V) without light illumination. (c) Inner-interface trapping model of the zirconium dielectrics sweeping from inversion ($V_g = +1.0$ V) with light illumination.

the derived T_{BD} data for the scaled area of 0.1 cm^2 and the 0.01% failure rate for the samples.[21,22] In the above, the data for the area scaling and the 0.01% line were derived from the Weibull distribution of the 150 °C data assuming a random distribution of breakdown sites.[23] The derived maximum operating voltage could be, in these conditions, as high as 1.6 V, which is much higher than 1 V for the sub-0.1 μm device as obtained from the ITRS roadmap.

Figure 4(a) shows the hysteresis in the C–V characteristics of the sample without light illumination. The solid line is

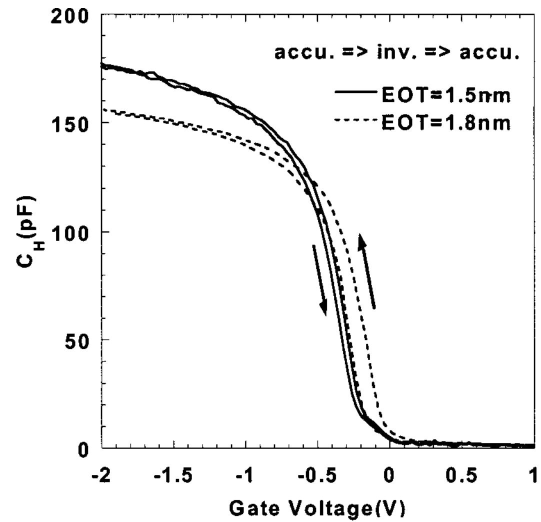

FIG. 7. Hsyteresis phenomenon of the zirconium dielectrics sweeping from accumulation for the thinner zirconium oxide (solid line) and thicker one (dashed line) without light illumination.

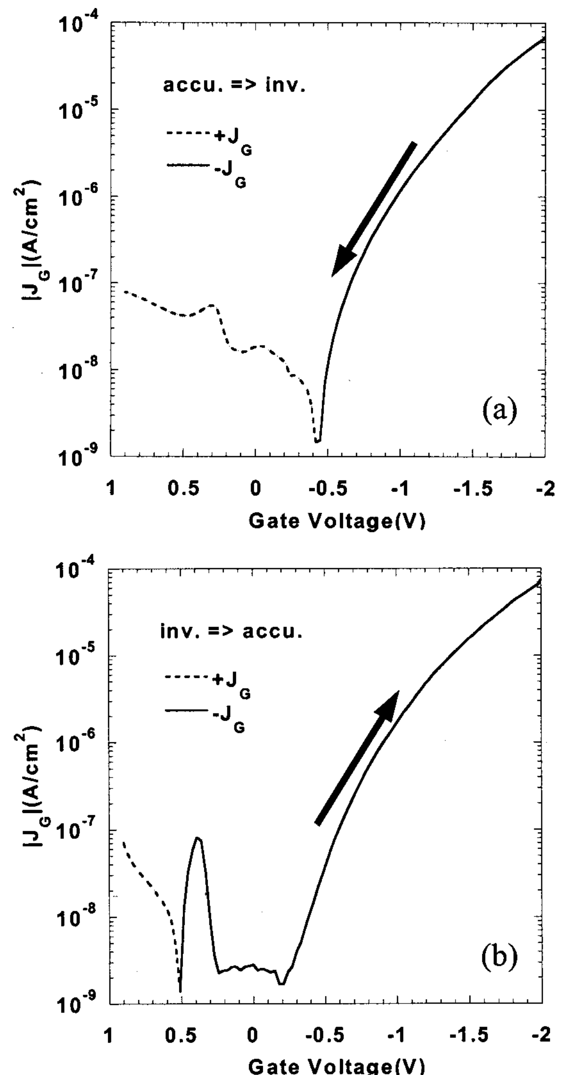

FIG. 8. (a) Absolute values of the current-density vs voltage characteristics sweeping from accumulation to inversion. (Turn-around voltage $= -0.4$ V). (b) Absolute values of the current-density vs voltage characteristics sweeping from inversion to accumulation. (Turn-around voltage $= +0.5$ V).

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the C–V characteristics for measuring the curve by sweeping the voltage from accumulation to inversion and then sweeping back (-2.0 V$\Rightarrow+1.0$ V$\Rightarrow-2.0$ V). A shift of about 45 mV is observed. The dashed line is the curve measured by sweeping from inversion to accumulation and then sweeping back. A shift of 45 mV is also observed. However, when light was applied during the measurement, the shift increased to 110 mV, as shown in Fig. 4(b). To explore the reason for this phenomenon, a bias temperature stress (BTS) of $V_g = \pm 0.7$ V, 125 °C for 30 min was applied to the sample. For BTS of both positive and negative polarities, as shown in Fig. 5, no significant C–V curve shifts were observed. It was concluded that the hysteresis phenomenon was not caused by the mobile ion effect.

As revealed by the TEM picture of Fig. 2, there exists a thin silicate layer between the ZrO_2 and silicon substrate. An energy band diagram of the TiN/ZrO_2/Zr-silicate/p-Si structure was recently reported.[24] Due to the imperfect structure of the interface between the ZrO_2 and Zr-silicate, it would be expected that this interface would act as charge trapping centers. Therefore, an inner-interface trapping model as shown in Fig. 6 is proposed to explain the hysteresis phenomenon. When the capacitor is first at accumulation ($V_g = -2.0$ V), majority carriers (holes for the p-type Si substrate) tunnel from p-Si substrate through the Zr-silicate layer and are trapped at the inner-interface, as shown in Fig. 6(a). When the voltage is swept toward the positive direction, the C–V curve shifts negatively. Then, when the voltage is swept to the positive side to make the capacitor stay at inversion ($V_g = +1.0$ V), the trapped holes at the inner-interface will be de-trapped and at the same time minority carriers (electrons) will tunnel from the p-Si substrate and trapped at the inner-interface, as shown in Fig. 6(b). This makes the C–V curve shift positively when the voltage is swept toward the negative side. The mechanism makes the C–V curve have a hysteresis loop. As a light illumination is applied to the semiconductor, electron–hole pairs will be generated [see Fig. 6(c)], which make the above phenomenon more evident. Especially, the light illumination makes a more significant effect on minority carriers as seen from Fig. 4(b), where a larger voltage shift of 110 mV was observed for the voltage sweeping from inversion toward accumulation. The change on the majority carrier concentration was insignificant, thus making almost the same C–V curve as the voltage was swept from accumulation toward inversion.

Figure 7 shows the C–V curve shifts for two different thicknesses of the zirconium dielectrics. It shows that the thicker zirconium dielectric (dashed line) has a larger C–V curve voltage shift (100 mV) than that (45 mV) of the thinner. Based on our proposed model, as the thickness of the zirconium dielectrics increases, the relative distance of the inner-interface as compared to the total thickness of the dielectrics will be closer to the silicon substrate, resulting more shift of the C–V curve. Figures 8(a) and 8(b) show the absolute current density–voltage ($|J|$–V) characteristics of the dielectrics measured with the voltage swept from accumulation to inversion and from inversion to accumulation respectively. For Fig. 8(a), the current is negative and becomes positive at the gate voltage equaling -0.4 V, but for Fig. 8(b), the current is positive and becomes negative at the gate voltage equaling $+0.5$ V. This difference in the turn-around voltages of the current can also be explained by using the inner-interface trapping model. As the capacitor is at the accumulation region, holes are trapped at the inner-interface [see Fig. 6(a)], making the turn-around voltage of the current be at -0.4 V when the gate voltage is swept toward the inversion region; while as the capacitor is at the inversion region, electrons are trapped at the inner-interface [see Fig. 6(b)], making the turn-around voltage of the current be at $+0.5$ V when the gate voltage is swept towards accumulation.

IV. CONCLUSION

In conclusion, the hysteresis phenomenon of the zirconium dielectrics can be explained by using an inner-interface trapping model. The influence of light illumination on the hysteresis phenomenon is quite serious because of more charges trapped at the ZrO_2/Si-silicate interface. The model well explains not only the hysteresis effect but also the thickness effect of the C–V characteristics and the different turn-around voltages on the J–V characteristics of the zirconium dielectrics capacitor.

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