Device Modeling of Ferroelectric Memory Field-Effect Transistor (FeMFET)

Hang-Ting Lue, Chien-Jang Wu, *Member, IEEE*, and Tseung-Yuen Tseng, *Fellow, IEEE*

Abstract—**A numerical analysis of the electrical characteristics for the ferroelectric memory field-effect transistors (FeMFETs) is presented. Two important structures such as the metal–ferroelectric–insulator–semiconductor field–effect transistor (MFISFET) and metal–ferroelectric–metal–insulator–semiconductor field–effect transistor (MFMISFET) are considered. A new analytic expression for the relation of polarization versus electric field (P–E) is proposed to describe the nonsaturated hysteresis loop of the ferroelectric material. In order to provide a more accurate simulation, we incorporate the combined effects of the nonsaturated polarization of ferroelectric layers and the nonuniform distributions of electric field and charge along the channel. We also discuss the possible nonideal effects due to the fixed charges, charge injection, and short channel. The present theoretical work provides some new design rules for improving the performance of FeMFETs.**

Index Terms—**Ferroelectric memory field-effect transistors (FeMFET), ferroelectric, ferroelectric random access memory (FeRAM), memory, metal–ferroelectric–insulator–semiconductor (MFIS), metal–ferroelectric–metal–insulator–semiconductor (MFMIS), modeling, one transistor (1T), transistor.**

I. Introduction

THE ferroelectric random access memory (FeRAM) [1] has acquired much attention in recent years because they can provide nonvolatile memory operation with fast writing time. Among several possible device structures, the ferroelectric memory field-effect transistor (FeMFET) [2]–[7] having a nondestructive readout operation and high density is of vital interest. The FeMFET includes the MFISFET [2]–[5] and MFMISFET [6], [7]. In these device structures, the ferroelectric material is placed on the gate of the transistor. The stored dipole moments in the ferroelectric material can adjust the threshold voltages of an FeMFET and thus the drain current of each switching state can be discriminated and identified as a logic state in a memory.

There have been many reports on the fabrications of MFIS- and/or MFMIS-based FETs and capacitors thus far. The systematic theoretical methods [2], [3] for the characterization and prediction of the experimental results however remain rarely seen.

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TABLE I
Device Parameters for the Simulation of FeMFET in the Text

Parameter	Description	Values used in simulation
P_r	Remnant polarization	2.5 μC/cm^2
P_s	Saturation polarization	3 μC/cm^2
E_c	Coercive field	50 kV/cm
ε_F	Dielectric constant of ferroelectric	150
t_F	Ferroelectric film thickness	200 nm
EOT	Equivalent oxide thickness of insulator	4 nm
N_a	Substrate doping concentration (*p*-type)	10^{16} 1/cm^3
A_F	Ferroelectric film area (For capacitor)	1 cm^2 (For MFIS only)
A_I	Insulator film area (For capacitor)	1 cm^2
μ	Electron mobility (For FET)	300 cm^2/volt-sec
L	Channel length (For FET)	1 μm
W	Channel width (For FET)	1 μm

In order to theoretically investigate the electrical characteristics of an FeMFET, Miller *et al.* have first proposed a mathematical model [2]. In their model, the drain current calculated by using Brews charge sheet model [10] is not suitable for an FET operated in the saturation (after pinchoff) and subthreshold regions. The model simply assumes the electric field in the ferroelectric film to be constant, independent of the channel position [2], [3]. This assumption is only valid for the case of low drain voltage. In this paper, we shall remove these limitations and propose a more relevant model to include not only the nonsaturated polarizations of the ferroelectric layer but the nonuniform distribution of the field and charge along the channel position. Systematic analyses on the electrical characteristics for MFISFET and MFMISFET in addition to the associated capacitors will be made. The material and geometric parameters of these devices used are in a wide range in order to gain some physical insight about the operation of FeMFETs. The calculation algorithm will also be described in detail so that one can easily follow. We have used 12 parameters to describe the transistor (as listed in Table I), which are the required minimum physical parameters and no other phenomenological ones are needed. The results of the electrical properties of the FeMFETs will be shown to be independent of the value of equivalent oxide thickness (EOT) of the insulator. In addition, the insulator may be fabricated in a stacked structure rather than a single layer, for the purpose of better crystallization in some experiments. With these reasons and for a more general simulation purpose, the parameter of the insulator is indicated by a single EOT instead of the dielectric constant ε_I and thickness t_I ($EOT = t_I(\varepsilon_{\mathrm{SiO_2}}/\varepsilon_I)$).

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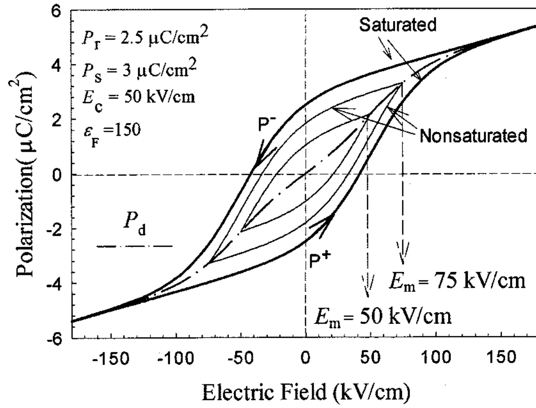

Fig. 1. P–E for the ferroelectric materials under various maximum electric fields in (1)–(6).

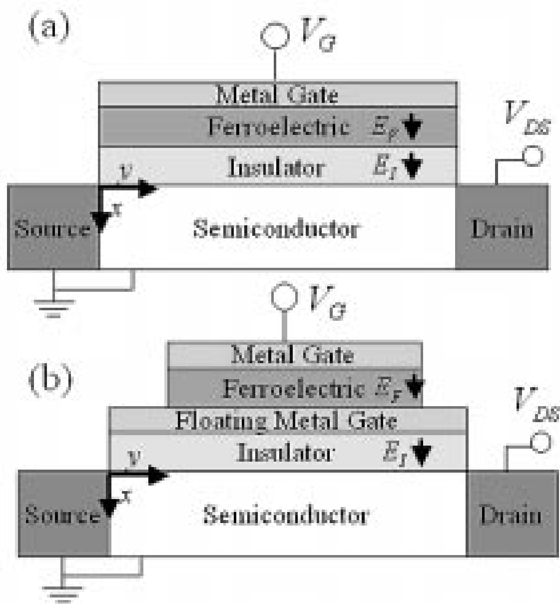

Fig. 2. Device structures and the associated sign conventions for the (a) MFISFET and (b) MFMISFET.

II. Phenomenological Model of Polarization Electric Field (P–E) of the Ferroelectric Capacitors

Miller *et al.* [8] have proposed a simple model to fit the experimental polarization–electric field (P–E) relationship in a ferroelectric capacitor, namely

$$P^{+}(E) = P_s \tanh\left(\frac{E-E_c}{2\delta}\right) + \varepsilon_F\varepsilon_0 E \tag{1}$$

where

$$\delta \equiv E_c \left(\ln\left(\frac{1+\frac{P_r}{P_s}}{1-\frac{P_r}{P_s}}\right)\right)^{-1} \tag{2}$$

$$P^{-}(E) = -P^{+}(-E). \tag{3}$$

Here, $P^{+}(E)$ indicates the lower (positive-going) branch of the P–E relation, while $P^{-}(E)$ is the upper (negative-going) branch. The last term $\varepsilon_F\varepsilon_0 E$ in the right hand side of (1) denotes the linear contribution of the dipole moment. Equations (1)–(3) fit well into the P–E relation of the saturated hysteresis loop. They cannot, however, describe the nonsaturated (minor) situation. We now construct a new expression for the minor hysteresis loop within the framework of the previous model. The minor hysteresis loop is supposed to be determined by a parameter, E_m, the maximum electric field that the ferroelectric layer may undergo. The minor hysteresis loop consists of two branches, $P^{+}(E,E_m)$ and $P^{-}(E,E_m)$. Since E_m is the maximum electric field, it is expected that $P^{+}(E,E_m)$ and $P^{-}(E,E_m)$ must intersect there. Together with the fact stated in [8], "existing data indicate that the derivative of the polarization with respect to the electric field, evaluated at a constant field, is independent of the amplitude of the applied signal, at least to first order," the minor loops can be derived and given by

$$\begin{aligned} P^{+}(E,E_m) =& P_s \tanh\left(\frac{E-E_c}{2\delta}\right) + \varepsilon_F\varepsilon_0 E \\ &+ \frac{1}{2}\left(P_s \tanh\left(\frac{E_m+E_c}{2\delta}\right)\right. \\ &\left. - P_s \tanh\left(\frac{E_m-E_c}{2\delta}\right)\right) \end{aligned} \tag{4}$$

$$\begin{aligned} P^{-}(E,E_m) =& P_s \tanh\left(\frac{E+E_c}{2\delta}\right) + \varepsilon_F\varepsilon_0 E \\ &- \frac{1}{2}\left(P_s \tanh\left(\frac{E_m+E_c}{2\delta}\right)\right. \\ &\left. - P_s \tanh\left(\frac{E_m-E_c}{2\delta}\right)\right). \end{aligned} \tag{5}$$

The polarization as a function of the maximum electric field is defined by

$$\begin{aligned} P_d(E_m) = \varepsilon_F\varepsilon_0 E_m &+ \frac{1}{2}\left(P_s \tanh\left(\frac{E_m+E_c}{2\delta}\right)\right. \\ &\left. + P_s \tanh\left(\frac{E_m-E_c}{2\delta}\right)\right). \end{aligned} \tag{6}$$

Two calculated minor loops of P–E are depicted in Fig. 1. The unpolarized ferroelectric material is first at the origin ($P=0, E=0$). Once the applied field is increased, the dipole moment will follow the curve of $P_d(E_m)$ until the maximum electric field E_m is reached. Then the polarization will follow $P^{+}(E,E_m)$ and $P^{-}(E,E_m)$ along the direction indicated in Fig. 1.

Equations (4)–(6) are simple and analytic and they can be used to simulate the characteristics for a ferroelectric-based device. Although they are not suitable for the case of the applied voltage being arbitrarily asymmetrical as stated in the [9], yet they are time-saving in the computer calculation.

III. C–V Simulation of the Capacitors

The structures of MFISFET and MFMISFET together with the sign conventions are depicted in Fig. 2. For the capacitance–voltage (C–V) simulation of MFIS capacitor, the continuous boundary condition for the normal electric displacement is

$$D = \varepsilon_0 E_F + P(E_F) = \varepsilon_I\varepsilon_0 E_I = \varepsilon_{\rm Si}\varepsilon_0 E_{\rm Si} \tag{7}$$

where E_F, E_I, and E_{Si} are the electric fields in the ferroelectric layer, insulator, and semiconductor (Si), respectively. We can ignore $\varepsilon_0 E_F$ in (7) because it is much smaller than the dipole moment $P(E_F)$. Gauss's law gives $\varepsilon_{\mathrm{Si}}\varepsilon_0 E_{\mathrm{Si}} = -Q_s(\psi_s)$, where $Q_s(\psi_s)$ is the space charge (per unit area) in the semiconductor and ψ_s is the surface band bending potential. Equation (7) can then be rewritten as

$$P(E_F) = -Q_s(\psi_s), \tag{8}$$
$$\frac{\varepsilon_I \varepsilon_0}{t_I} V_I = \frac{\varepsilon_{\mathrm{SiO_2}}\varepsilon_0}{EOT} V_I = -Q_s(\psi_s). \tag{9}$$

The corresponding voltage drops in the ferroelectric layer and insulator are V_F and V_I, respectively. The space charge density $Q_s(\psi_s)$ is given in [10].

The total gate voltage is given by

$$V_G = \psi_s + V_I + V_F. \tag{10}$$

Assuming the unpolarized ferroelectric film is first at the origin ($E = 0, P = 0$), then the dipole moment will follow $P_d(E_m)$. Given the maximum writing gate voltage, $+V_W$ or $-V_W$ and solving, with the help of Newton's method, (8)–(10), one can find the corresponding surface band bending potential ψ_s as well as the maximum electric field E_m in the ferroelectric layer. Once E_m is determined, two branches $P^+(E, E_m)$ and $P^-(E, E_m)$ in (4) and (5) are explicitly determined. Repeatedly solving (8)–(10) by sweeping gate voltage from $-V_W$ to $+V_W$ and using $P^+(E, E_m)$, then ψ_s, V_I and V_F as a function of gate voltage can be obtained. Similarly, one can find ψ_s, V_I and V_F by sweeping from $+V_W$ to $-V_W$ together with $P^-(E, E_m)$. The reason for the direction will be further discussed in Section V.

The capacitance, obtained from the series combination of the multilayered capacitors, is expressed as

$$C_{total} = \left(\frac{1}{C_I} + \frac{1}{C_F} + \frac{1}{C_D(\psi_s)}\right)^{-1} \tag{11}$$

where

$$C_I = \frac{A_I \varepsilon_I \varepsilon_0}{t_I} = \frac{A_I \varepsilon_{\mathrm{SiO_2}}\varepsilon_0}{EOT} \tag{12}$$
$$C_F = \frac{A_F \varepsilon_F \varepsilon_0}{t_F} \tag{13}$$

and $C_D(\psi_s)$ is the capacitance of semiconductor given in [10].

As for MFMIS capacitor in Fig. 2(b), the area of ferroelectric is different from that of the insulator. Then (8) should be modified as

$$A_F P\left(\frac{V_F}{t_F}\right) = \frac{A_I \varepsilon_{\mathrm{SiO_2}}\varepsilon_0}{EOT} V_I. \tag{14}$$

Equations (11)–(13) describe the capacitance of semiconductor at low frequency. However, the capacitance at high frequency does not satisfy this relation at strong inversion. At high frequency, the generation rate of the charge carriers from the depletion region can not follow the rapid change of the applied signal and consequently the capacitance remains at the minimum value. Since the ordinary C–V is measured at high frequency, we constrain the capacitance to the minimum value at the strong-inversion condition.

IV. Simulation of Drain Current of FeMFETs

The drain current is calculated by using Pao and Sah's double integral [11], namely

$$I_D = q\mu \frac{W}{L} \int_0^{V_{DS}} \int_{\psi_B}^{\psi_S} \frac{\left(\frac{n_i^2}{N_a}\right) e^{\beta(\psi - V)}}{\xi(\psi, V)} d\psi dV \tag{15}$$

where $\psi_B = (kT/q)\ln(N_a/n_i)$, n_i is the intrinsic carrier concentration, and N_a is described in Table I. Here, $\xi(\psi, V)$ is the electric field at the insulator/semiconductor interface given in [11]. The double integral over the band bending potential ψ and the channel potential V includes the integration over the width of depletion region and the channel length. The channel potential is the relative change of the electron quasi-Fermi potential along the channel position with respect to the source. In (15), both drift and diffusion currents have been considered and consequently can be used to investigate the drain current for an FeMFET operating in all possible regions such as sub-threshold, triode and saturation. In addition, the electric field and surface band bending potential are assumed not to be constant along the channel, which appears to be more relevant than the previous models [2], [3]. For an MFISFET, the gate voltage is given by

$$V_G = \psi_s + \frac{Q_s(\psi_s, V)}{\frac{\varepsilon_{\mathrm{SiO_2}}\varepsilon_0}{EOT}} + E_F t_F \tag{16}$$

where

$$Q_s(\psi_s, V) = P(E_F, E_m) \tag{17}$$

where

$$Q_s(\psi_s, V) = \mp \frac{\sqrt{2}\varepsilon_{\mathrm{Si}}\varepsilon_0 kT}{qL_D} \cdot \left(\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right) + \frac{n}{p} e^{-\beta V} \cdot \left(e^{\beta\psi_s} - \beta\psi_s e^{\beta V} - 1\right) \right)^{1/2} \tag{18}$$

and $P(E_F, E_m) = P^+(E_F, E_m)$ or $P^-(E_F, E_m)$ for $-V_W \rightarrow +V_W$ or $+V_W \rightarrow -V_W$, respectively. Here E_m is the same as that in Section II for the capacitors. Equations (16) and (17) can be used to solve for ψ_s and E_F by Newton's method. The gate voltage V_G and drain voltage V_{DS} can be varied arbitrarily to obtain the desired current-voltage (I–V) relationship. Note that the value of V_G must be sufficiently large to ensure $\psi_s > \psi_B$. In the case $\psi_s < \psi_B$ such that the condition of no inversion is produced in the semiconductor surface, FeMFET then will be operated in the cutoff region, which is of no interest to us here.

The electric field, surface band bending and channel potentials as a function of the channel position can be calculated based on the original derivation of (15) [11]. With the fact that the drain current is unchanged at every channel position, y, we can

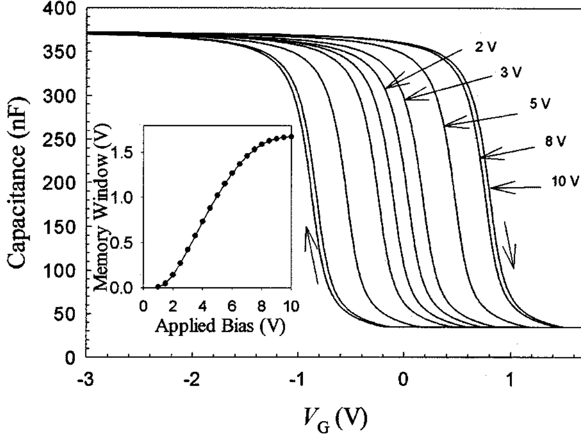

Fig. 3. C–V simulations of MFIS capacitor at various applied biases. The device parameters are defined in Table I. The inset shows the corresponding memory window as a function of applied bias.

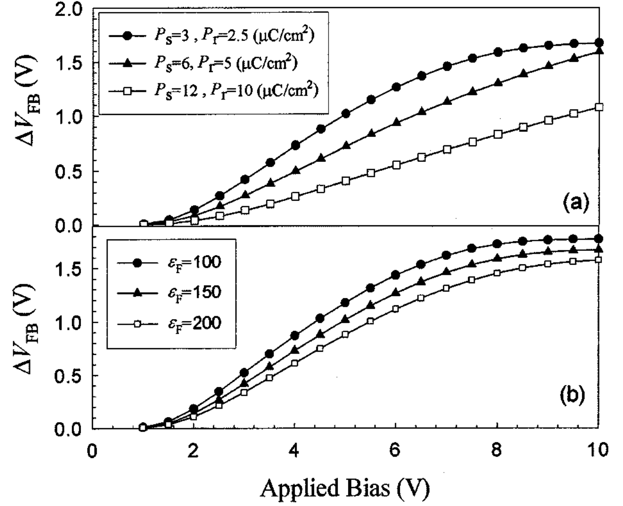

Fig. 4. Memory window as a function of applied bias of MFIS capacitor for (a) various P_s with a constant ratio of $P_r/P_s = 5/6$ and (b) various ε_F. The other parameters are the same as Table I.

integrate the drain current over the channel position. With the aid of the change of variable we then have

$$\begin{aligned} I_D\frac{y}{L} =&\frac{1}{L}\int_0^y I_D dy \\ =&q\mu\frac{W}{L}\int_0^{V(y)}\int_{\psi_B}^{\psi_S}\frac{\left(\frac{n_i^2}{N_a}\right)e^{\beta(\psi-V)}}{\xi(\psi,V)}d\psi dV \end{aligned} \quad (19)$$

where the drain voltage is integrated to $V(y)$ instead of V_{DS}. It seems to be a tedious task to solve (19) because it is an integral equation. In fact, without any additional numerical calculation there is a simple way of directly converting the I_D-V_{DS} plot to the $V(y) - y$ plot. Note that the channel position in (19) is more easily solved for a given channel potential because the right-hand side of (19) is simply the drain current if the drain voltage is $V(y)$. Therefore, if the I_D-V_{DS} plot is first calculated by changing the drain voltage V from 0 to V_{DS}, then $I_D(V)/I_D(V_{DS})$ can be simply converted to y/L whereas V just corresponds to the channel potential $V(y)$ at this bias condition. Upon getting the $V(y)$, the corresponding ψ_s, V_I and V_F are readily determined according to (16)–(18).

As for the MFMISFET, some different calculation procedures must be done because the floating metal gate will make the voltage across the ferroelectric V_F uniform in the longitudinal direction. As shown in Fig. 2(b), an MFMISFET can, in effect, be treated as a series of an MOSFET and an MFM capacitor. Thus by separately investigating the behaviors for these two devices enable us to analyze the characteristics of an MFMISFET. At a low drain voltage, the stored charges in MOSFET are closely equal to those in MOS capacitor. In this case, (9) and (14) can be employed to determine the gate voltage of MOSFET and the drain current may be found from (15).

V. Numerical Results and Discussion

The simulations to be done are for both the capacitor and transistor. The device and material parameters used in the present study are listed in Table I. The EOT of the insulator is set to be 4 nm and the ferroelectric is chosen to have a moderate polarization in order to obtain a suitable memory window at the low operation voltages.

In Fig. 3, we plot the C–V memory window for an MFIS capacitor. The window is opened wider as the bias voltage is increased, reaching a saturated value for a larger applied bias as displayed in the inset of Fig. 3. The memory window width is defined as the flat-band voltage shift of the two aligned directions of the polarizations. At flat-band condition, $\psi_s = 0$ and then both V_I and the polarization of ferroelectric film are equal to zero according to (11) and(12). Thus the flat-band gate voltage is simply the voltage in ferroelectric, V_F. The maximum memory window at large bias can be calculated by $2E_c' t_F$, where E_c' is the electric field with zero polarization. Accordingly, the maximum memory window under large applied bias can then be derived as

$$\Delta V_{FB}(\max.) = 2E_c' t_F \approx 2E_c t_F \left(1 - \frac{2\delta\varepsilon_F\varepsilon_0}{P_s}\right). \quad (20)$$

Equation (20) agrees with the maximum value obtained in the inset of Fig. 3.

Although it is common to recognize that the hysteresis direction for C–V curve should follow the direction in Fig. 3, its physical reason however is rarely given thus far. We now give an explanation on it. If one applies a writing voltage ($V_W < 0$), then the electric field generated in the ferroelectric and the insulator should be negative-valued according to the sign convention in Fig. 2. The polarization will then follow the lower branch P^+ based on the description in Section II. At the flat-band condition, the polarization is zero and the corresponding electric field is positive-valued. Hence the flat-band gate voltage is positive. Similarly, the flat-band gate voltage is negative for a positive writing voltage ($V_W > 0$). Consequently, the hysteresis loop will trace the clockwise direction as demonstrated in Fig. 3. Likewise, the hysteresis loop will trace counterclockwise direction for an n-type substrate.

Shown in Figs. 4–6 are the memory windows as a function of bias voltage at various material parameters for an MFIS capacitor. Figs. 4(a), (b) and 5(a) show the effect of P_s, ε_F and EOT on the memory window, respectively. The results imply

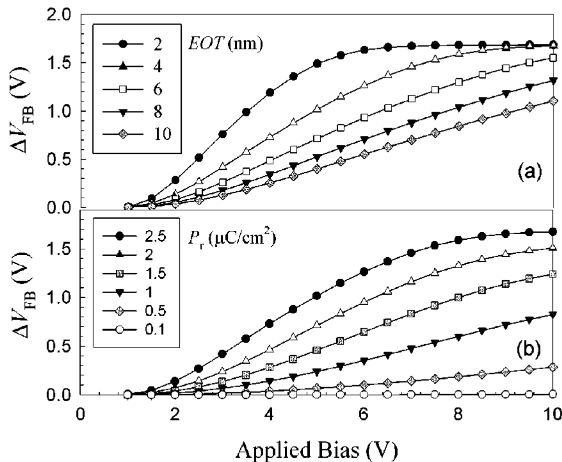

Fig. 5. Memory window as a function of applied bias of MFIS capacitor at different values of (a) EOT of insulator and (b) P_r at the condition of a constant value of P_s. The other parameters are the same as Table I.

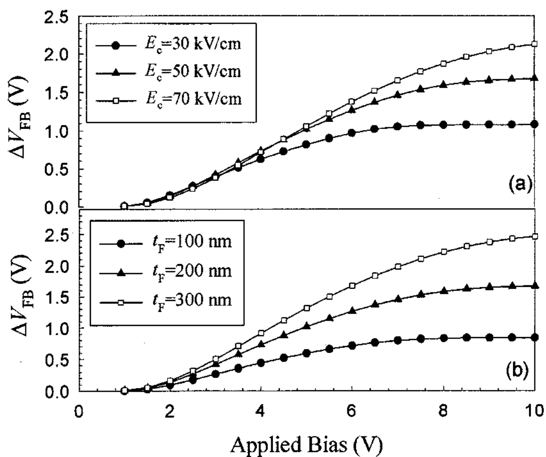

Fig. 6. Memory window as a function of applied bias of MFIS capacitor for various values of (a) E_c and (b) t_F. The other parameters are the same as Table I.

that the decrease in P_s, ε_F and EOT is necessary for capacitance matching of the ferroelectric and insulator layers so that the voltage drop in the ferroelectric layer can be increased to drive the ferroelectric into larger minor loop. Fig. 5(b) shows the memory window versus bias voltage at various values of P_r for a fixed P_s. The memory window is enhanced with increasing P_r. Several literatures [5] have stated that a small polarization ($P_r > 0.1\ \mu\text{C/cm}^2$) is sufficient to obtain the memory window. We think that this assumption is incorrect because a small value of P_r would result in the linear-like P–E curve, leading the ferroelectric to behave closely to the paraelectric phase. The memory window for $P_r = 0.1\ \mu\text{C/cm}^2$ is very small, as indicated in Fig. 5(b). Therefore, increasing the ratio P_r/P_s, or equivalently obtaining a square-like hysteresis loop, is essential for obtaining a large memory window.

Fig. 6 illustrates the effects of coercive field and thickness of ferroelectric layer on the memory window. Larger values in E_c and t_F generally increase the memory windows at the same writing voltage but the writing voltage should be increased to obtain the saturated memory window. Although increasing E_c and t_F enhance the memory window, the devices are operated in a smaller minor hysteresis loop at low operation voltages. We believe the ferroelectric thin film in the saturated polarization is more stable (such as retention characteristics) than that in a minor loop. Therefore, certain trade-off should be made to optimize the material parameters.

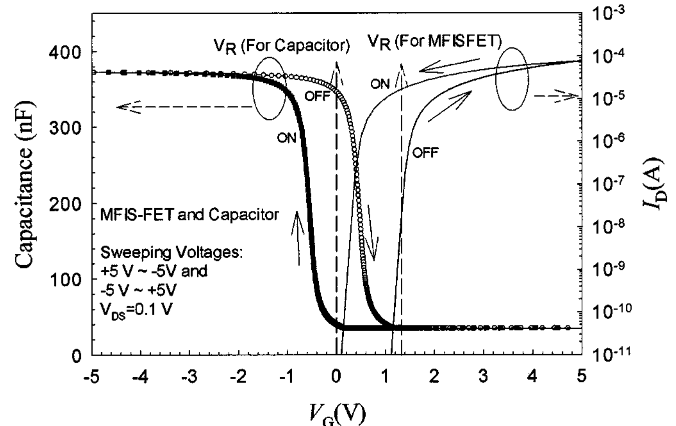

Fig. 7. C–V and I_D–V_G simulations of MFIS capacitor and MFISFET. The device parameters are given in Table I. The direction of memory window is also shown here.

Both C–V relationship of MFIS capacitor and I_D–V_G curve of MFISFET are shown in Fig. 7 for the purpose of comparison. The drain current shows a similar memory window to the C–V curve. The results shown here indicate that the threshold voltages of these two states are effectively separated by the two directions of polarization in the ferroelectric and then can be identified as two states: "ON " and "OFF". In order to have a better sense margin, a suitable choice of V_R for an FeMFET is shown in Fig. 7 in which the drain current ratio $I_D(\text{ON})/I_D(\text{OFF})$ is larger than 10^3, suitable for memory operation.

Reported studies in the literatures mostly focused only on MFIS capacitors because they are easy to fabricate and useful for material characterization. For MFIS capacitor, a suitable reading voltage V_R must be selected so that the difference in capacitance is large, as seen in Fig. 7. However, V_R for MFIS capacitor is different from that for FeMFET. Therefore, it is worthy of mentioning that if measurements such as retention and fatigue issues are carried out with a defined V_R, one then should note that the measured results for both MFIS capacitor and FeMFET may be different because of their distinct values in V_R.

Fig. 8 demonstrates the drain current as a function of the drain voltage for both ON- and OFF-state. We can see that the drain current of OFF-state is less than that of ON-state at the same bias condition. A simple insight can be gained from this figure. The threshold voltage of ON-state is smaller than that of OFF-state by about 1 V, namely the drain current of ON-state at $V_G = 3$ V is close to that of OFF state with $V_G = 4$ V. Likewise, the drain current at $V_G = 2$ V (ON) is close to that at $V_G = 3$ V (OFF).

Fig. 9 shows the drain current versus gate voltage at various writing voltages of ± 3 V $\sim \pm 10$ V. The memory window of the drain current increases with increasing writing voltage, which is similar to C–V curves indicated in Fig. 3. The inset is the corresponding P–E curve of the ferroelectric layer for each state.

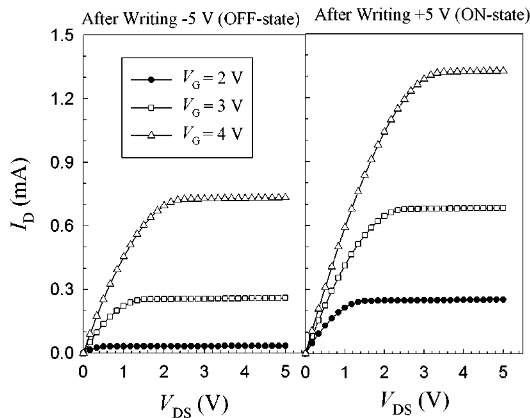

Fig. 8. I_D-V_{DS} simulations of MFISFET for the ON and OFF states with various V_G. The device parameters are given in Table I.

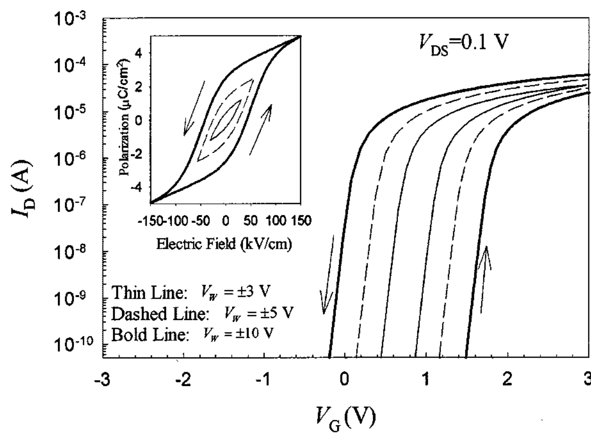

Fig. 9. I_D-V_G simulations of MFISFET for various writing voltages, V_W. The device parameters are given in Table I. The inset shows the corresponding P–E relations of the ferroelectric material.

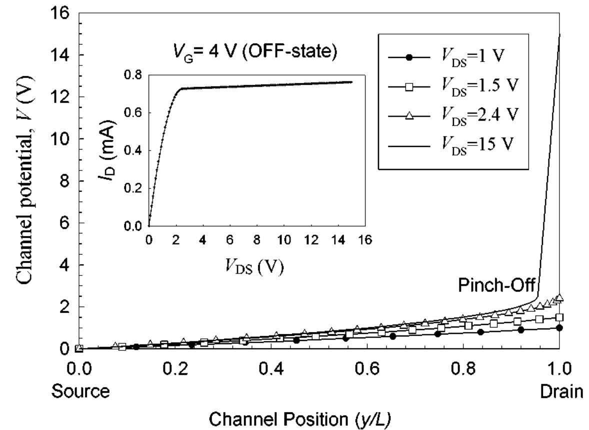

Fig. 10. Channel potential V as a function of the channel position for various drain voltages of MFISFET. The inset shows the plot of I_D-V_{DS} at $V_G = 4$ V for the OFF state in Fig. 8.

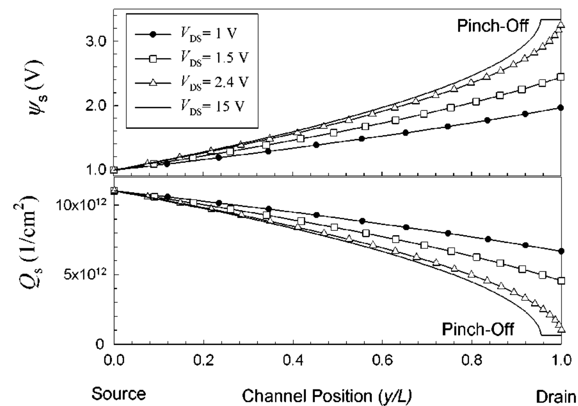

Fig. 11. Surface band bending ψ_s and Surface charge density Q_s as a function of the channel position for various drain voltages of MFISFET.

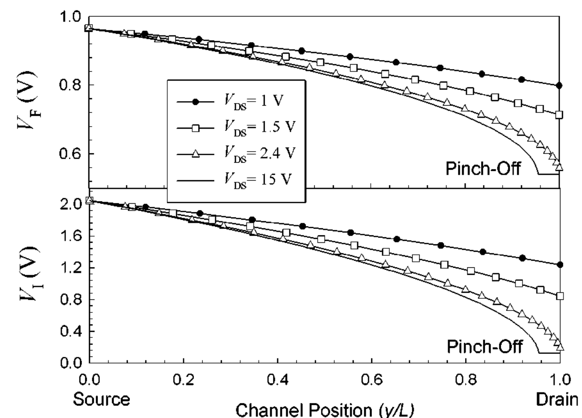

Fig. 12. Voltage drop across the ferroelectric layer V_F and insulator layer V_I as a function of the channel position for various drain voltages of MFISFET.

The results indicate that a larger writing voltage would enhance the polarization to a larger minor hysteresis loop.

The channel potential (or electron quasi-Fermi potential), surface band bending, space charge density, V_F and V_I are shown in Figs. 10–12. Fig. 10 shows the results of channel potential, in which we employ the plot of drain current versus drain bias in the inset. The maximum drain voltage is taken to be high (15 V) to clearly illustrate the after pinchoff (or saturation region) behavior. The band bending and channel potential generally increase from the source to drain. When the drain voltage is larger than about V_G-V_T (where V_T is the threshold voltage), the channel becomes "pinchoff" and the band bending is constant, as shown in Fig. 11. The space charge density near the drain attains a very small value and the depletion region mainly contributes to the remnant space charges. As seen in Fig. 10, the electron quasi-Fermi potential (V) drops pronouncedly from the drain to the pinchoff point. This causes a large gradient in the quasi-Fermi potential and it will compensate the small space charge density and keep the drain current constant. In Fig. 12, it is indicated that both V_F and V_I decrease from the source to the drain. The V_I will decrease to a very small value after pinchoff while there is still a remanent value of V_F. In the calculation of Miller *et al.* [2], the voltages in the insulator and the ferroelectric have been assumed to be constant for convenience. This assumption would lead to a large deviation at a large drain voltage. However, in our model here, we remove this limitation and the distributions of voltages are calculated as well.

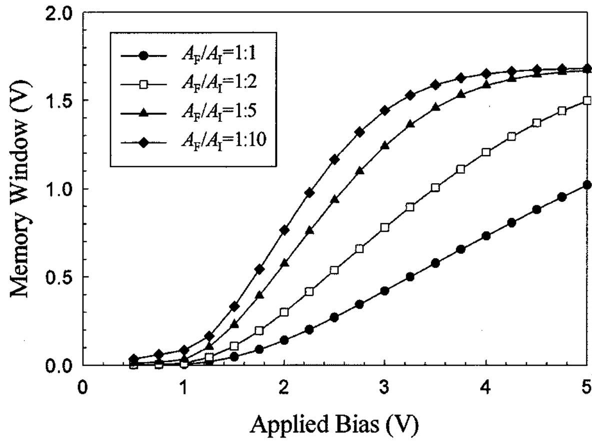

Fig. 13. Memory windows as a function of applied bias of MFMIS capacitor with various area ratios A_F/A_I. The other parameters are the same as Table I.

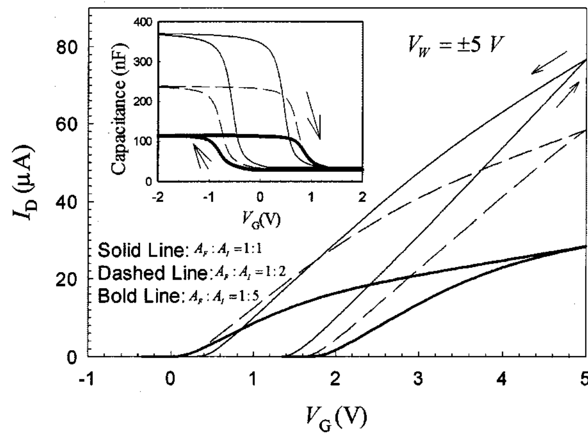

Fig. 14. I_D–V_G simulations for MFMISFETs with various area ratios A_F/A_I. The other device parameters are given in Table I. The inset is the corresponding C–V relation of MFMIS capacitors with the same A_F/A_I as in MFMISFETs.

For MFMIS capacitor, the memory windows increase with decreasing area ratio, A_F/A_I, as shown in Fig. 13. For a small value in area ratio, the memory window increases with applied bias and attains the maximum memory window rapidly. Fig. 14 displays the I_D–V_G of MFMISFET and C–V of MFMIS capacitor for various area ratios at the writing voltages of ±5 V. The memory window increases from 1 V to 1.7 V as the area ratio decreases from 1 to 0.2. The MFMIS structures with small area ratio can easily drive the ferroelectric layer to saturated polarization, which is more stable than a minor loop and is expected to have a longer retention time [6], [7] and better repeatability of threshold voltage during switching. However, the accumulation capacitance and the drain current decrease when the area ratio is decreased. This phenomenon is due to the decrease in total gate capacitance of the MFMIS structure that arises from the decrease of area of MFM, as shown in the inset of Fig. 14. The decreasing drain current effectively reduces the current ON/OFF ratio in spite of the increasing memory window, which is a drawback of the device performance. The device designers, therefore, should make certain tradeoffs between the memory window and the drain current when the area ratio decreases.

VI. Other Possible Effects

A. Fixed Charges

For an MFIS structure, the fixed charges may reside at the interface of ferroelectric/insulator or of insulator/semiconductor. Denoting respectively the fixed charges as Q_{FI} and Q_{IS}, Gauss's law then gives

$$Q_{IS} = -Q_s(\psi_s) - \frac{\epsilon_I \epsilon_0}{t_I} V_I \tag{21}$$

and

$$Q_{FI} = \frac{\epsilon_I \epsilon_0}{t_I} V_I - P^{\pm}\left(\frac{V_F}{t_F}, E_m\right). \tag{22}$$

With the existences of Q_{FI} and Q_{IS}, the voltages across the insulator and ferroelectric should change to V_I' and V_F', respectively. Although (22) cannot be solved in an analytical form, we can expand the solution in the first —order term and the total shift in the gate voltage due to the fixed charge is then given by

$$\Delta V_G = (V_I' - V_I) + (V_F' - V_F) \approx -\left(\frac{Q_{IS}}{\frac{\varepsilon_I \varepsilon_0}{t_I}} + \frac{Q_{IS} + Q_{FI}}{\frac{\varepsilon_F \varepsilon_0}{t_F} + \frac{P_s}{2\delta t_F}}\right). \tag{23}$$

B. Charge Injection

In recent developments of MFIS structures there are many high dielectric constant materials for the insulators. However, with their small bandgaps and polycrystalline structures, they often have large leakage currents and low breakdown voltages. If the device parameter is not carefully designed, the applied voltage mostly lies in the insulator rather than in the ferroelectric film, causing a large leakage current or even breakdown. In addition, the interdiffusion problems often generate a large density of trap states, in which the charges may be stored. These effects cause charge injection, which is similar to the operation of flash memory. For example, if a large and negative gate voltage is applied to MFIS capacitor, a positive Q_{FI} will be generated due to the leakage currents in the insulator, leading to a negative shift (23) in flat-band voltage. Similarly, a large and positive gate voltage will induce a negative Q_{FI}, producing a positive shift in flat-band voltage. Note also that this charge injection can cause a hysteresis loop but with a reverse direction in the ferroelectric memory hysteresis loop. Accordingly, the charge injection will reduce the ferroelectric memory window or even results in the wrong hysteresis direction.

C. Short-Channel Effect

In Section IV, the current-voltage relationship is calculated from Pao and Sah's double integral. This formula is derived on the basis of the gradual channel approximation, in which the transverse electric field is much greater than the longitudinal one. However, for a short channel device, the influence of source/drain region on the channel and the effect of velocity saturation become important. The overall short channel effects will eventually reduce the drain current that is less than the value estimated in Section IV and increase the subthreshold slope. However, we believe the threshold voltage change between the two polarization states are still close to the estimated using our

method, at least in the first order. There also exist many complicated effects. For example, the thickness of ferroelectric film incorporated in FeMFET is often several thousands of angstroms, which is comparable to the channel length if submicron transistor is fabricated. Therefore, the fringing electric fields exist outside the gate area and this effect in turn reduces the gate control capabilities of the transistors. This similar effect has been proposed by Chen *et al.* [12] for the transistors made of high-k gate dielectrics.

VII. Conclusion

In summary, some detailed numerical analyses of MFISFET, MFMISFET, and the associated capacitors have been made for the various material and device parameters. We have presented a new simple and analytical P–E relation for the ferroelectric material, including the nonsaturated polarization. Based on this analytical formula along with Pao and Sah's double integral for the drain current, the electrical characteristics of the above devices can be investigated. First, we have successfully simulated the C–V memory windows at various applied biases. A simple and clear explanation on the direction of the memory window is also given. Second, the nonuniform distributions of the field and charge along the channel position of the FeMFETs have been taken into account from Pao and Sah's double integral. The drain current of the FeMFETs operated in all possible regions except the cut-off region can be calculated by this way. Third, other possible effects such as fixed charge, charge injection and the short channel effect are also addressed in the present study.

For the MFIS and MFMIS structures, we have found some useful design rules for improving the device performance: Decreasing P_s and ε_F, increasing P_r/P_s ratio and reducing EOT of the insulators and A_F/A_I of the MFMIS structures are the important factors to obtain a saturated memory window at a low operation voltage. Increasing E_c and t_F may also result in a larger memory window, while the voltage required to drive the ferroelectric into saturated polarization is higher. In addition to the memory window, other issues should also be considered. For example, decreasing P_s and ε_F, reducing A_F/A_I of the MFMIS structures and increasing t_F will reduce the drain current and then the current ON/OFF ratio is decreased. Care must be taken to avoid possible breakdown or charge injection of the insulator due to the small thicknesses and high voltage drops across them. Besides, it is suggested to operate the FeMFETs in saturated polarizations for better retention characteristics. Therefore to optimize the device performances, certain tradeoff between these parameters should be made. If some clear device specifications are given, the present simulation method can provide the optimization of the device parameters.

References

[1] A. Sheikholeslami and P. G. Gilak, "A survey of circuit innovations in ferroelectricrandom-access memories," *Proc. IEEE*, vol. 88, pp. 667–689, 2000.

[2] S. L. Miller and P. J. McWhorter, "Physics of the ferroelectric nonvolatile memory field effect transistor," *J. Appl. Phys.*, vol. 72, no. 12, pp. 5999–6010, 1992.

[3] M. Ullmann, H. Goebel, H. Hoenigschmid, and T. Hander, "A BSIMS3v3 and DFIM based ferroelectric field effect transistor model," *IEICE Trans. Electron*, vol. 83, no. 8, pp. 1324–1330, 2000.

[4] E. Tokumitsu, R. Nakamura, and H. Ishiwara, "Nonvolatile memory operation of metal—Ferroelectric—Insulator—Semiconductor (MFIS) FETs using PLZT/STO/Si(100) structures," *IEEE Electron Device Lett.*, vol. 18, pp. 160–162, Apr. 1997.

[5] K. H. Kim, J. P. Han, S. W. Jung, and T. P. Ma, "Ferroelectric RAM (FEDRAM) FET with metal/$SrBi_2Ta_2O_9$/SiN/Si gate structure," *IEEE Electron Device Lett.*, vol. 23, pp. 82–84, Feb. 2002.

[6] E. Tokumitsu, T. Isobe, T. Kijima, and H. Ishiwara, "Fabrication and characterization of metal—Ferroelectric—Metal—Insulator—Semiconductor (MFMIS) structures using ferroelectric $(Bi, La)_4Ti_3O_{12}$ films," *Jpn. J. Appl. Phys.*, vol. 40, pp. 5576–5579, 2001.

[7] E. Tokumitsu, K. Okamoto, and H. Ishiwara, "Low voltage operation of nonvolatile metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS)-Field-Effect-Transistors (FETs) using Pt/$SrBi_2Ta_2O_9$/Pt/$SrTa_2O_6$/SiON/Si structures," *Jpn. J. Appl. Phys.*, vol. 40, pp. 2917–2922, 2001.

[8] S. L. Miller, R. D. Nasby, J. R. Schwank, M. S. Rodger, and P. V. Dressendorfer, "Device modeling of ferroelectric capacitors," *J. Appl. Phys.*, vol. 68, no. 12, pp. 6463–6471, 1990.

[9] S. L. Miller, J. R. Schwank, R. D. Nasby, and M. S. Rodger, "Modeling of ferroelectric capacitor switching with asymmetry nonperiodic input signals and arbitrary initial conditions," *J. Appl. Phys.*, vol. 70, no. 5, pp. 2849–2860, 1991.

[10] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1983, ch. 7 and 8.

[11] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 3.

[12] B. Cheng, M. Cao, R. Rao, A. Inani, P. V. Voorde, W. M. Greene, J. M. C. Stork, Z. Yu, P. M. Zeitzoff, and J. C. S. Woo, "The impact of high-k gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, pp. 1537–1544, July 1999.

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