# Design of a Wide-Band Frequency Synthesizer Based on TDC and DVC Techniques

Terng-Yin Hsu, Terng-Ren Hsu, Chung-Cheng Wang, Yi-Chuan Liu, and Chen-Yi Lee

***Abstract*—A wide-band frequency synthesizer based on time-to-digital (TDC) and digital-to-voltage (DVC) conversion techniques is proposed here. The proposed frequency synthesizer has the capabilities of jitter reduction and large bandwidth, making it more robust for high-frequency applications. A test chip is designed and fabricated in 0.6-$\mu$m CMOS single-poly triple-metal process. Here, the novel DVC circuit is realized by tristate inverters, where the resolution can achieve 0.2 mV. Control stability of jitter can improve about 24 dB by exploiting the TDC-based controller. In order to achieve high output frequency and large output range, an analog voltage-controlled oscillator is designed to provide a locked range from 900 to 1900 MHz with $<$ 22 kHz resolution at 3.3 V. Simulation and test results show that the proposal can work as expected. Moreover, the TDC-based controller can be treated as soft IP to speed up turnaround time.**

***Index Terms*—ADPLL, clock generator, DVC, frequency synthesizer, IP, mixed mode, SOC, TDC.**

## I. Introduction

FOR MOST applications, noise and jitter are important issues in system integration to meet system performance as well as to reduce costs. In other words, each part (chip) must be able to tolerate and handle many imperfections to make integration easier, such as noise coupling, voltage variation, and jitter effects. Recently, the frequency synthesizer has become almost an essential component in both chips and systems, where its key characteristics are pulling range and jitter. Hence, the goal of this research is to design frequency synthesizers with both large pulling range and low controlled jitter.

To improve performance and decrease costs of system integration, more requirements and constraints must be taken into account in implementations. For advances and improvements of digital VLSI, all digital methodology has good capabilities in satisfying the above requirements of computer and communication applications in recent years. A major problem of traditional frequency synthesizers is the highly technology-dependent implementation. Therefore, a portable design approach is exploited in digital VLSI to improve system-on-chip (SOC) turnaround time. For example, a robust on-chip system clock synthesizer is very important in high-speed microprocessors. Many phase-locked loop (PLL)/digital phase-locked loop (DPLL)-based designs can be found in the literature. In [1]–[3], several design techniques are presented to improve the performance of the PLL with analog low-frequency and current-controlled ring oscillators. In [4], an all-digital phase-locked loop (ADPLL)-based frequency synthesizer under 500-fs resolution is realized on 0.5-$\mu$m CMOS, however, it has large power consumption.

In order to cope with the portability issue with low cost,[1] a novel approach is proposed and developed in this paper to make use of advantages of digital VLSI. The proposed frequency synthesizer, based on time-to-digital (TDC) and digital-to-voltage (DVC) conversion techniques, has features of low controlled jitter and large pulling range. It is different from traditional approaches in the tracking and locking mechanisms. A new digital integrator is exploited to extract the period of the signal. To reduce jitter, an average processing mechanism is included to make output more clean and robust. In implementations, a tristate inverter-based digital-to-voltage converter is realized by connecting with different I/O types, and an analog voltage-controlled oscillator (VCO) is used to enhance output frequency over gigahertz. For systems, a finite-state controller can be applied to reduce controlled jitter with common I/O interfaces, and it can make integration more robust and easier. The proposed frequency synthesizer belongs to mixed-mode cell-based designs and has been verified on silicon using an in-house 0.6-$\mu$m CMOS cell library. According to the testing results, the frequency synthesizer can generate any frequency ranging from 900 to 1900 MHz with $<$ 22 kHz resolution at 3.3 V.

The rest of this paper is organized as follows. The algorithm for jitter reduction and frequency search is first addressed in Section II. The architecture of the frequency synthesizer is explained in Section III. Related circuit designs are represented in Section IV. Implementation and test results of the proposed solution are described and discussed in Section V.

## II. Algorithm

The concept of the proposed frequency synthesizer is to extract desired information from the reference clock by a digital mechanism. The most important issue is to reduce jitter, coupled with output of the frequency synthesizer or digital-controlled oscillator (DCO), and to generate a clean target frequency (period) based on the proposed extractions.

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[1]The low-cost issue is mainly focused on turnaround efficiency in SOC designs.

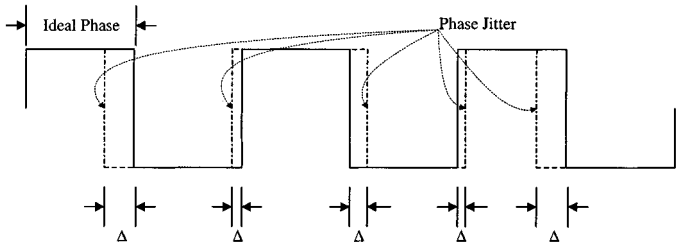


Fig. 1. Jitter phenomena modeled by uniform distribution.

### A. Jitter Reduction

To compensate jitter variation, digital signal processing (DSP) schemes are needed to eliminate such imperfections. At first, a hardware description language (HDL) jitter model must be established to verify proposed algorithms. For simplification without losing generality, the jitter phenomena are modeled by uniform distribution, as shown in Fig. 1, and formulated as

$$T_{\text{jitter}} = T_{\text{ideal}} + \sum_{j=0}^{1} \Delta_j \tag{1}$$

where $\Delta$ is a random variable distributed uniformly from $-a$ to $a$, $a$ is equal to the peak-to-peak jitter of the clock, and $T_{\text{ideal}}$ is the period of jitterless clock or named ideal frequency (period). It is assumed that all jitters are independent and identical distribution (i.i.d.) in statistics. With this model, many practical situations can be easily monitored during high-level simulation to improve designs.

In [5], there are many algorithms applied to compensate for distortions, however, many of them are too complex to be realized in a frequency synthesizer. On the other hand, complexity (cost) and power dissipation of frequency synthesizers are key parameters, which must be as small as possible. With considerations of complexity and performance, the average processing is considered here, where it can average the spectrum in the frequency domain or period in the time domain. For example, taking complexity into account, it is not flexible to average signals in the frequency domain because it needs more procedures for the Fourier transform. From (1), the time-domain average of periods is

$$\begin{aligned} T_{\text{average}} &= \frac{\sum_{i=0}^{n-1} T_{\text{jitter}(i)}}{n} \\ &= T_{\text{ideal}} + \frac{\sum_{i=0}^{n-1}\sum_{j=0}^{1} \Delta_{ij}}{n}. \end{aligned} \tag{2}$$

Note that the second term in (2) is an error after average. By the central limit theorem (CLT) [6], it is shown that the variance after average processing in (2) is less than origin (individual) in (1). It means that jitters have been reduced by average. In mathematics, it is impossible to completely remove jitter factors, however, it can be reduced to acceptable ranges by large numbers of average times $n$. On the other hand, it is possible to minimize errors in (2), but they cannot be reduced to zero. In addition, the response time is also proportional to $n$, which cannot be set too large because of physical limitations, such as size, complexity, power, and speed. From simulations, it is possible to get several combinations for design parameters and then to choose a proper solution that supports a good improvement of size, power, and jitter reduction under an acceptable response time. After averaging, the extraction of periods will be decided and the controller begins to search for a target clock. Hence, the average processing is recycled per $n$ to trade off error and response time.

### B. Frequency Search

Similar to [8], the frequency-search process is a kind of database searching problem, where a target frequency is just one of the possible solutions within a set. Because frequency and period are equivalent ($f = 1/T$), the searching procedure of frequency synthesizer is performed in the time domain. In other words, a target period is searched instead of frequency. We define a set of all available periods which is $[T_{\min}, T_{\max}]$ and a target period $T_{\text{target}}$ within the set. The key feature is how to find $T_{\text{target}}$ from $[T_{\min}, T\max]$. According to [7]–[9], the binary search is an efficient algorithm in implementations, where a searching procedure is made per one-half distance until it finds a solution. The disadvantage of the binary search is that a target may be missed during the search process. Hence, it needs to recycle several searches through the whole set before a solution is found. In order to compensate such a searching miss, a fix-step algorithm is included into the proposed algorithm. To trade off both missing probability [7] and searching efficiency, there are two searching conditions applied to meet requirements. One is a coarse search based on the binary search to improve efficiency, and the other is a fine search based on the fix-step algorithm to reduce missing probability. Thus, a threshold is created to determine which algorithm must be used to achieve the target.

In Fig. 2, it is assumed that the period of an initial clock is equal to $T_{\text{clock}}(0) = (T_{\min} + T_{\max})/2 = T_{\text{mid}}$. The target period (frequency) is denoted by $T_{\text{target}}$ within $[T_{\text{mid}}, T_{\max}]$ and the reference period, which is obtained by average processing of the reference clock in Section II-A, is $T_{\text{ref}} = (M/N)T_{\text{target}}$ where $N$ and $M$ are programmable constants. At first, the difference between $NT_{\text{ref}}$ and $MT_{\text{clock}}(0)$ is estimated, and then the status (fast/slow) of the initial clock divided by $M$ is determined. In the next searching cycle, a new period of an initial clock is decided by $T_{\text{clock}}(1) = T_{\text{clock}}(0) + T_{\text{mid}}/2$ and the same searching procedure is activated again. When the difference between $NT_{\text{ref}}$ and $MT_{\text{clock}}(k)$ is within the threshold, a fix-step algorithm will be selected to calculate a new period until it finds a target clock. Thus, the target period is equal to

$$\begin{aligned} T_{\text{target}} &= T_{\text{clock}}(k)|_{\text{Binary-Search}} + T_{\text{clock}}(C)|_{\text{fix-step}} \\ &= \left[T_{\text{clock}}(k-1) + \frac{T_{\text{mid}}}{2^k}\right] + \sum_{i=0}^{C-1} (\Delta\tau_i) \end{aligned} \tag{3}$$

where $C$ is a constant for total steps in the fix-step algorithm, and $\Delta\tau$ is the step size of the fix-step algorithm. The worst case time complexity of the frequency-search algorithm is $O(\log_2 n)$ [8]. Hence, the mathematical formulation for lock-in time is equal to

$$T_{\text{lock-in}} = (a \cdot \log_2 K) + n + C \tag{4}$$

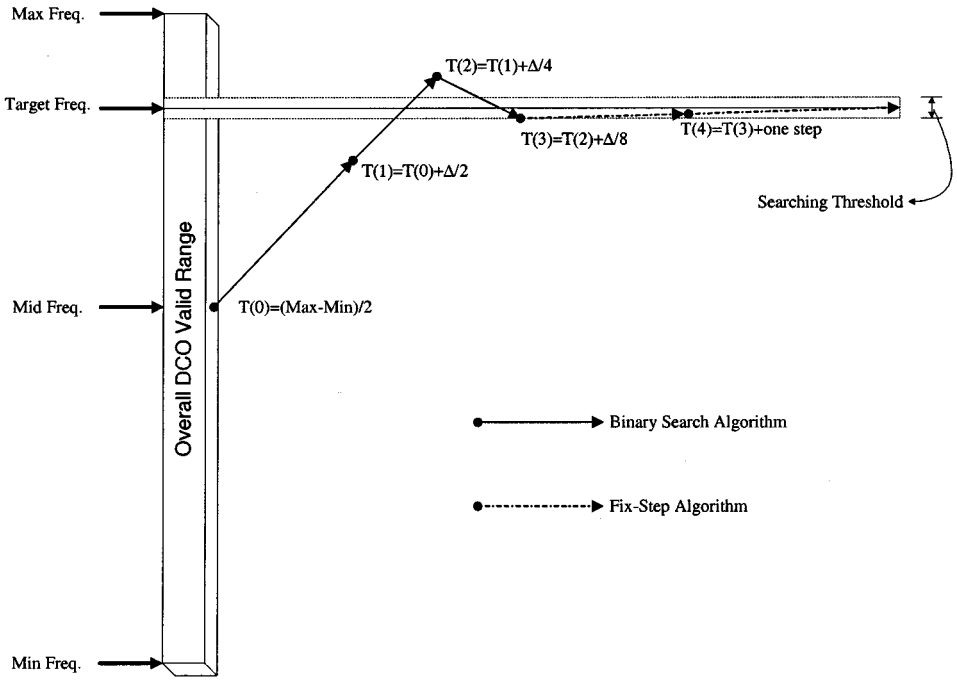


Fig. 2. Search algorithms and signal steps.

where $a$ is a constant of missing times of binary search, $K$ is the overall coarse-search stages within the set, and $n$ is a number of average in (2) (generally, $C << K$ and $n$).

## III. Architecture

According to the above descriptions, there are two building blocks to accomplish the proposed concept, namely, the finite-state machine (FSM) controller or named control IP which is used to search a possible solution or a target frequency from $[T_{\min}, T_{\max}]$, and a controllable oscillator which is to generate the output clock based on the temporary searching result, as shown in Fig. 3. There are three major blocks included in the control IP, namely, the digital integrator to extract the signal's information, the average unit for jitter reduction, and the frequency searcher whose purpose is to find a possible controlled condition of the oscillator. In order to connect with different interfaces, such as a digital controlled ring oscillator [8], [9] or VCO, it is necessary to add some converters among different I/O structures. With considerations of common interface of control IP, these I/O converters must combine with oscillators to form DCOs, as shown in Fig. 3.

In this paper, our definition of *low jitter* is the controlled stability of the DCO. This means that the low-jitter frequency search must be able to minimize or to isolate input jitter without losing accuracy. According to Section II-A, $n$ is an important parameter of jitter reduction. By simulation, a jitter variance is a function of $n$, and $n = 64$ or $128$ are proper numbers to trade off costs and performance. The operation of the proposed frequency synthesizer is presented as follows.

The function of the digital integrator is to convert frequency from time to digital numbers. By quantization, DSP techniques can easily be implemented to compensate imperfections (jitter). After being digitized, the quantized information will

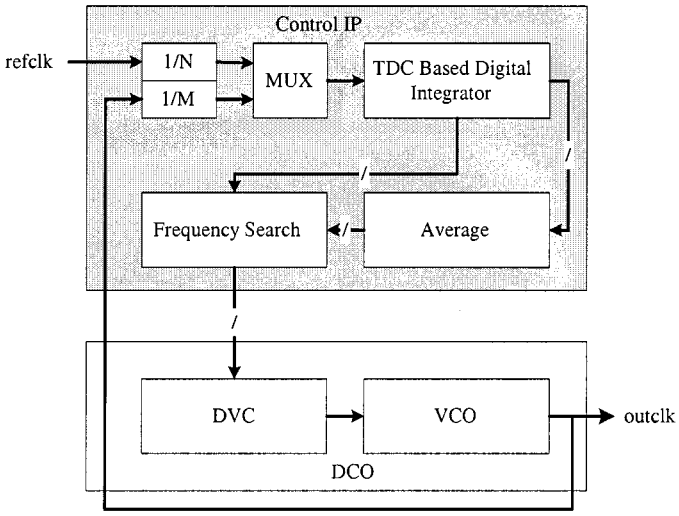


Fig. 3. Architecture of the proposed frequency synthesizer.

be averaged to reduce jitter and to improve extracted accuracy. According to the extractions, searching algorithms begin to find a possible solution for a target clock. If the target frequency is within the DCO bandwidth, searching algorithms always touch this solution. However, in probability, it may have to find a possible solution for a long search, as shown in (4) for $a > 1$. In physical environments, there are many imperfections and variations, such as quantized error, noise, voltage, and temperature, to cause the control IP to malfunction. In order to compensate jitter, voltage, and temperature variations, both average and searching procedures must be recycled, even if the loop finds a possible solution of target clock. The control-state diagram is shown in Fig. 4(a). For preventing mismatch, the frequency synthesizer only uses one digital integrator and one DCO to estimate and generate a target clock. The disadvantage

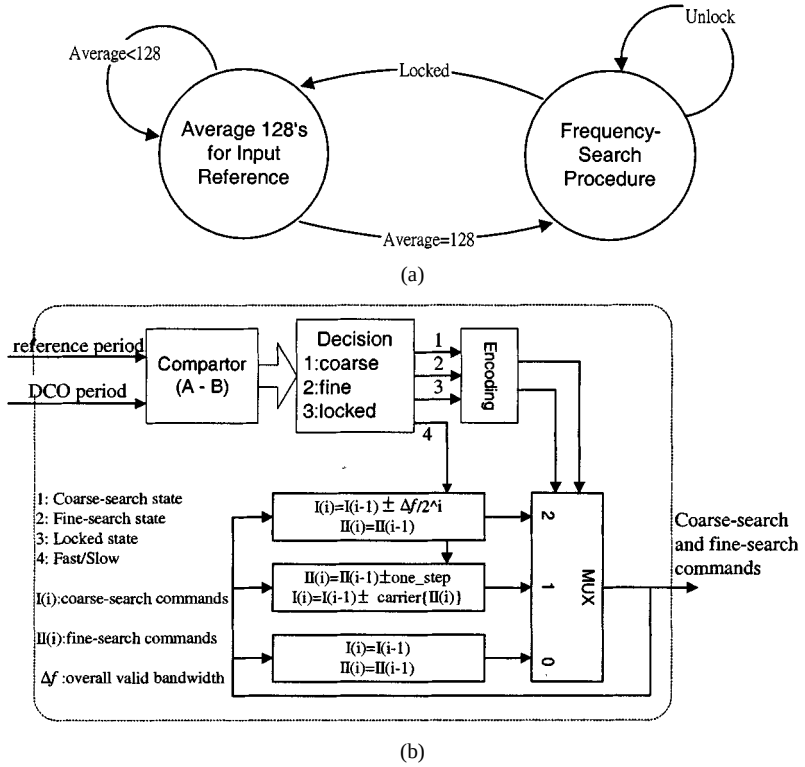


Fig. 4. (a) State diagram of control processes. (b) Structure of frequency-search module.

is to increase lock-in time. The estimating procedure exploits time-division-multiple schemes to share one digital integrator. Because low-power CMOS circuits are required, all modules must be controlled to stop or to run based on controlled status to reduce power dissipation. So, different from traditional approaches, all modules of the control IP are operating at burst mode. For example, the loop divider is always idle during the average procedure for the reference clock.

Physically, a digital integrator contains least-significant-bit (LSB) uncertainties and results in a missing probability of the frequency search. It means that the LSB of quantization may be different in the digital integrator, and then the searching results become error prone. To cope with this problem, it is necessary for frequency-search processing to include a decision threshold to increase the hit rate. The problem of including the decision threshold is the loss of searching accuracy. Trading off both hit rate and accuracy, the size of the threshold must be less than two bits, which are obtained by simulation and measurement. Finally, the complete frequency search includes two thresholds to select and to determine searching algorithms and controlled status, as shown in Fig. 4(b).

Because the control IP is an all-digital approach and can be constructed by HDL, it makes the proposed architecture more portable. Therefore, our proposal is convenient for SOC design to improve turnaround time efficiency.

## IV. Circuit Design

### A. Digital Integrator

In order to realize the algorithm of jitter reduction in Section II-A, a TDC technique is applied to implement a digital integrator. The structure of the digital integrator includes a delay chain, cascaded counter, and encoder, as shown in Fig. 5. The resolution of digital integrators is dependent on the unit delay of th edelay chain, and the maximum integrated period is decided by the length of the counter. In order to measure a signal's period, a delay chain is the kernel of the digital integrator, whose structure is completed by a D-type latch, and all of them are controlled by the input signal. At the beginning, a "1" is sent into the delay chain to monitor its run which likes to measure the distance of a ball rolling at the ground. When "1" runs once, a feedback "0" is sent to the chain again. The above procedure is recycled during operation. Therefore, a two's complement processing is needed to satisfy the unique output condition. The input signal is used as a switch for controlling "1" to run or to stop in the delay chain. If it sets all latches OFF, each bit of digitization can be read from each D-type latch. By this method, we can convert information from time to digital numbers, where the relationship of period and quantization level is linear. In order to handle overflow issues, a flag is designed to indicate out of range in the digital integrator to prevent control IP overlock in wide-band operations.

Because the cascaded counter after delay chain works with most-significant-bit (MSB) transient behavior in the delay chain, to reduce power dissipation and operation frequency, a total length of delay chain must satisfy the speed limitations of the cascaded counter in Fig. 5, whose maximum speed is decided by cell library. The constraint relationship between the delay chain and cascaded counter of digital integrator is formulated as

$$T_{\text{total}} = \sum_{i=0}^{L} T_{\text{latch}(i)} \geq \text{Max.}\{T_{\text{Cascaded Counter}}\}. \quad (5)$$

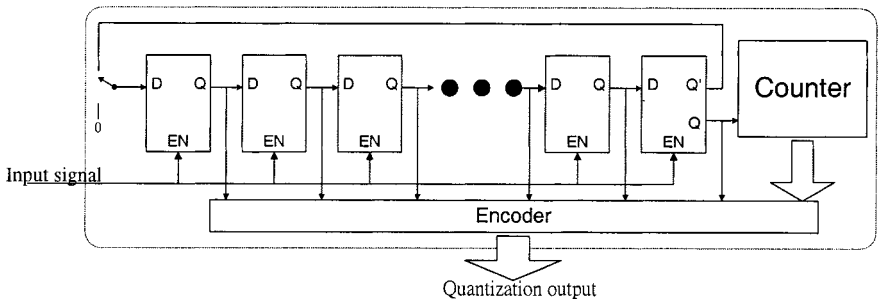


Fig. 5. Structure of D-latch-based digital integrator.

From (5) for 0.6-$\mu$m CMOS cell library, the maximum speed of a 10-bit counter is about 50 MHz, so the total delay of delay chain must be larger than 20 ns. For a long delay requirement, the counter becomes simple and small. Trading off both cost and timing, the length of a delay chain lies within $32 \sim 64$. In addition, its length is selected as $2^m$ due to simple encoder structure. Hence, the maximum frequency is limited by the scale of unit delay (resolution) in the digital integrator, and its minimum frequency is dependent on the length of the counter. The frequency range of the proposed digital integrator with a 6-bit delay chain and 10-bit counter (overall, 16 bits) is from 10 kHz to 20 MHz under 0.5-ns resolution and $< 1\%$ error in 0.6-$\mu$m CMOS single-poly triple-metal (SPTM) standard cells.

### B. Digital-to-Voltage Converter

Because the interfaces of the control IP are digital but the VCO only accepts voltage (analog signal), an interface conversion is needed to handle different I/O structures. An alternative is to implement some analog function blocks via digital design methodology. Though the digital-implemented function block may have less accuracy, it is suitable for some SOC applications. In Fig. 3, the DVC is an important I/O block between a control IP and an analog VCO. By digital methodology, we can reduce the design effort efficiently and easily implement the DVC.

*1) Basic Concept:* It is found that characteristics of inverters are not only a digital cell but also a voltage-to-voltage converter. The concept of an inverter-based DVC is parallel connections of several inverters whose output nodes are connected together, as shown in Fig. 6. Since the input of each inverter (In[0] $\sim$ In[$n-1$]) can be connected to either high or low, the tied output node will be at some voltage level between voltage high and voltage low when the circuit reaches the steady state. If each inverter input is connected together, it can be regarded as a super inverter with large driving capability. The individual input can perform the function of digital-to-voltage conversion. The mathematic derivations are given below.

From the analyses, it is known that the inverter threshold of an inverter is determined by the ratio of the gain factor $k$ of the pMOS and nMOS [10], where $k$ is defined as $k = \mu C_{\rm ox}(W/L)$. Because all inverter inputs can only be either high or low, which means either the pMOS or the nMOS in an inverter is off, and outputs in this DVC are connected together. From the Kirchhoff's current law (KCL) [11], all currents flowing into pMOS have to be equal to that flowing into nMOS. Assume we have $N$ inverters in the simple DVC and $M$ of the inverter inputs are

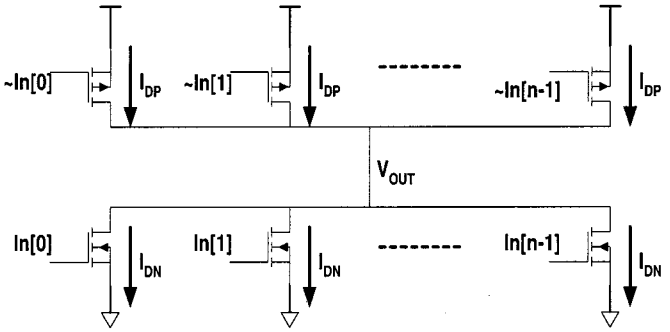


Fig. 6. Basic DVC circuit.

connected to logic high. Thus, $M$ of the nMOS and $N-M$ of the pMOS transistors are turned on and the others are turned off.

$$MI_{\rm DN} = (N-M)I_{\rm DP}. \tag{6}$$

When $V_{\rm out} \geq V_{\rm DD} - V_{\rm TN}$, nMOS is in the saturation region and pMOS is in the linear region. From (6), $V_{\rm out}$ can be solved as follows.

$$V_{\rm out} = |V_{\rm TP}| + \sqrt{(V_{\rm DD} - |V_{\rm TP}|)^2 - \alpha(V_{\rm DD} - V_{\rm TN})^2} \tag{7}$$

where $\alpha$ is the ratio factor and is defined as

$$\alpha \leq \frac{V_{\rm TN}(2V_{\rm DD} - 2|V_{\rm TP}| - V_{\rm TN})}{(V_{\rm DD} - V_{\rm TN})^2}. \tag{8}$$

When $V_{\rm out} \leq |V_{\rm TP}|$, the pMOS transistor is in the saturation region and the nMOS transistor is in the linear region. The situation is very similar to the above, and their results may look much alike and are formulated as

$$V_{\rm out} = V_{\rm DD} - V_{\rm TN} - \sqrt{(V_{\rm DD} - V_{\rm TN})^2 - \frac{1}{\alpha}(V_{\rm DD} - |V_{\rm TP}|)^2} \tag{9}$$

$$\alpha \geq \frac{(V_{\rm DD} - |V_{\rm TP}|)^2}{|V_{\rm TP}|(2V_{\rm DD} - 2V_{\rm TN} - |V_{\rm TP}|)}. \tag{10}$$

When $V_{\rm DD} - V_{\rm TN} > V_{\rm out} > |V_{\rm TP}|$, both pMOS and nMOS transistors are in the linear region. See (11) and (12) at the bottom of the next page.

These equations for evaluating output voltages and their criterions of $\alpha$ are summarized in Table I. To obtain the output voltage at a certain input configuration, we first calculate the value of $\alpha$, and then apply one of these three equations based on the value of $\alpha$. The estimating results using those equations are compared with the simulation results in Fig. 7.

*2) Advanced Structure:* The major drawback of the simple DVC is its nonlinearity. From simulations, it has an output characteristic approximately linear when small variations around the

TABLE I
SUMMARY OF DVC EQUATIONS

| α Criterions | Output Voltage |
|---|---|
| $\alpha \geq \frac{(V_{DD}-\lvert V_{TP}\rvert)^2}{\lvert V_{TP}\rvert(2V_{DD}-2V_{TN}-\lvert V_{TP}\rvert)}$ | $V_{DD}-V_{TN}-\sqrt{(V_{DD}-V_{TN})^2-\frac{1}{\alpha}(V_{DD}-\lvert V_{TP}\rvert)^2}$ |
| $\alpha < \frac{(V_{DD}-\lvert V_{TP}\rvert)^2}{\lvert V_{TP}\rvert(2V_{DD}-2V_{TN}-\lvert V_{TP}\rvert)}$ & $\alpha > \frac{V_{TN}(2V_{DD}-2\lvert V_{TP}\rvert-V_{TN})}{(V_{DD}-V_{TN})^2}$ | $\frac{\alpha(V_{DD}-V_{TN})-\lvert V_{TP}\rvert-\sqrt{[\alpha(V_{DD}-V_{TN})-\lvert V_{TP}\rvert]^2-(\alpha-1)V_{DD}(V_{DD}-2\lvert V_{TP}\rvert)}}{\alpha-1}$ |
| $\alpha \leq \frac{V_{TN}(2V_{DD}-2\lvert V_{TP}\rvert-V_{TN})}{(V_{DD}-V_{TN})^2}$ | $\lvert V_{TP}\rvert+\sqrt{(V_{DD}-\lvert V_{TP}\rvert)^2-\alpha(V_{DD}-V_{TN})^2}$ |

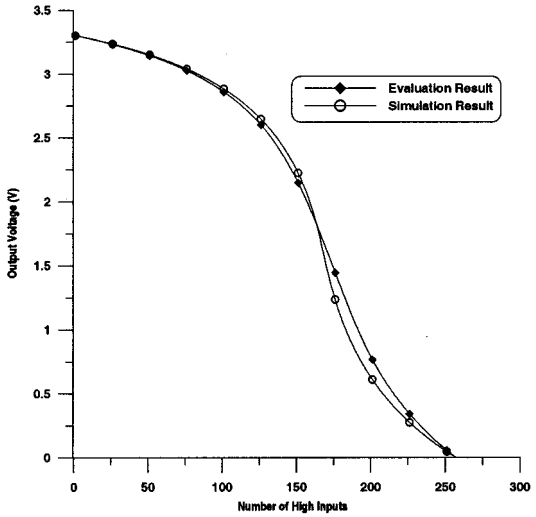


Fig. 7. Comparison between evaluation and simulation results of simple DVC.

operating point are applied to the input. Thus, input words of the DVC are divided into two parts. One part is for the coarse tuning and the other is for fine tuning. The coarse-tuning process is similar to determining the operating point of the DVC and the fine-tuning process is then to make small changes in the input. Once the operating point is determined, the relation between the output voltage and the fine-tuned words becomes almost linear. To achieve the operations described above, tristate inverters are used to make some difference at each input node. There are two types of tristate inverters; one with normal driving capability is used for the coarse tuning and the other with very small driving capability is used for the fine tuning, as shown in Fig. 8(a) and (b). The input pin of each tristate inverter is always connected to the voltage high, and the input of the individual inverter is always connected to the voltage low. The control pin of each tristate inverter now becomes the digital input of the DVC. The structure of the advanced DVC is shown in Fig. 9. There are

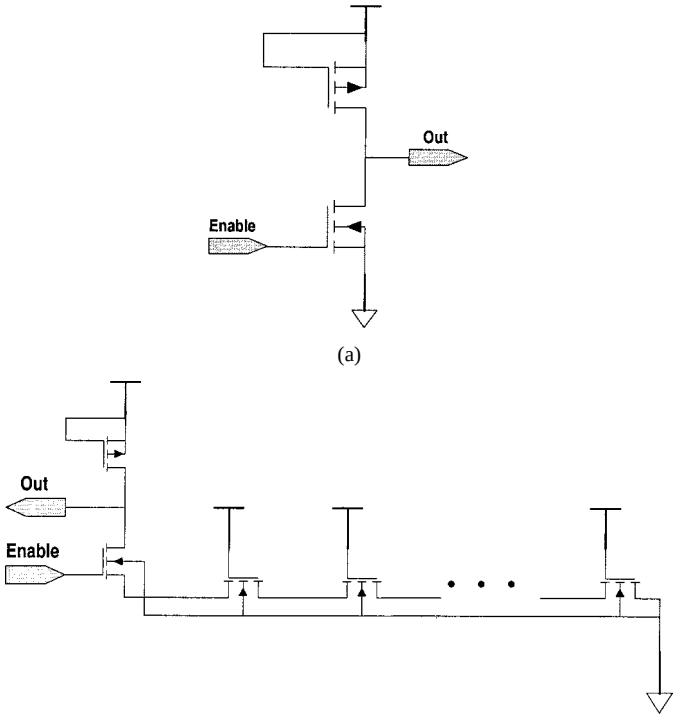


Fig. 8. (a) Tristate inverters for coarse tuning. (b) Tristate inverters for fine tuning.

two groups of input words in this DVC structure. One group is called "Coarse," which is used for the coarse tuning, and the other is called "Fine," which is used for the fine tuning. Because the input of the individual inverter is always connected to ground, the voltage level at the output node will be at voltage high if all the controlling words are off. When one or more of the controlling words are on, the voltage level at the output node will be pulled down toward the ground. The more controlling words are on, the lower the output voltage will be. The output voltage reaches its lowest value, which is determined by the characteristic of the inverter and the tristate inverters, when all of the controlling words, including Coarse and Fine, are on. Since every tristate inverter in each part is the same, the output voltage is not determined by the turned-on order but is determined by the turned-on number. For example, the pattern $100,\ldots,0$ and $010,\ldots,0$ in the coarse tune, as well as the fine tune, will produce the same output voltage. With the modified structure and the controlling scheme, we can greatly improve the linearity of the DVC.

The simulation result of the advanced DVC with 32 coarse-tune inverters and 256 fine-tune ones is shown in Fig. 10, where each line represents each coarse-tune stage and the horizontal axis represents the changes of the fine-tune stage.

$$V_{\text{out}} = \frac{\alpha(V_{\text{DD}}-V_{\text{TN}})-|V_{\text{TP}}|-\sqrt{[\alpha(V_{\text{DD}}-V_{\text{TN}})-|V_{\text{TP}}|]^2-(\alpha-1)V_{\text{DD}}(V_{\text{DD}}-2|V_{\text{TP}}|)}}{\alpha-1} \tag{11}$$

$$\frac{V_{\text{TN}}(2V_{\text{DD}}-2|V_{\text{TP}}|-V_{\text{TN}})}{(V_{\text{DD}}-V_{\text{TN}})^2} < \alpha < \frac{(V_{\text{DD}}-|V_{\text{TP}}|)^2}{|V_{\text{TP}}|(2V_{\text{DD}}-2V_{\text{TN}}-|V_{\text{TP}}|)} \tag{12}$$

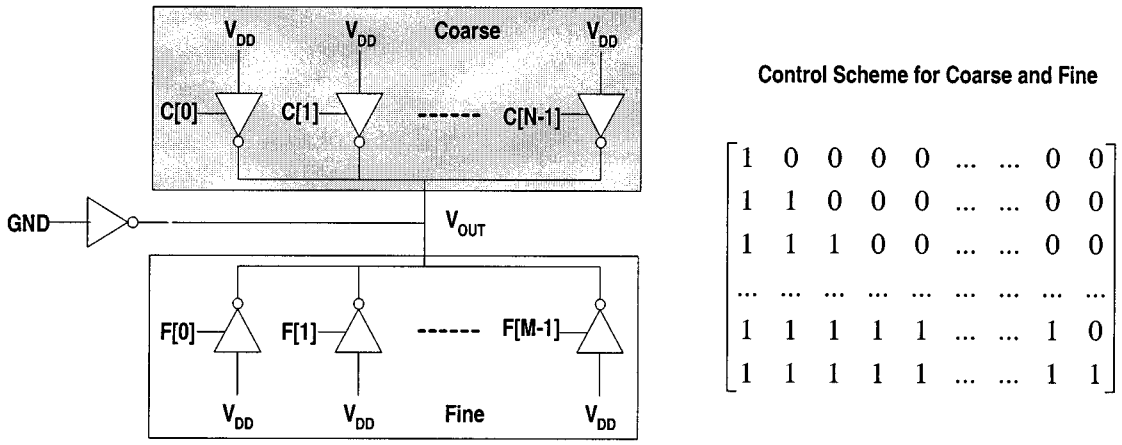


Fig. 9. Structure of advanced DVC and its control schemes.

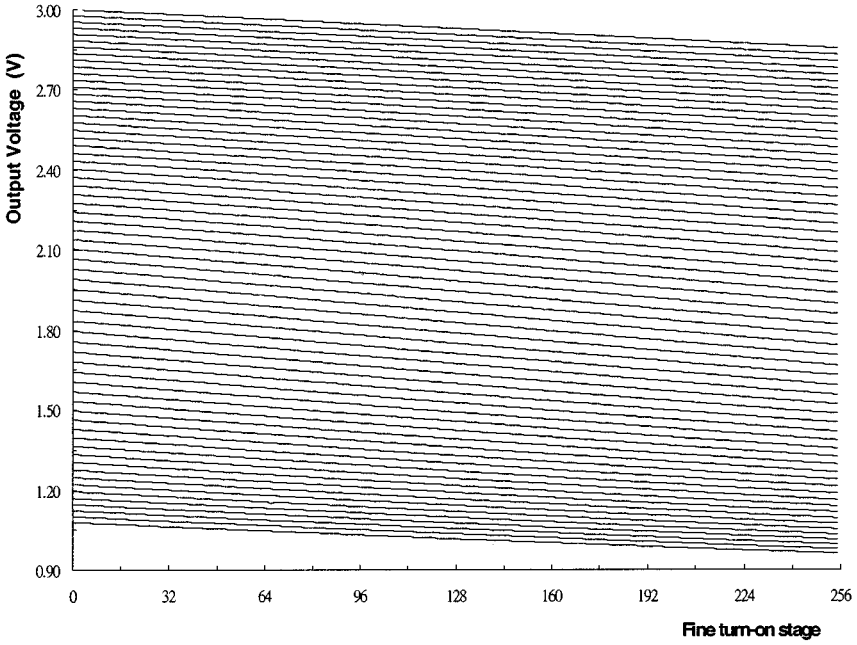


Fig. 10. Simulation result of advanced DVC with 32 coarse and 256 fine stages.

We can see that under each coarse-tuning stage, the relation between the output voltage and the fine-tuning inputs is almost linear. The minimum voltage resolution that the advanced DVC can achieve is about 0.24 mV. The mathematic derivations are analyzed as follows.

Applying KCL in Fig. 9, relations between drain currents of both nMOS and pMOS transistors are obtained.

$$Nk_{n1}\chi_n + Mk_{n2}\chi_n = k_p\chi_p \tag{13}$$

Where $\chi_p$ or $\chi_n$ is the remainder factor except the gain factor $k$ in the drain current equation, either according to the MOS operation region. Rearranging (13) gives the ratio factor for the advanced DVC.

$$\alpha = \frac{Nk_{n1} + Mk_{n2}}{k_p}. \tag{14}$$

Comparison between the simulation and evaluation results, which fixes at a certain coarse-tuning state and changes the fine-tuning stages, is illustrated in Fig. 11. Because the cell-based DVC has no mechanisms against power-supply noise, this structure is sensitive to power-supply noise, which will reduce the DVC resolution. If high voltage resolution is required in applications, a voltage regulator or a separate voltage source is recommended.

### C. Voltage-Controlled Oscillator

In silicon verification, a wide-band VCO is needed, combined with the control IP and DVC, to realize the fully integrated frequency synthesizer. By implementing a VCO similarly with dual-delay [12] and two-stage [13] structure, a wide-band VCO is shown in Fig. 12. In order to keep working conditions of nMOS transistors (from linear to saturate) during oscillation, where those changes create VCO output with large variations, such as dc-level and swing, we use one nMOS transistor M7 connected to the ground and controlling the total current. Its role is like a current mirror to keep all nMOS transistors worked at fixed condition during oscillation. Hence, a tail-current source nMOS transistor, which is commonly used in a conventional emitter-coupled logic (ECL)-like differential

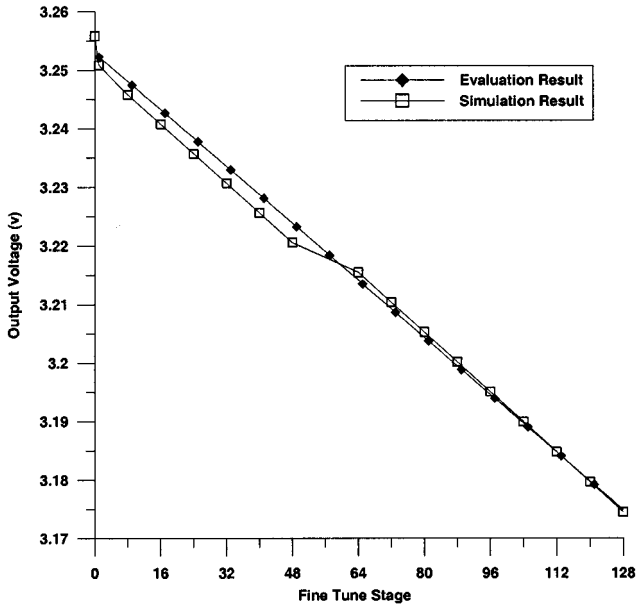


Fig. 11. Comparison between evaluation and simulation results of advanced DVC.

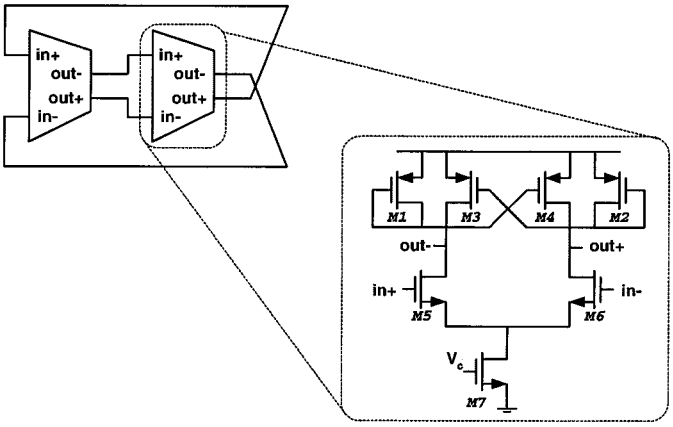


Fig. 12. Structure of a two-stage VCO.

CMOS pair, is avoided to reduce $1/f$ noise. Dual pairs of nMOS load transistors, M1, M2, M3, and M4, are added to the delay cell to constitute a CMOS-like latch. The tuning characteristic of VCOs is shown in Fig. 13. The summary of VCOs is given in Table II.

In order to connect with the control IP, the high frequency of the VCOs must be slowed down to satisfy IP specifications. Most dynamic registers need clk and clk_, and it is necessary to generate differential signals from one signal synchronously. The reason for choosing the true single-phase clock (TSPC)-based register is convenience, but its drawback is that it is too sensitive to input variation. Based on differential delay-cell architecture, the VCO can generate the differential signals at the same time. Therefore, it is possible to choose differential dynamic registers without any extra effort. A high-speed dynamic register proposed in [14], as shown in Fig. 14, used as a divided-2 circuit. The dynamic register consists of a positive latch and a negative latch and is less sensitive to its inputs. The output duty cycle remains around 50%.

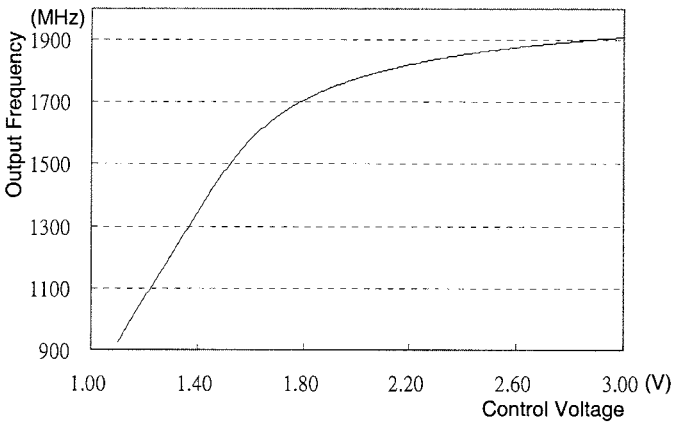


Fig. 13. Tuning characteristics of VCO.

TABLE II
SUMMARY OF PROPOSED VCO

| Items | The proposed VCO |
|---|---|
| Bandwidth | *(824 ~ 2080) MHz* |
| DC-level | *+(1.56 ~ 1.80) V* |
| Voltage Swing | *+(1.96 ~ 2.24) V* |

## V. IMPLEMENTATION AND DISCUSSION

The fully integrated frequency synthesizer is fabricated in 0.6-$\mu$m CMOS SPTM process. First, a control IP is described by Verilog-HDL, where a digital integrator is designed at gate level with timing information from an in-house standard-cell library. The jitter model is used to verify and improve the proposed architecture. Then Verilog source codes are synthesized to generate gate-level netlists and schematics for further simulations and verifications. Compared with gate-level netlists and original codes, their behaviors and timing are checked at this step. In addition, it is also necessary to optimize area and timing. In order to trade off among size, power, complexity, and speed, a factor of power-delay product versus complexity (size) is used to improve physical parameters. This means that a case of low complexity with minimum power dissipation is a proper solution. After verifications, auto place and routing (APR) tools are used to complete the physical designs of the control IP. In order to increase driving strength at higher operating frequency, we use clock-tree distribution to maintain signals.

The full-custom design portion is to draw the DCO layout (both DVC and VCO). Basic cells used in the DCO are drawn first and the DCO is then constructed using these basic cells hierarchically. After all layouts are done, design rule check (DRC) and layout versus schematic (LVS) are performed to verify the layout. Post-layout simulations are also executed by HSPICE. In this phase, parasitic effects are added to the circuit and the results have to meet specifications. In order to complete joint simulation of the whole frequency synthesizer, a mixed-mode simulator is used, however, it requires a lot of computing power and time. By modeling the DCO in Verilog HDL, it is able to simulate and verify the whole frequency synthesizer in less time under HDL level where the iteration cycle is short. If the simulation result is incorrect, we can change configurations and parameters of control IP and redo the simulation in a short period.

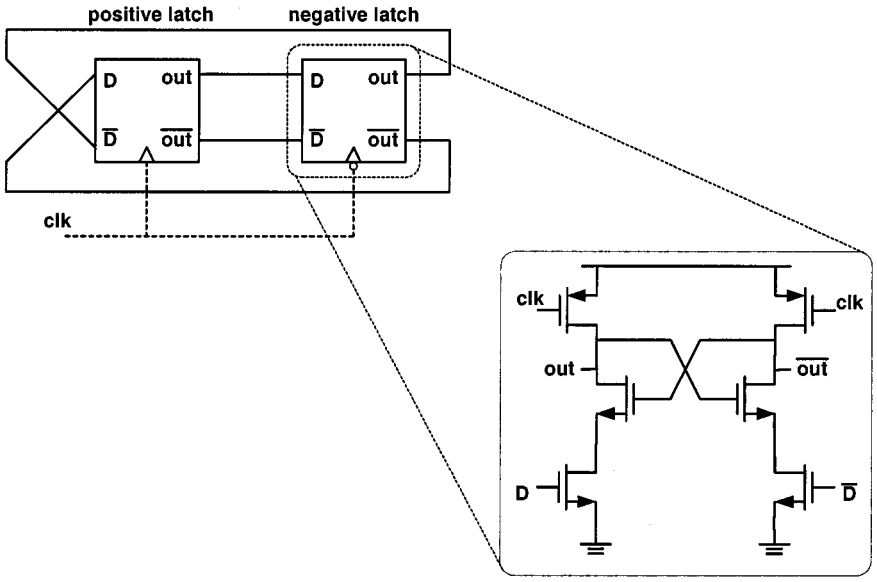


Fig. 14. Dynamic register-based prescaler.

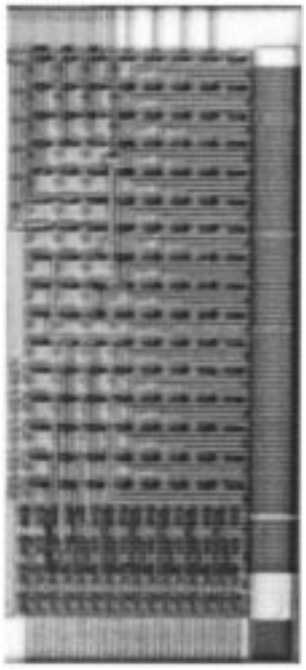

Fig. 15. Microphoto of advanced DVC with 32 coarse and 256 fine stages.

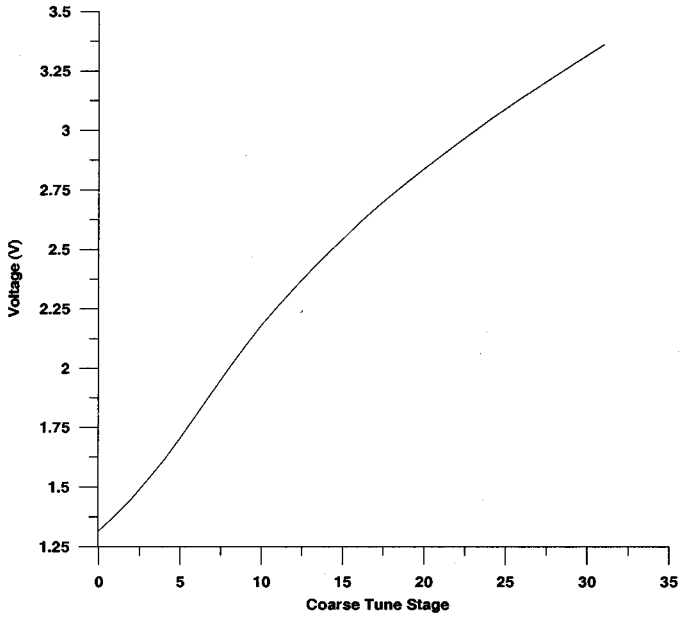


Fig. 16. Measured result of the proposed advanced DVC.

After the simulation results are correct, design flow is split up into the cell-based design and the full-custom design portions.

The proposed DVC structure discussed above provides a low-cost and efficient design to perform the function of digital-to-voltage conversion. Since modules used in the DVC structure are only inverters and tristate inverters, which are very common and various in a cell library, we can construct such a DVC by using cell libraries only. The word length of the coarse tuning is 32 bits and that of the fine tune is 256 bits. The core size of the DVC is 200 $\mu$m $\times$ 475 $\mu$m. The microphoto is shown in Fig. 15. This DVC has an output range from 1.2 to 3.3 V, while the supplied voltage is $+3.3$ V. The output range is to fit the controlling voltage range of the VCO, which is from 1.5 to 3.3 V.

The measurement result shows that the minimum voltage step of the DVC is almost equal to 0.2 mV, as shown in Fig. 16. From post-layout simulations of control IP with $M = 100$ under a 10-MHz reference clock with peak-to-peak jitter $\pm 10$ ns, where the ratio of jitter per period is 20% (peak-to-peak), the jitter of the searching commands for DCO is only 1.13% (peak-to-peak) per period. So, the proposed IP can improve jitter about 24 dB, as shown in Fig. 17. Fig. 18 shows the measured jitter of the reference clock. Measured results show that operating frequency of the proposed frequency synthesizer ranges from 900 to 1900 MHz at 3.3 V, and its working supply voltage range can be $+2.8 \sim 3.7$ V. When jitter of the reference clock is

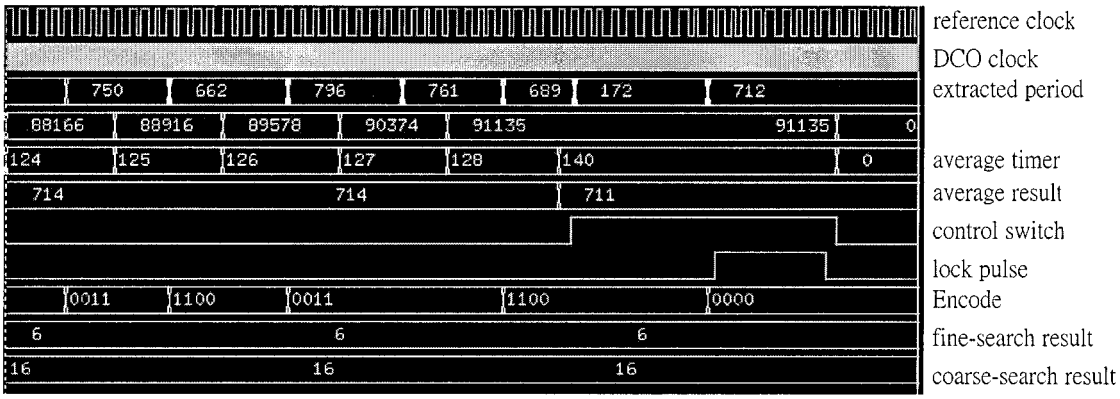


Fig. 17. Post-layout simulation of control IP with 20% reference jitter.

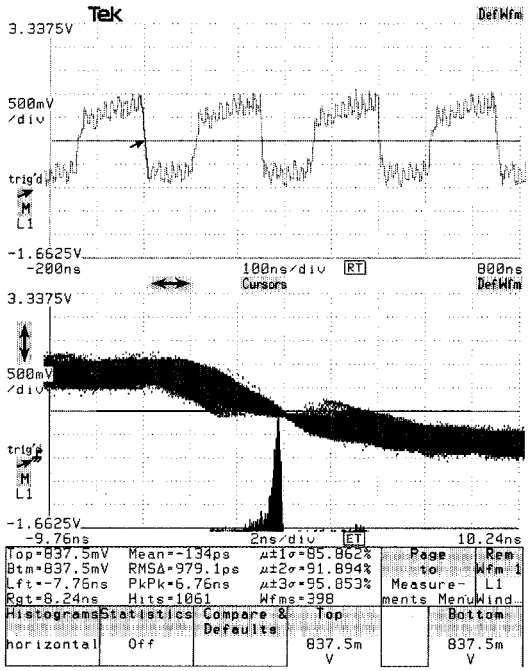


Fig. 18. Histogram of input jitter at 4 MHz.

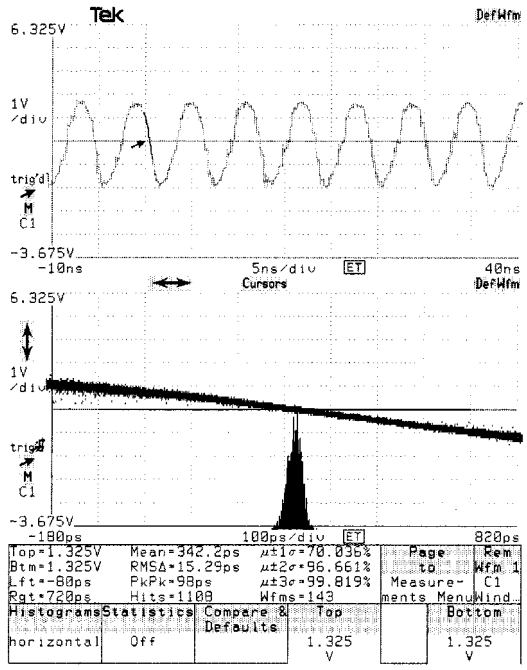


Fig. 19. Histogram of synthesizer output at 1344 MHz, and tested output (1/8) at 168 MHz $\pm$ 49 ps (peak-to-peak) with $N = 1$ and $M = 336$.

4.0 MHz $\pm$ 3.38 ns (peak-to-peak), Fig. 19 shows measured results with $N = 1, M = 336$, synthesizer output at 1344 MHz, and test output (1/8) at 168 MHz $\pm$ 49 ps (peak-to-peak). A measurement of VCO output frequency versus DVC settings is shown in Fig. 20. Frequency spectrums of the proposed frequency synthesizer locked at 900 MHz and 1.98 GHz are shown in Figs. 21 and 22, respectively. From Figs. 21 and 22, the spectrum influenced by the induced noise is about $-46$ dB, where such a degradation is caused by the digital part (control IP) in the proposed design. The comparison with conventional approaches is listed in Table III, where the proposed structure pays a cost of power dissipation to support wide-band operations. The chip microphoto of the proposed frequency synthesizer is shown in Fig. 23, and its summary is listed in Table IV.

In this paper, the proposed controller can be described by a synthesizable HDL code and becomes a soft-IP. A VCO is also modeled by HDL behavioral description to combine with controller IP for HDL-level simulation. Thus, the design cycle for SOC design can be reduced a lot.

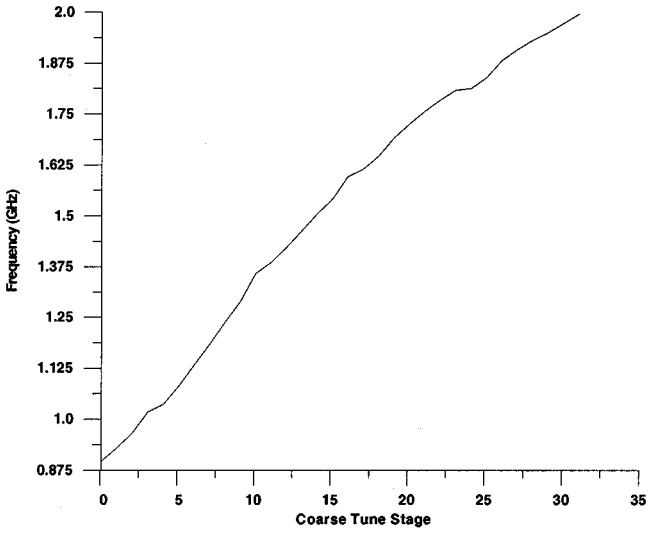


Fig. 20. Measured result of VCO output frequency versus DVC settings.

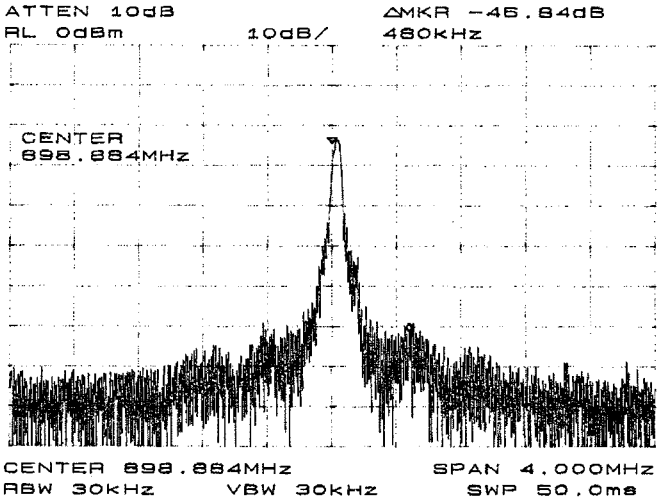


Fig. 21. Spectrum of frequency synthesizer locked at 900 MHz.

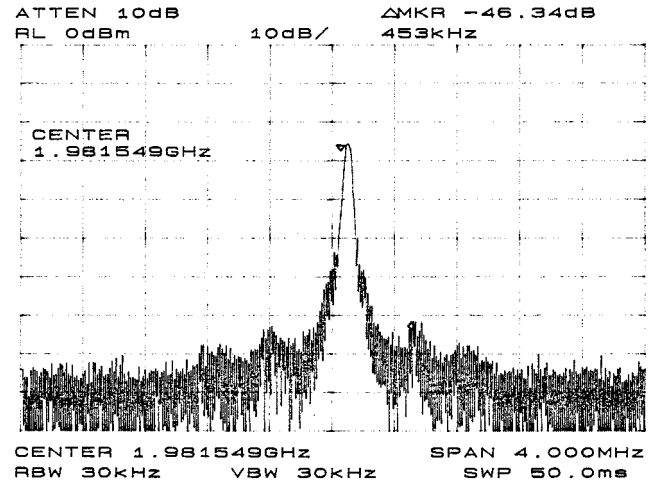


Fig. 22. Spectrum of frequency synthesizer locked at 1.98 GHz.

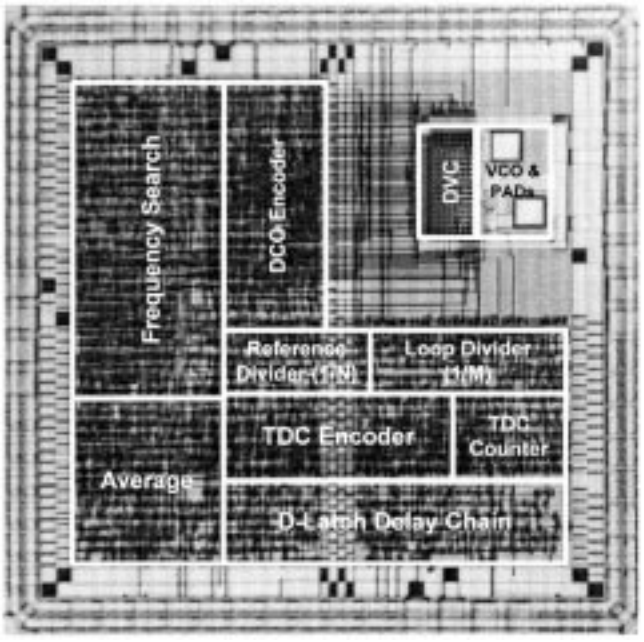


Fig. 23. Chip microphoto of the proposed frequency synthesizer.

TABLE III
COMPARISON WITH CONVENTIONAL ARCHITECTURES

| | Output Range | Structure | Power | Process |
|---|---|---|---|---|
| Ref[15] | (1700~1900)MHz | 4 stages | 60mW@3V | 0.35um |
| Ref[16] | 661MHz~1.27GHz | 2 stages | 15.4mW@2.5V | 0.5um |
| Ref[12] | 750MHz~1.2GHz | 4 stages | 30mW@3V | 0.6um |
| The proposed | 900MHz~1.9GHz | 2 stages | <100mW@3.3V | 0.6um |

TABLE IV
SUMMARY OF CHIP FEATURES

| Items | Specification |
|---|---|
| Technology | TSMC 0.6um SPTM CMOS |
| VLSI Type | Mixed Mode |
| Function | Frequency Synthesizer |
| Loop Bandwidth | Auto-Scan |
| Frequency Range | 865 MHz ~ 1.98 GHz |
| Lock-in Time | $A*O(\log_2 n)+N_2+C < 144$ cycles |
| Reference Clock | 10 KHz ~ 20 MHz |
| DVC Resolution | ~ 0.2mV |
| Pin Counts | 68 (48 signal + 20 power) |
| Power Dissipation (DCO) | ~ 100mW @ 1.9 GHz (with Test Board) |
| Power Dissipation (IP) | <10mW @ 20 MHz (reference) |
| Power Supply | +3.3 V |
| Core Size | 1961 um × 1961 um |

## VI. CONCLUSION

To exploit advances of digital VLSI, a mixed-mode frequency synthesizer with large pulling-in range and low controlled jitter has been presented in this paper. Based on an in-house 0.6-$\mu$m CMOS SPTM standard cell library, the proposed IP, DVC, and VCO has been designed, fabricated, and tested. Results show that the mixed-mode solution provides a clock from 900 to 1900 MHz, which meets the requirements of many high-speed SOCs. The most important is that the design cycle can be greatly reduced, and system turnaround time can be improved during technology migration. As a result, the completely portable control IP and cell-based fully integration CMOS VLSI solution becomes available for SOC applications.

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