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Correlation Between Electrical Characteristics and Oxide/Polysilicon Interface Morphology for Excimer-Laser-Annealed Poly-Si TFTs

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This work investigates the correlation between electrical characteristics and gate-oxide/polysilicon interface morphology for excimer-laser-annealed (ELA) poly-Si thin-film transistors (TFTs). The main feature of ELA poly-Si films is protrusion at grain boundaries that makes the film surface appear very rough. The surface roughness increases with increasing laser energy density and causes degradation of off-current and reliability for the ELA poly-Si TFTs. This degradation of the off-current is attributed to the lower channel resistance due to the increase in crystallinity of the poly-Si layer and the enhancement of localized electric field arising from the protrusions at the grain boundaries. In addition, the increase of localized electric field also degrades device reliability. Passivation of gate oxide/poly-Si channel by NH_3-plasma treatment was found to be favorable in improving the performance and reliability of the ELA poly-Si TFTs.
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Low-temperature processed (LTP) polycrystalline silicon thin-film transistors (poly-Si TFTs) are attracting much attention for use in active matrix liquid crystal displays (AMLCDs) because of their higher field-effect mobility and driving current compared to amorphous silicon TFTs currently used for large-area electronics.[1] Thus, integration of the AMLCD and its peripheral driver circuits on a single glass substrate is of great advantage for the LTP poly-Si TFTs. In order to fabricate LTP poly-Si TFTs on a glass substrate, all of the fabrication processes must be carried out at low temperatures of no more than 600°C.

It is well known that excimer laser annealing (ELA) is a very promising scheme for the crystallization of amorphous silicon because the laser process heats thin silicon films to the melting point on several tens of nanoseconds that allows the films to melt and recrystallize without significantly heating the glass substrate. Moreover, it has been reported that ELA resulted in high-quality polysilicon films with very few intragrain defects, leading to significant improvement in the electrical characteristics of poly-Si TFTs.[2-5] However, during the phase transformation from liquid to solid in the laser crystallization, many protrusions are formed at the oxide/polysilicon interface, causing a very rough surface of polysilicon.[6] The enhanced electric field arising from the asperities at the rough surface led to adverse effects on the electrical characteristics and also created reliability problems in the ELA poly-Si TFTs.[7,8] The surface roughness inherent to the ELA process has been a troublesome problem. In recent years, many investigations have been reported regarding the formation mechanism of protrusions and the reduction scheme of the surface roughness,[5,6,9-11] whereas little study has been made with respect to the correlation between device behavior and interface morphology for the ELA poly-Si TFTs.[12] In this study, correlation between electrical characteristics and oxide/polysilicon interface morphology of the ELA poly-Si TFTs is investigated, in particular, the off-state characteristics and device reliability. In addition, the study also includes the effects of NH_3-plasma treatment on the ELA poly-Si TFTs.

Experimental

Self-aligned top-gated n-channel ELA poly-Si TFTs were fabricated on thermal oxide-covered silicon wafers according to the following procedures. A 110 nm thick low-pressure chemical vapor deposited (LPCVD) amorphous Si layer was first deposited using a SiH_4 process at 550°C. All specimens were then irradiated by KrF excimer laser beam ($\lambda = 248$ nm) with various energy densities at room temperature in a vacuum ambient ($\sim 10^{-3}$ Torr). The excimer laser beam had a pulse duration of 15 ns and a pulse repetition rate of 20 Hz. An optical homogenizer produced a 1.8×23 mm line-shaped profile on the surface of the irradiated specimen. The line-shaped profile scanned the whole surface area of the substrate with a 98% overlap ratio per each laser shot, so that every part on the silicon film was irradiated 50 times by the excimer laser light with the same energy density. After the laser annealing, the silicon film was patterned into individual active device islands, and a 120 nm thick plasma-enhanced chemical vapor deposited (PECVD) tetraethyl orthosilicate (TEOS) oxide was deposited at 300°C to serve as the gate insulator. A second LPCVD poly-Si film was subsequently deposited and patterned using dry reactive ion etching (RIE) to form the gate electrode. Next, the source/drain and gate regions were doped with phosphorus via self-aligned P^+ ion implantation at an energy of 40 keV to a dose of 5×10^{15} cm^{-2}, followed by a thermal annealing at 600°C for 24 h in an N_2 ambient. Then, a 500 nm thick PECVD-TEOS passivation oxide was deposited at 300°C. After the contact holes were opened, metallization of Al electrodes was completed, followed by a sintering process at 400°C for 30 min in an N_2 ambient. For comparison, control samples were also fabricated following the same process except that the ELA was replaced by a solid-phase crystallization (SPC) conducted in a furnace at 600°C for 24 h in an N_2 ambient. In addition, a group of TFTs was subjected to NH_3-plasma hydrogenation at 300°C in a parallel-plate reactor with a power density of 0.7 W/cm^2 in order to investigate the passivation effect of NH_3 plasma on the electrical characteristics of ELA poly-Si TFTs. In this study, all devices investigated have a gate width/length dimension of 50/10 μm.

The images of the oxide/polysilicon interface morphology of the poly-Si TFTs were measured using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The *I-V* characteristics of the fabricated devices were measured using an HP4145B semiconductor parameter analyzer. Various device parameters, including the threshold voltage (V_{TH}), the subthreshold swing (S.S.), the maximum on-current (I_{ON}), and the minimum off-current (I_{OFF}) were measured at a drain voltage of $V_{DS} = 5$ V. The threshold voltage is defined as the gate voltage which yields a drain current (I_{DS}) of 500 nA ($I_{DS} = 100$ nA $\times$ W/L). The field-effect mobility (μ_{FE}) is calculated from the maximum value of the transconductance at $V_{DS} = 0.1$ V. The maximum and minimum values of I_{DS} at $V_{DS} = 5$ V are designated as I_{ON} and I_{OFF}, respectively.

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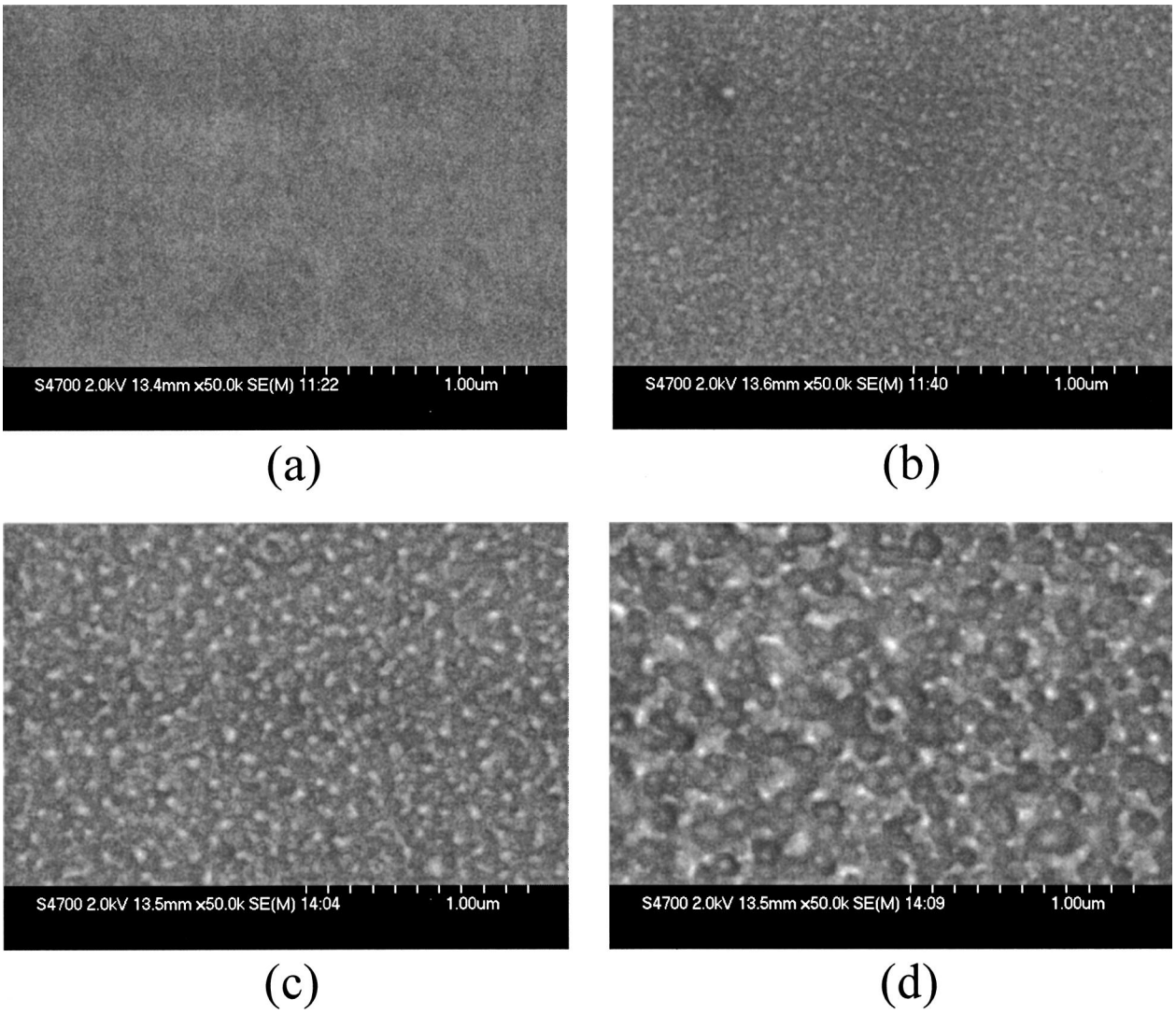

Figure 1. SEM micrographs showing surface morphologies of Si films crystallized by excimer laser irradiation with various energy densities: (a) as-deposited α-Si, (b) 160, (c) 190, and (d) 250 mJ/cm^2.

Results and Discussion

Oxide/polysilicon interface morphology.— Figure 1 illustrates the SEM images of silicon films crystallized by excimer laser irradiation with various energy densities. It can be seen clearly that the larger the irradiated laser energy density is, the higher the localized protrusion is formed, making the film surface rougher. During the laser irradiation on the α-Si layer, significant mass transport occurred toward the grain boundaries due to the very short solidification period of the melted silicon films. The 10% density change between the solid and liquid phases of silicon provides a driving force for the creation of capillary waves, and hence, the solidifying silicon expands and exerts a positive force on the adjacent melt. Thus, during the solidification, grains grow laterally and push the liquid silicon toward the growth direction. In the final stage of solidification, when two growing grains meet to form the grain boundary, protrusion is developed because liquid silicon has a larger density than solid silicon. Where two grains meet to form a grain boundary, a ridge develops. In addition, where three or more grains meet to form a vertex, a hillock may develop.[5,6] Figure 1 shows that surface roughness always accompanies the formation of grain boundaries, forming shallow valleys in the grains and large hillocks at the boundaries. Although the grain boundaries are invisible in Fig. 1, the protrusions are the consequence of the existing grain boundaries, as reported in the literature.

AFM was used to evaluate the surface roughness of silicon films. Figure 2 illustrates the AFM images of poly-Si films obtained by SPC and ELA with various energy densities. The results of AFM are consistent with and complementary to those of SEM. Poly-Si films grown directly by LPCVD usually lead to the formation of tooth-like-shaped grains with valleys appearing at the grain boundaries.[13] This is different from the ELA poly-Si films, where the relative height of hillocks at the boundaries to valleys in the grains causes the asperity of polysilicon surface. Irradiation with low LED resulted in smooth surfaces; however, as the LED increased, the surface roughness also increased due to the ridge and/or hillock formation. Figure 3 shows the root-mean-square (rms) value of surface roughness R_{rms} *vs.* irradiated LED with data of the SPC poly-Si film included for comparison. A change in surface roughness increasing rate is found to occur at LED of 160 mJ/cm^2. This turnaround LED is consistent with the energy density of surface melting (E_{SM}) reported in literature.[5] Below the turnaround LED, the silicon film is almost unmolten during the irradiation, causing only slight change

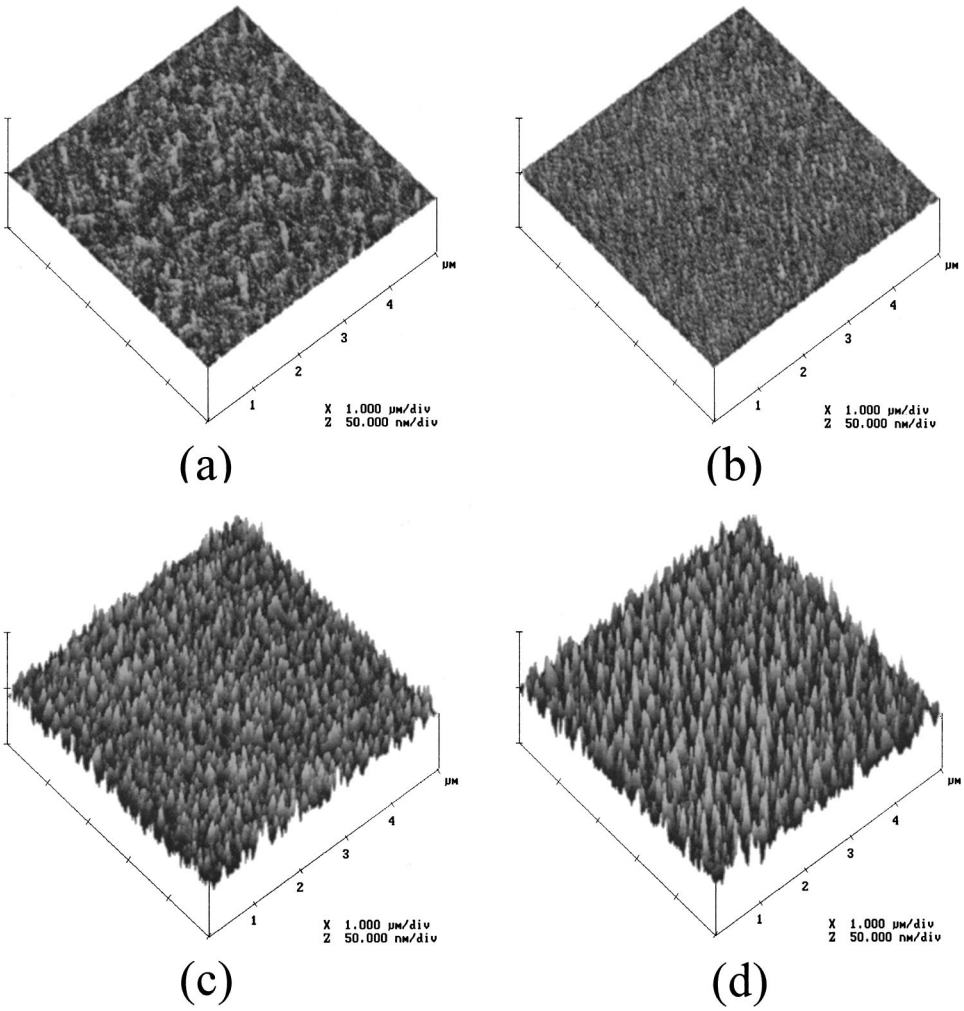

Figure 2. AFM images of Si films crystallized by SPC and ELA with various energy densities: (a) SPC at 600°C for 24 h, (b) ELA with 160 mJ/cm^2, (c) ELA with 190 mJ/cm^2, and (d) ELA with 250 mJ/cm^2.

in surface roughness with LED; however, above the turnaround LED, the silicon film is partially or completely melted, depending on the irradiated LED, and crystallized by the liquid-phase crystallization, resulting in the rapid increase in surface roughness with increasing LED. It was reported that the microstructure of the ELA poly-Si films is clearly stratified with a large-grain layer on the surface and the underlying fine-grain material. The large-grain material corresponds to the crystallization from the molten phase and the underlying fine-grain material corresponds to the explosive crystallization.[14,15] As the LED increases, the melting depth is also increased to result in downward extension of the large-grain region toward the poly-Si/substrate interface, forming even larger grains. At the same time, a larger amount of liquid silicon is pushed toward the grain boundaries as a result of an increase in grain size with increasing LED,[6,14] causing the formation of a higher ridge and/or hillock and thus an increase in surface roughness, as shown in Fig. 3.

Electrical characteristics of ELA poly-Si TFTs.— Figure 4 shows the typical transfer characteristics (I_{DS}-V_{GS}) of the ELA poly-Si TFTs with various (LEDs). It is found that the device characteristics are significantly affected by the irradiated LED. Figure 5 shows the field-effect mobility (μ_{FE}) and the threshold voltage (V_{TH}) *vs.* irradiated LED for the ELA poly-Si TFTs. The μ_{FE} increases with LED while the V_{TH} decreases with LED; this is because an increase in the irradiated LED results in an increase in the grain size, causing a decrease in the number of grain boundaries[16,17] and hence a decreasing trap state density. Figure 6 shows the activation energy (E_a) of drain current *vs.* gate voltage (V_{GS}), measured at V_{DS} = 0.1 V, for

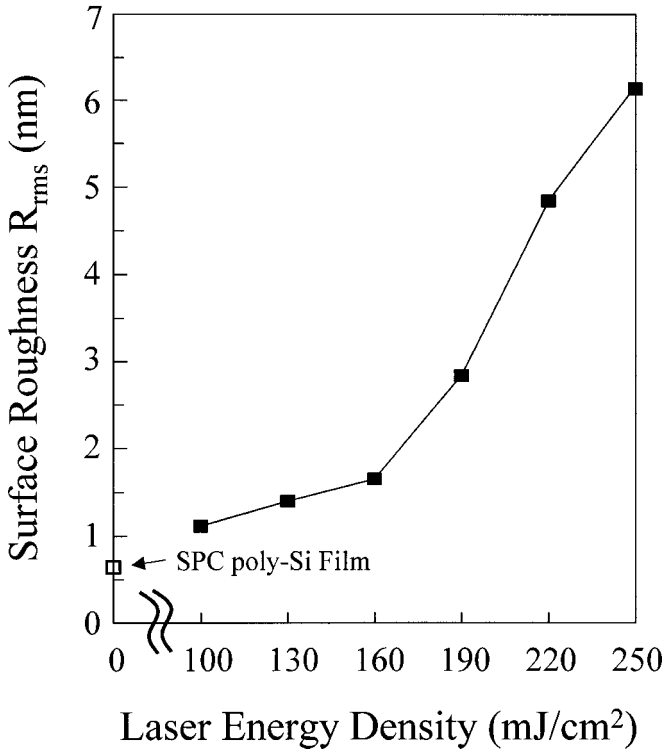

Figure 3. RMS value of surface roughness R_{rms} *vs.* irradiated LED. Data of SPC poly-Si film is included for comparison.

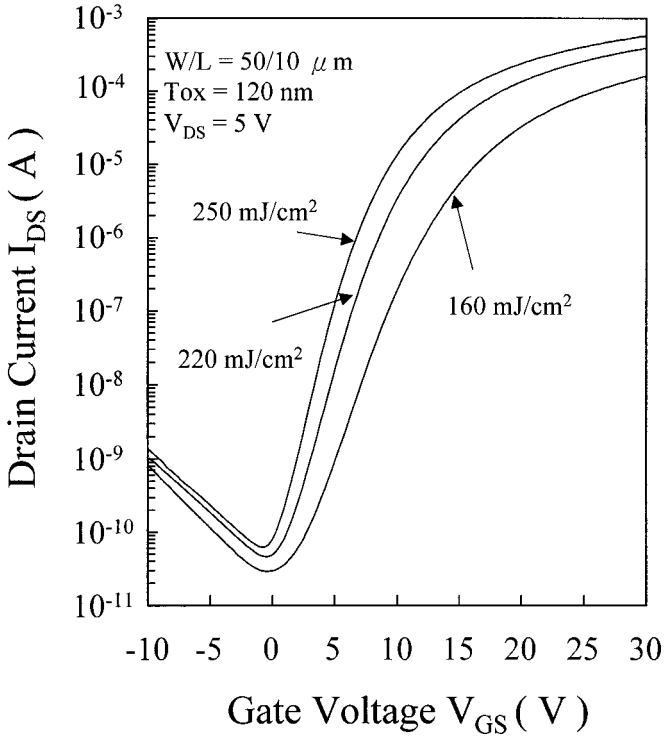

Figure 4. Typical transfer characteristics (I_{DS} − V_{GS}) of ELA Poly-Si TFTs irradiated with various LEDs.

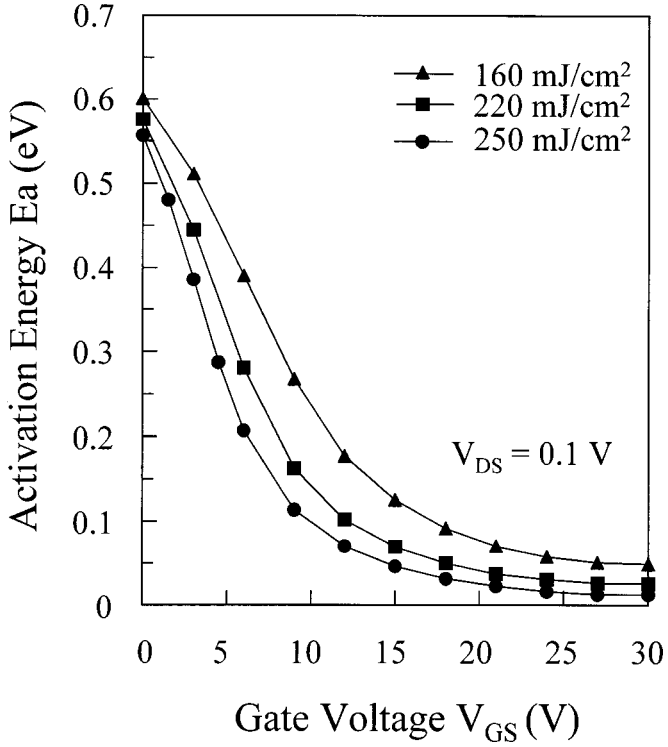

Figure 6. Activation energies (E_a) of drain current *vs.* gate voltage (V_{GS}), measured at V_{DS} = 0.1 V, for the ELA poly-Si TFTs irradiated with different LEDs.

the ELA poly-Si TFTs irradiated with different LEDs. The activation energy of drain current can be derived from the Arrhenius plot of drain current, and the value of E_a reflects the carrier transport barrier of the grain boundary within the poly-Si channel.[18] The lower the E_a is, the lower the carrier transport barrier of the grain boundary will be. A lower transport barrier implies a lower trap state density. Thus, irradiation with a higher LED would result in a lower E_a and hence, lower trap state density, leading to improvement of the device performance, as shown in Fig. 4-6.

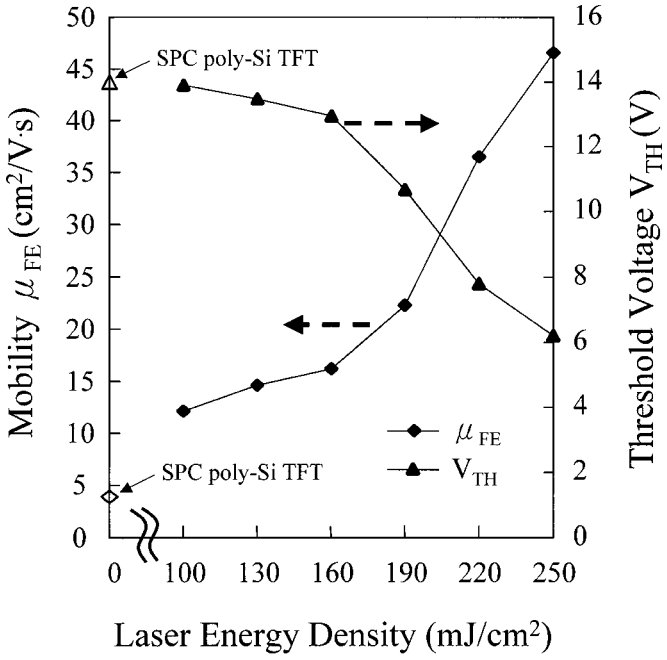

Figure 5. Field-effect mobility (μ_{FE}) and threshold voltage (V_{TH}) *vs.* irradiated LED for the ELA poly-Si TFTs. Data of SPC poly-Si TFT are included for comparison.

The off-current (I_{OFF}) *vs.* irradiated LED for the ELA poly-Si TFTs is illustrated in Fig. 7. It is found that the I_{OFF} increases with increasing LED, similar to two reports in the literature[14,19] but contradictory to another report.[17] It is well known that TFTs with high off-current degrade the contrast ratio of display because of the loss of video information before the frame is being refreshed. Thus, a low off-current is necessary to hold the signal level for an acceptable image quality.[20] Since there is a similar tendency of increasing off-current (I_{OFF}) and surface roughness (R_{rms}) with respect to the increasing LED (Fig. 7 and 3), we presume that some sort of a correlation should exist between the oxide/polysilicon interface morphology and the off-current of the ELA poly-Si TFTs.

It has been reported that the off-current in the LTP poly-Si TFTs is composed of two components: the resistive current in the low-gate-bias region and the junction leakage current in the high-gate-bias region.[21,22] The resistive current is controlled by the channel resistance, which in turn is related to the crystallinity of the poly-Si channel layer. The better the crystallinity of the poly-Si channel layer is, the lower the channel resistance will be. Since roughness of the poly-Si layer increases with increasing LED, we presume that the resistive current also increases with increasing LED, because the increase of surface roughness implies the increasing crystallinity of the poly-Si layer. The junction leakage current is known to be controlled by the emission of trapped carriers in the potential wells at the grain boundaries. In the negative high-gate-bias region, the applied reverse gate bias causes the potential barrier to be so thin that the tunneling of trapped carriers to the conduction band, directly or intermediately via trap states, occurs very frequently. Thus, the junction leakage current is closely correlated with the high reverse gate bias. Since the poly-Si surface roughness increases with increasing LED, the localized electric field will be further enhanced by the poly-Si surface asperity arising from the protrusions at the grain

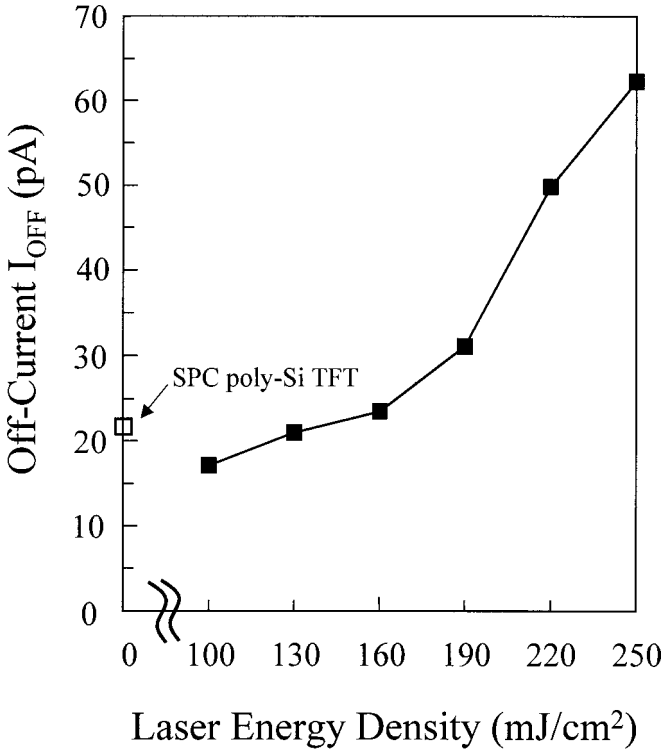

Figure 7. Off-current (I_{OFF}) *vs.* irradiated LED for the ELA poly-Si TFTs. Data of SPC poly-Si TFT is included for comparison.

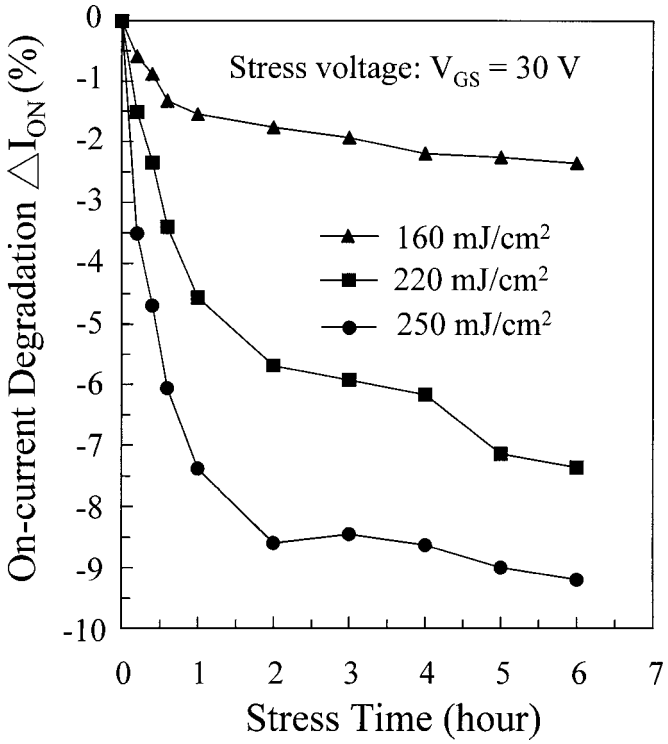

Figure 8. On-current degradation *vs.* stress time under a stress voltage of V_{GS} = 30 V for the ELA poly-Si TFTs irradiated with various LEDs.

boundaries with the increasing LED. As a result, tunneling of trapped carriers to the conduction band is enhanced, leading to the increase of junction leakage current in the high-gate-bias region with increasing LED. This correlation between the oxide/polysilicon interface morphology and the off-current of the ELA poly-Si TFTs clearly explains the observation in this work that both the interface roughness and the off-current increased with increasing LED.

Figure 8 shows the on-current degradation as a function of stress time under a stress voltage of V_{GS} = 30 V for the ELA poly-Si TFTs irradiated with different LEDs. The percent degradation of on-current ΔI_{ON} is defined as $\Delta I_{ON}(\%) = [(I_{ON}$ after stress $- I_{ON}$ before stress$)/I_{ON}$ before stress$] \times 100\%$. It is found that the on-current degradation increased with the stress time; moreover, the degradation increased with increasing LED. With an externally applied gate bias, localized electric field in the oxide is enhanced by the asperity at the oxide/poly-Si interface;[8] this enhanced high electric field may generate electron traps distributed throughout the bulk of the SiO_2.[23] Thus, when a high gate-stressing voltage is applied, electrons are injected from the channel region into the oxide layer and may subsequently be trapped into the oxide electron traps, resulting in the degradation of on-current. Since the poly-Si surface roughness (*i.e.*, asperity) increases with increasing LED, localized electric field in the oxide also increases with increasing LED. As a result, the on-current degradation increases with increasing LED.

Passivation effect of NH_3-plasma.—We have found that increasing LED resulted in an increase of off-current as well as degradation of device reliability. Thus, NH_3-plasma treatment was performed on the ELA poly-Si TFTs to improve the device electrical characteristics. Figure 9 shows the typical transfer characteristics ($I_{DS} - V_{GS}$) of the ELA (with 250 mJ/cm^2 LED) poly-Si TFTs with and without an NH_3-plasma passivation for 3 h. Obvious improvement in device performance was obtained by the NH_3-plasma treatment, in particular, the off-current. This is attributed presumably to the passivation of the trap states at the SiO_2/poly-Si interface and in the poly-Si channel by the dissociated nitrogen and hydrogen radicals.[24] The measured as well as extracted key device parameters are summarized in Table I. It is found that larger improvement in V_{TH} and S.S. was obtained by the NH_3-plasma passivation, while the im-

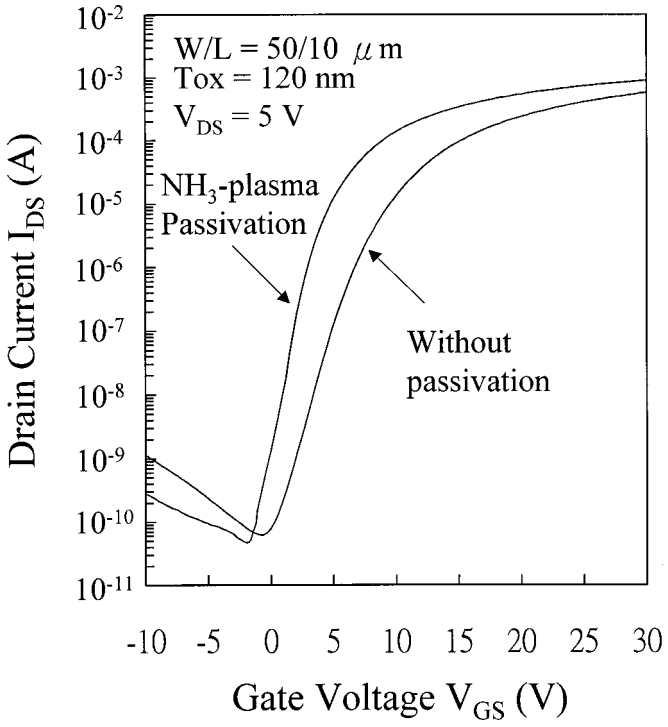

Figure 9. Typical transfer characteristics ($I_{DS} - V_{GS}$) of the ELA (250 mJ/cm^2 LED) poly-Si TFTs with and without an NH_3-plasma passivation for 3 h.

Table I. Comparison of device characteristics for ELA poly-Si TFTs (with 250 mJ/cm^3 excimer laser annealing) with and without NH_3 plasma passivation.

Device parameters	NH_3-plasma passivation	
	With	Without
Threshold voltage, V_{TH} (V)	2.5	6.2
Subthreshold swing, S.S. (V/dec)	0.79	1.39
Field-effect mobility, μ_{FE} (cm^2/V s)	62	46
On/Off current ratio, I_{ON}/I_{OFF}	1.92×10^7	9.12×10^6

provement in μ_{FE} is comparatively smaller. It was reported that the midgap states located at the grain boundaries, which are related closely to V_{TH} and S.S., have a faster response to the hydrogenation, while the intragranular tail states that are related closely to μ_{FE} respond slowly to the hydrogenation.[25] Since the ELA crystallized poly-Si film generally consists of a very low density of intragranular tail states (inside the grains), defects located at the grain boundaries dominate the devices' electrical characteristics. Presumably, the poly-Si channel of the ELA poly-Si TFTs studied in this work still contain a few intragranular tail states, which are closely related to the μ_{FE}; thus, the improvement in μ_{FE} is of a smaller degree compared to that of V_{TH} and S.S. by the NH_3-plasma treatment. Figure 10 shows the on-current degradation as a function of stress time under a stress voltage of V_{GS} = 30 V for the ELA poly-Si TFTs (irradiated with 250 mJ/cm^2 laser energy density), with and without an NH_3-plasma passivation. It is found that the on-current degradation under a high voltage stress was greatly alleviated by the NH_3-plasma passivation. We attribute this improvement to the effect of nitrogen radicals in the oxide. It was reported that there are many strained bonds within the polyoxide, especially at local regions in the vicinity of the grain boundaries.[26] These strained bonds are easily broken by high-energy electrons when a high electric field is applied to the oxide, causing generation of trap states. With an NH_3-plasma treatment, the nitrogen radicals in the oxide may strengthen the strained bonds and passivate the trap states,[27-29] resulting in alleviation of the on-current degradation.

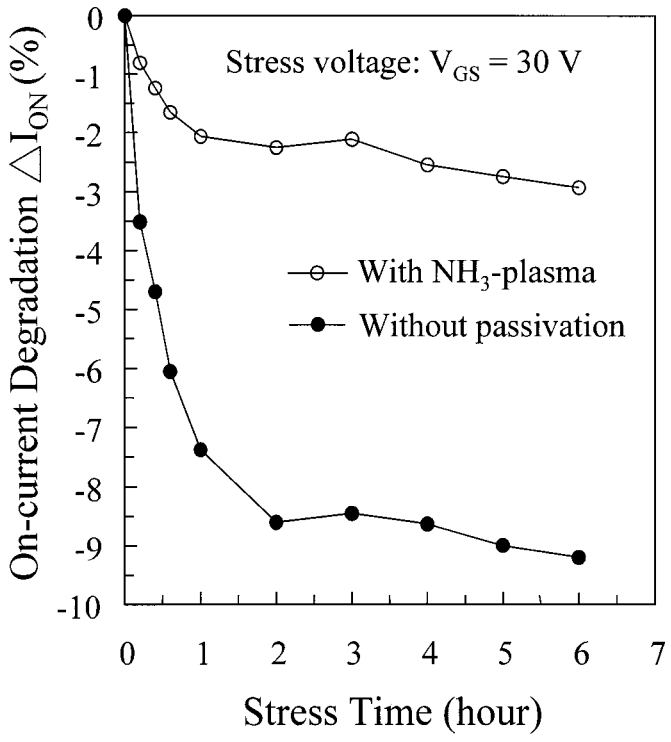

Figure 10. On-current degradation *vs.* stress time under a stress voltage of V_{GS} = 30 V for the ELA poly-Si TFTs (with 250 mJ/cm^2 LED) with and without NH_3-plasma passivation.

Conclusion

The correlation between the electrical characteristics of ELA poly-Si TFTs and the gate-oxide/polysilicon interface morphology was investigated. It is found that both the off-current and the interface roughness of the ELA poly-Si TFTs increased in a similar fashion with increasing LED. The degradation of the off-current, which is composed of a resistive current and a junction leakage current, is closely related to the poly-Si surface roughness. Enhanced protrusions at grain boundaries as a result of increasing LED increase the poly-Si surface roughness and thus the crystallinity of the poly-Si layer, leading to the increase of resistive current at low gate bias. With increasing LED, the asperities arising from the protrusions at grain boundaries also enhance the localized electric field, leading to the enhancement of trapped carrier tunneling to the conduction band, and thus the increasing of junction leakage current at high gate bias. The degradation of the devices on-current (I_{ON}) under a high-voltage stress also deteriorates with increasing LED, because the increasing localized electric field in the oxide enhanced by the asperity at the oxide/poly-Si interface leads to generation of increasing amount of trap states in the oxide. Nevertheless, the device performance and reliability can be significantly improved by NH_3-plasma treatment due to the passivation effect of nitrogen radicals generated in the NH_3 plasma. We believe that the reduction or elimination of oxide/polysilicon interface roughness is of essential importance for the improvement of device performance for the ELA poly-Si TFTs, in particular, the off-current and reliability.

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