PERGAMON

Vacuum 67 (2002) 595–598

VACUUM
SURFACE ENGINEERING, SURFACE INSTRUMENTATION & VACUUM TECHNOLOGY

www.elsevier.com/locate/vacuum

A W-spacer GOLD TFT with high performance and high reliability

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Abstract

In this paper, we successfully fabricated Gate-Overlapped Lightly-doped Drain (GOLD) polycrystalline silicon thin-film transistors (poly-Si TFTs) with selectively deposited spacers. Under appropriate deposition conditions, tungsten (W) films can be selectively deposited on poly-Si gate electrodes to form spacers without any additional etching process. Compared to the conventional poly-Si TFTs without LDD structures, our devices effectively suppress the kink effect and the punch-through phenomenon in short-channel devices. The hot-carrier reliability of our devices is also improved due to the reduced electric field on the drain side. In addition, the transconductance of our devices is compatible to that of conventional devices. This is because the W-spacer acts as a part of gate electrode to induce channel when the device is operated under ON state.

Keywords: LDD; GOLD; Short channel; Kink effect; Selective tungsten (W); Hot-carrier stress; Punch through; Poly-Si TFT

1. Introduction

In recent years, poly-Si TFTs attract great deal of attention since they have better drive ability than amorphous silicon TFTs. However, the anomalous leakage current [1] and the severe kink effect of poly Si TFTs limit their application on active matrix liquid crystal display. To solve these problems, various lightly doped drain (LDD) structures have been devised. Typical LDD structures use offset region or oxide spacer [2] to reduce the drain electric field, but their transconductances (G_m) are also inevitably decreased because the lightly doped/offset regions induce increased series resistance. Accordingly, the gate-overlapped LDD (GOLD) structures that were originally proposed for MOSFETs [3] are applied on poly-Si TFTs [4] to suppress the leakage current and kink effect while retaining high transconductance. In addition, LDD devices with spacer structures are more practical than those with offset regions since the formers avoid misalignment issues and reduce the cost of an additional mask. However, it is found that spacer structures have large gate-induced drain leakage (GIDL) current. This arises from the serious plasma damage generated by the reactive-ion etching (RIE) process [5].

In this paper, we fabricated a novel GOLD structure without using RIE process to form

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0042-207X/02/$ - see front matter
PII: S0042-207X(02)00237-3

spacers. By using tungsten chemical vapor deposition (W-CVD) technology, the spacers were selectively deposited on gate electrode without any additional etching process. Compared to conventional poly-Si TFTs, our devices have compatible transconductance and less pronounced kink effect. The hot-carrier reliability and the punch-through resistance of our devices are also improved.

2. Device structure and fabrication process

A schematic cross-section of the W-spacer poly-Si TFT is shown in Fig. 1. The device was fabricated on 550 nm of buffer oxide that acts as the glass substrate. The 100 nm undoped amorphous-Si channel is grown by low-pressure chemical vapour deposition (LPCVD) by pyrolysis of silane (SiH_4) at 550°C. Furnace annealing then crystallises the amorphous film to poly-Si film with grain size about 500 nm. After active region patterning, the 50 nm gate insulator was deposited in furnace using TEOS and O_2 gases. The 200 nm poly-Si film was then deposited by LPCVD and patterned to be gate electrode. Lightly doped drain (LDD) regions were formed by phosphorous implantation with dosage of 1E13 cm^{-2}. Then, the tungsten (W) spacer was selectively deposited on gate electrode by chemical vapour deposition (CVD) with 20 sccm WF_6 and 6 sccm SiH_4 gases. The process temperature was 300°C, and the process pressure is 0.69 Torr. The W-CVD system we used is ERA-1000 of ULVAC co. 3E15 cm^{-2} of phosphorus was implanted and activated by 20 s rapid thermal annealing (RTA) at 750°C to form self-aligned source and drain. Finally, after 300 nm of TEOS oxide deposition by plasma enhanced CVD (PECVD) and contact hole patterning, 500 nm of Al was evaporated and patterned to form metal pads. Fig. 2 is the SEM micrograph of our W-spacer devices, a conformal W-spacer film is found to enclose the poly Si gate electrode. The thickness of the W film is about 300 nm and can be modulated by different deposition times.

3. Results and discussion

3.1. Suppression of the kink effect

Typical $I_D - V_D$ characteristics of W-spacer LDD poly-Si TFT and conventional poly-Si TFT without LDD structure are compared in Fig. 3. The channel dimensions of these two devices are identical. The kink effect of W-spacer device is less pronounced when compared to the conventional one. It is well known that the kink effect of poly-Si TFTs is related to the impact ionisation effect caused by the high electric field near the drain side. The LDD structure of our devices lowers the

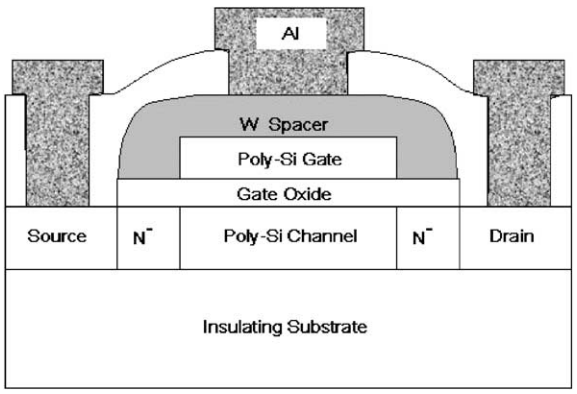

Fig. 1. The schematic cross-section of the W-spacer GOLD poly-Si TFT.

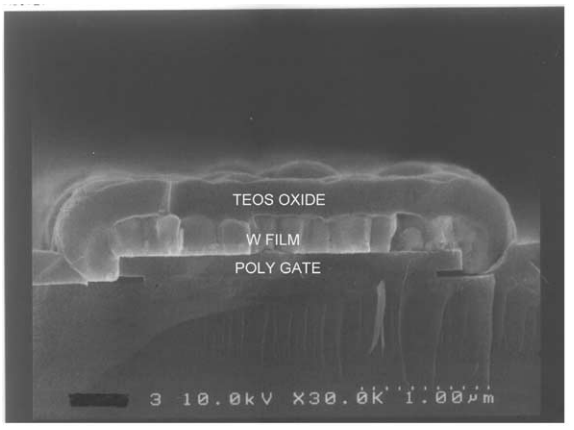

Fig. 2. The SEM micrograph of the poly-Si gate enclosed by W-spacer; thickness of W film is about 300 nm.

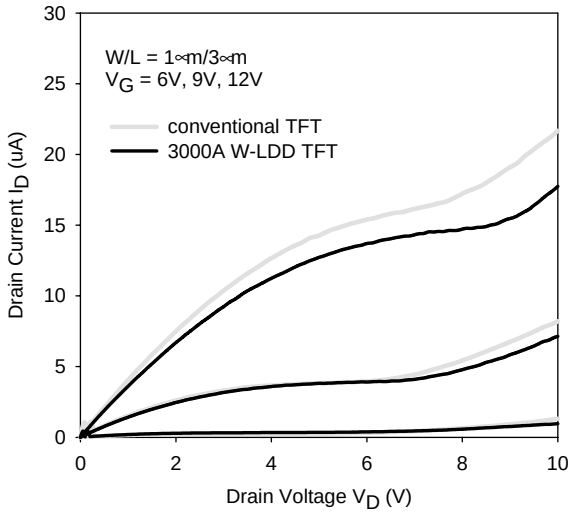

Fig. 3. The typical I_D-V_G characteristics of W-spacer GOLD poly-Si TFT and conventional TFT; the kink effect of W-spacer TFT is suppressed.

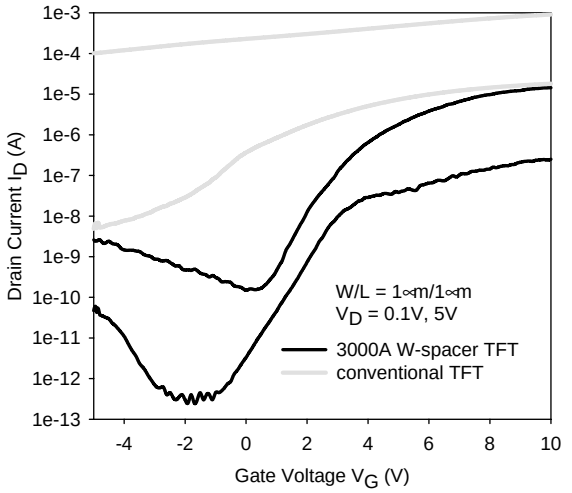

Fig. 4. I_D-V_G characteristics of W-spacer GOLD poly-Si TFT and conventional TFT; the conventional TFT has severe punch-through effect when the channel length is 1 μm.

electric field effectively and therefore suppresses the kink effect. It is also observed that the drive currents of these two devices are compatible. The series resistance in the LDD region does not degrade the performance of W-spacer TFTs. This is because the W-spacer acts as a part of gate electrode to induce channel when the device is operated under the ON state. The transconductance (G_M) of W-spacer TFT is about 60 nS while that of the conventional one is about 90 nS.

3.2. Improvement of immunity to punch-through effect

It has been reported that small dimension TFTs have superior performance such as large drive current and extremely small subthreshold swing [6]. However, punch-through effect also becomes more serious when channel length scaled down. The depletion region of drain side extends more easily to the source and constructs an uncontrollable channel in the body region. Fig. 4 depicts the I_D-V_G characteristics of W-spacer poly-Si TFT and conventional TFT. The conventional TFT reveals serious punch-through effect when the channel length is 1 μm. The W-spacer TFT, on the contrary, retains typical characteristics in short-channel devices. This represents that our structure is suitable for small dimension TFTs.

3.3. Reduction of drain-avalanche hot-carrier (DAHC) degradation

DAHC degradation is a serious problem for n-type short-channel poly-Si TFTs [7,8]. To improve the reliability of short-channel devices, it is necessary to reduce the DAHC degradation. The dependence of threshold voltage degradation on the stress time is depicted in Fig. 5 The W-spacer TFT has higher immunity against the DAHC stress than the conventional device. The reason should result from the suppression of hot-carrier generation due to the reduction of drain electric field described previously.

4. Conclusion

In conclusion, a GOLD poly-Si TFT with selectively grown W-spacer has been fabricated successfully. The device effectively reduces the drain electric filed and therefore suppresses the

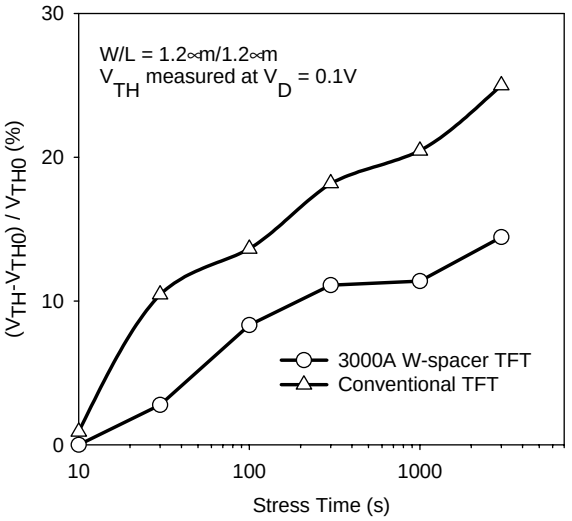

Fig. 5. Comparison of I_D-V_G characteristics of W-spacer TFTs with LDD and offset structures.

related short-channel effects. The hot-carrier reliability is improved and transconductance compatible to the conventional device is also obtained. This structure is also applicable to fabricate small dimension TFTs due to the better immunity to the punch-through effect.

Acknowledgements

The authors would like to thank Mr. J.L. Hsu for his assistance to moderate the process conditions of W-CVD. The authors also thank Mr. C.H. Jan for cross-section SEM support.

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