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Comparison of poly-Si films deposited by UHVCVD and LPCVD and its application for thin film transistors

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Abstract

The ultra-high vacuum chemical vapor deposition (UHVCVD) system can deposit poly-Si film without any laser or furnace annealing. The uniformity of threshold voltage and mobility is superior to that deposited by low-pressure chemical vapor deposition (LPCVD) system. However, due to the deposition in polycrystalline phase for UHVCVD, the film surface is rough and results in low field effect mobility compared to that obtained by LPCVD using disilane (Si_2H_6) in amorphous phase followed by solid phase crystallization (SPC). The on–off current ratio for UHVCVD deposited poly-Si thin film transistors (TFTs) is approximately one order smaller, however, the leakage current for LPCVD SPC TFTs is higher. In this experiment, NH_3 was introduced to both of the two samples to improve the device performance. It can be shown that improvements on device characteristics are more significant for UHVCVD deposited poly-Si TFTs, e.g. threshold voltage decreased dramatically and the on–off current ratio improved by two orders of magnitude. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: poly-Si; TFT; Ultra-high vacuum chemical vapor deposition (UHVCVD); Low-pressure chemical vapor deposition (LPCVD); Solid phase crystallization (SPC); Plasma passivation

1. Introduction

Polycrystalline silicon thin films deposited on SiO_2 surfaces are important materials for microelectronic manufacture. For some specific applications such as the thin film transistors (TFTs) made on glasses, a low-temperature deposition technique is desired. Many methods had been applied to prepare the channel film for fabricating poly-Si TFTs, such as solid phase crystallization (SPC) [1–3], excimer laser annealing (ELA) [4–6], and depositing poly films at reduced pressure without recrystallization [7]. The conventional method used the LPCVD technique to deposit amorphous silicon (a-Si) and then followed by long-term SPC to transform a-Si films to poly-Si films, the SPC process is time consuming (24–48 h), which may affect the throughput and thermal budget of fabrication. Another method used excimer laser to crystallize the a-Si channel film. ELA is a very promising technique for the fabrication of high-performance poly-Si TFTs. However, the deviation of energy within the laser beam causes

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variation of grain size in the poly-Si, and the overlapped area between the beams will degrade the crystallization in the poly-Si film [8].

Recently, it was found that ultra-high vacuum chemical vapor deposition (UHVCVD) can deposit poly-Si film with high quality at lower temperature [9]. This approach deposits poly-Si films at reduced pressures, e.g. <1 m Torr, which is low compared to that of conventional LPCVD (normally >100 m Torr) and leads to fine grain film growth below 550°C without employing further annealing treatments. This finding makes fabrication of low temperature possible, and yields high throughput, low thermal budget. The UHVCVD system features an ultra-clean growth environment (background pressure $\sim 1\times10^{-8}$ Torr). The carbon and oxygen concentrations are below the SIMS detection limit [9]. However, due to the deposition in polycrystalline phase for UHVCVD at reduced pressure, the film surface is rough and higher defect-density at grain boundaries which will degrade the TFT performance. The weakness can be overcome by either enlarging the grain size [10], passivating the defect-state by plasma treatment [11] or smoothing the film surface [9,12,13].

In this work, p-channel poly-Si TFTs were fabricated. The channel films were prepared by LPCVD SPC using Si_2H_6 and UHVCVD without crystallization, respectively. The TFT performance, effective trap-state density and trap-state density in band gap before and after plasma treatment, uniformity, variation of threshold voltage were compared for both LPCVD SPC poly-Si TFTs and UHVCVD deposited poly-Si TFTs.

2. Experimental details

Silicon wafer coated with a 500 nm thick thermal oxide was used as the substrate. Two methods were used to prepare the channel film. (a) 100 nm undoped a-Si film was deposited by LPCVD at 460°C using Si_2H_6 as the depositing source. The deposition pressure is 100 m Torr. The a-Si film was then recrystallized to poly-Si in N_2 ambient for 24 h at 600°C by furnace. (b) 100 nm undpoed poly-Si was grown by UHVCVD at 550°C using SiH_4 as the depositing source. Both of the two samples were then patterned and wet etching to form the active region. The 40 nm gate oxide was grown by Furnace in O_2 ambient at 900°C and followed by 300 nm thick undoped poly-Si deposited by LPCVD at 620°C to serve as the gate electrode. After poly gate was patterned, self-aligned implant (BF_2) was applied to form the p^+ source, drain and gate region. The post-implant annealing was performed in N_2 ambient at 900°C for 30 min to activate the dopant atoms. The 100 nm plasma-enhanced chemical vapor deposition (PECVD) oxide was grown to form as the cap layer. Contact holes were defined. Al was evaporated and patterned followed by a 400°C sintering in N_2 ambient for 30 min. NH_3 plasma treatment was applied in PECVD system for both of the two samples, and the plasma power and temperature was 200 W and 300°C, respectively. The treatment time was 2 h.

3. Results and discussions

Fig. 1 shows the comparisons of typical I_d-V_g curve for both UHVCVD deposited poly-Si TFTs and LPCVD SPC poly-Si TFTs before and after NH_3 plasma treatment, respectively. It can be seen that device performance before treatment is poorer

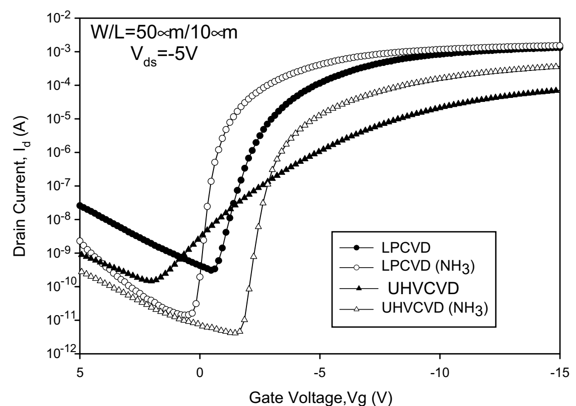

Fig. 1. Comparison of drain current, I_d, versus gate voltage, V_g, for LPCVD SPC poly-Si TFTs' and UHVCVD deposited poly-Si TFTs' before and after NH_3 plasma treatment; both are p-channel devices.

for UHVCVD deposited poly-Si TFTs, i.e. larger threshold voltage (V_{th}) and subthreshold swing (SS), smaller field effect mobility (μ_{EF}) and on–off current ratio, as shown in Table 1. The poorer device performance for UHVCVD deposited poly-Si TFTs is due to more grain boundaries (smaller grain size, i.e. $\sim$80 nm for UHVCVD deposited poly-Si film compared to that, $\sim$1 μm for LPCVD SPC poly-Si film) which result in increased trap-state density, therefore the increased V_{th} as well as larger SS, as shown in Fig. 2 for calculated trap-state density in band gap [14]. The effective trap-state density [15] is also shown in Table 1 which is consistent with Fig. 2. To reduce the trap-state density, the NH_3 plasma treatment was introduced to improve device performance, which can passivate the dangling bonds of poly-Si in grain boundaries and gate oxide interface. Fig. 1 illustrates also the transfer curve after NH_3 treatment for UHVCVD deposited poly-Si TFTs and LPCVD SPC poly-Si TFTs. We can find that device performance improves after plasma treatment, moreover, improvement for UHVCVD deposited poly-Si TFTs is more significant, which can also be verified in Fig. 3. The trap-state density after NH_3 treatment is almost identical for UHVCVD deposited poly-Si TFTs and LPCVD SPC poly-Si TFTs. Table 1 also lists some parameters for both devices. Note that after NH_3 treatment, the on–off current ratio is almost the same ($\sim 10^8$) which is a consequence of decreased trap-state density, but the field effect mobility is, however, still low for UHVCVD deposited poly-Si TFTs. The smaller mobility is attributed to the rougher surface obtained by as-deposited poly-Si in UHVCVD system. Fig. 4 show the atomic force

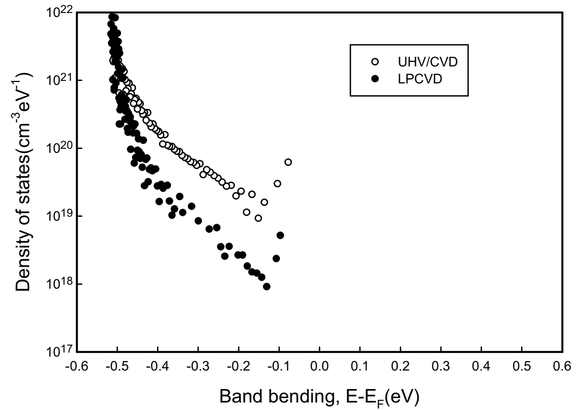

Fig. 2. The density of states in band gap of p-channel device for UHVCVD deposited poly-Si TFT and LPCVD SPC poly-Si TFT.

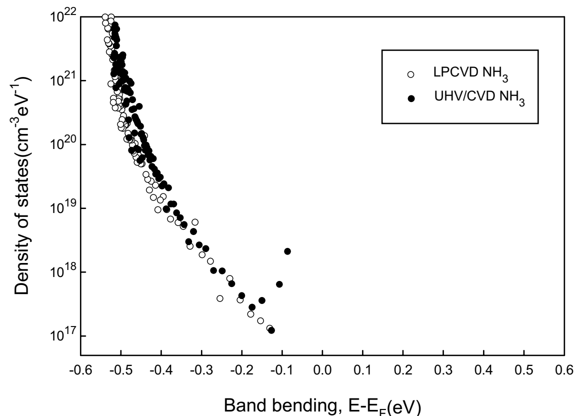

Fig. 3. Comparison of trap-state density after plasma treatment for UHVCVD deposited poly-Si TFT and LPCVD SPC poly-Si TFT.

Table 1
Comparison of poly-Si TFT parameters for LPCVD SPC TFT and UHVCVD deposited poly-Si films before and after plasma treatment

Poly-Si film by	μ_{EF} (cm^2/V s)	SS (V/decade)	N_t ($\times 10^{12}$ cm^{-2})	I_{min} (pA)	V_{th} (V)	On/off current ratio
LPCVD	78.8	0.39	3.7	306	−2.86	4.30×10^6
LPCVD (NH_3)	106	0.16	2.1	14	−1.07	1.08×10^8
UHVCVD	5.0	1.55	9.4	145	−6.28	5.51×10^5
UHVCVD (NH_3)	25	0.31	3.0	4.1	−1.16	1.37×10^8

All values are evaluated at $V_d = -0.5$ V except the trap-state density (N_t) and on ($V_g = -15$ V)/off (I_{min}) current ratio are determined at $V_d = -0.1$ and -5 V, respectively.

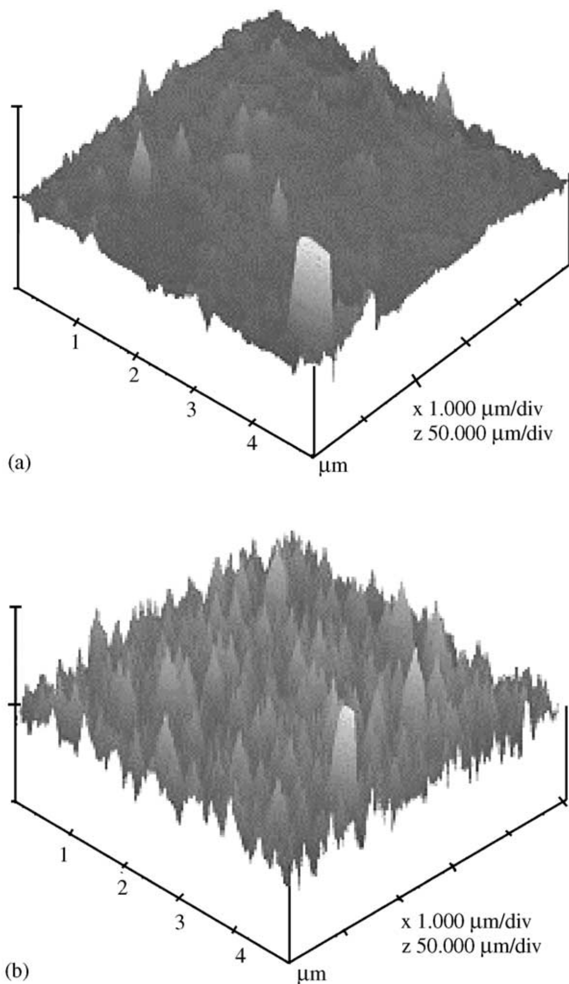

Fig. 4. The surface morphology of (a) LPCVD SPC poly-Si film and (b) UHVCVD deposited poly-Si film, which have the average roughness of (a) 1.7 nm and (b) 3.5 nm observed by atomic force microscope.

microscope (AFM) pictures for UHVCVD grown poly-Si film and LPCVD SPC poly-Si film, it can be seen that the as-deposited UHVCVD grown poly-Si has larger mean roughness (3.5 nm) than that of LPCVD SPC poly-Si film (1.7 nm). Another benefit for UHVCVD deposited poly-Si is the uniformity consideration. Fig 5 shows the variation of field effect mobility and threshold voltage over the wafer for UHVCVD deposited poly-Si TFTs and LPCVD SPC TFTs. The two parameters were measured over the entire 3 in wafer for 21 points uniformly distributed. We can

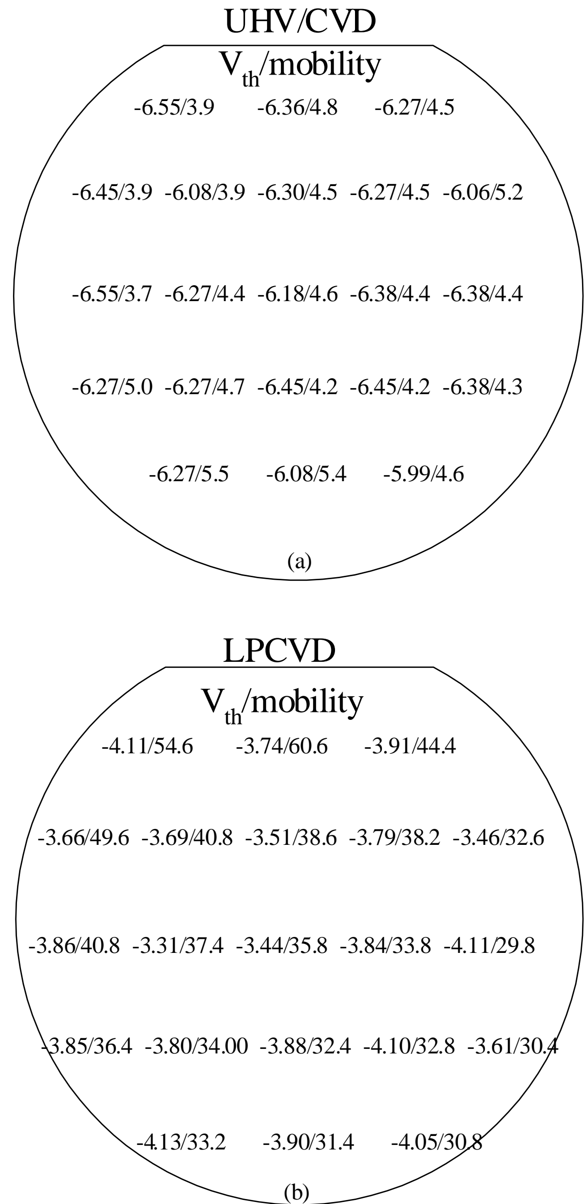

Fig. 5. (a) Uniformity of UHVCVD deposited poly-Si TFT with $V_{th} = -6.29 \pm 0.16$ V and mobility = 4.51 ± 0.47 cm^2/V s ($\pm 10\%$). (b) Uniformity of LPCVD SPC poly-Si TFT with $V_{th} = -3.79 \pm 0.23$ V and mobility = 38.01 ± 8.21 cm^2/V s ($\pm 21\%$).

see that uniformity of UHVCVD deposited poly-Si TFTs ($V_{th} = -6.29 \pm 0.16$ V, $U = 4.51 \pm 0.47$, 10%) is better than that of LPCVD SPC TFTs ($V_{th} = -3.79 \pm 0.23$ V, $U = 38.01 \pm 8.21$, 21%).

4. Conclusion

In this work, it has been shown that UHVCVD deposited poly-Si TFTs after plasma treatment have almost the same trap-state density as well as threshold voltage (~ -1.1 V) and on/off current ratio (10^8) as the LPCVD SPC poly-Si TFTs. Moreover, UHVCVD deposited poly-Si film does not need long time recrystallization, and the uniformity is better than that of LPCVD SPC poly-Si film. However, the mobility of UHV/CVD deposited poly-Si TFT after plasma treatment is still smaller compared with LPCVD SPC poly-Si TFT. This is due to the rough surface in the poly-Si film deposited by UHVCVD, and it can be solved if chemical mechanical polish (CMP) is used, which may help improve device characteristics for UHVCVD deposited poly-Si TFTs.

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