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Simultaneous etching of polysilicon materials with different doping types by low-damage transformer-coupled plasma technique

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Abstract

The feasibility of simultaneously etching n^+, p^+, and undoped polysilicon (poly-Si) materials by a commercial transformer coupled plasma (TCP) reactor has been investigated in this study. Response surface methodology (RSM) was used to optimize process parameters including pressure, TCP source power, bias power, and Cl_2/HBr flow on the main etch step. Quantitative relationships between etching performance and process parameters were established. Our results indicate that there exists a process parameter window that meets the requirements of etching polysilicon with different doping types simultaneously. High etch rate, superior uniformity, good end point detection (EPD) characteristics and profile control can be simultaneously obtained with the optimized recipe, irrespective of the doping types. Furthermore, only minor plasma-induced damage is detected as monitored from antenna transistors' charge-to-breakdown (Q_{bd}), threshold voltage and charge pumping current.

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Keywords: Response surface methodology; Plasma etching; Transformer coupled plasma; Doping type; Plasma-induced damage

1. Introduction

As the complementary metal-oxide-semiconductor (CMOS) device's feature size is scaled down to

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0.25 μm and beyond, buried-channel p-type transistors become more and more difficult to optimize due to aggravated short channel effects inherent in buried-channel devices. In light of this, dual polysilicon gate structure (i.e. n^+ polysilicon and p^+ polysilicon electrodes for achieving 'surface-channel' NMOS and PMOS, respectively) has been proposed for improving short-channel effects. Typical process flow in a 'dual-poly' process is to deposit and define undoped poly-Si gates first. Doping of n^+ and p^+ gate regions are then carried out later using separate lithographic steps, resulting in a complicated process flow for CMOS device integration. In addition, boron penetration and poly-Si depletion effects impose serious constraints on device integration, such as the shrinkage of available process window, as well as mismatch in process window between NMOS and PMOS.

One method to alleviate these restrictions is to dope the n^+ and p^+ poly-Si with a low temperature process (e.g. CVD in-situ doping method) [1] prior to gate patterning. For some specific applications, etching of n^+ and undoped poly-Si simultaneously was also proposed [2]. In these situations, one main challenge is to develop an etch recipe which is capable of anisotropically and uniformly etching poly-Si gate layers of different doping types with good profile control and low plasma-induced damage.

However, it has been documented that the etch rate of n^+ poly-Si is generally higher than that of undoped poly-Si, which is in turn higher than that of p^+ poly-Si with traditional RIE etching techniques [3,4]. But some studies have indicated that the etch rates for poly-Si materials of different doping types may be adjusted to the same level using high density plasma (HDP) technique (e.g. ECR and MORI source) [1,2]. In this study, we investigated the feasibility of simultaneous etching with different doping types using a popular commercial HDP plasma reactor (i.e. LAM TCP 9400SE). The parameters and responses to be considered are quite complex, thus an appropriate experimental strategy is needed to handle the experiments efficiently. RSM is a combination of mathematical and statistical techniques that is useful for the modeling and analysis of problems in which a response of interest is influenced by several variables, and the objective is to optimize this response [5]. It is economical for characterizing a complicated process. Moreover, it requires fewer experiments in order to study all levels of all input parameters, and filters out some effects due to statistical variation [5–12].

In this study, RSM was thus used to investigate and optimize process parameters including pressure, TCP source power, bias power, and Cl_2/HBr flow of the main etch step.

Another major issue that needs to be addressed in gate etching is the plasma process-induced damage. During plasma etching, severe charging of the gate electrode may occur. When this happens, a high electric field could develop in the underlying gate oxide, resulting in the degradation of gate oxide integrity [13,14]. In the meantime, the gate oxide at the gate edge is exposed to the plasma environment and bombarded by the energetic ions or photons [15]. These damage effects should be carefully treated and minimized. In this work, attention is also paid to this issue by characterizing the performance of the fabricated devices.

2. Experimental

A commercial high-density plasma etcher (i.e. LAM TCP 9400SE) was used for this study. Undoped poly-Si layers with two thickness (i.e. 4000 or 2000 Å) were deposited on thermally grown

oxide (i.e. 1000 or 40 Å) in a low pressure chemical vapor deposition (LPCVD) system. They were used for both etch rate measurement (i.e. with 4000 Å poly/1000 Å oxide) and profile characterization (i.e. with 2000 Å poly/40 Å oxide). Separate photo resist masking steps were used for BF_2^+ and As^+ ion implantations with dosage of 5×10^{15} cm^{-2} in order to form polysilicon regions with p^+ and n^+ doping types on the same 6-inch Si wafer. Afterwards, wafers were annealed at 1050 °C for 20 s to activate the dopants. Gate resist patterns were then defined, followed by poly-Si gate etching. All samples received a forming gas annealed at 400 °C for 20 min prior to probing.

In this study, we optimized the main etch step using RSM experiment design. Four process parameters were investigated here, i.e. pressure (6–14 mTorr), TCP source power (250–450 W), bias power (100–200 W), and Cl_2/HBr flow (Cl_2: 0–80, HBr + Cl_2 = 160 sccm). A total of 27 runs were included (i.e. 24 test conditions and three center points). Table 1 summarizes the process parameters and the variable factor ranges.

Both test transistors and capacitors were fabricated on 6-inch Si wafers with LOCOS (local oxidation of Si) isolation. Edge-intensive poly-gate antenna structures were used for monitoring the

Table 1
Run conditions for the RSM experiment

Standard order	Run order	Pressure (mTorr)	TCP (W)	Bias (W)	Cl_2 (sccm)
1	18	6	250	150	40
2	2	14	250	150	40
3	20	6	450	150	40
4	15	14	450	150	40
5	23	10	350	100	0
6	4	10	350	200	0
7	3	10	350	100	80
8	8	10	350	200	80
9	12	6	350	100	40
10	7	14	350	100	40
11	24	6	350	200	40
12	19	14	350	200	40
13	10	10	250	150	0
14	22	10	450	150	0
15	13	10	250	150	80
16	9	10	450	150	80
17	17	6	350	150	0
18	5	14	350	150	0
19	26	6	350	150	80
20	11	14	350	150	80
21	16	10	250	100	40
22	6	10	450	100	40
23	25	10	250	200	40
24	21	10	450	200	40
25	1	10	350	150	40
26	14	10	350	150	40
27	27	10	350	150	40

plasma-induced damage in the TCP poly-Si etcher. Electrical measurements were carried out with HP4156 parameter analyzer and HP8110 pulse generator.

3. Results and discussion

3.1. Parameters optimization

Measured responses were used to develop quadratic models for etch rate, uniformity, polysilicon/oxide and polysilicon/photoresist selectivity. The etch rate and uniformity of different doping types of polysilicon were studied. The general form for the model is [5,11,12]

$$Y = b_0 + \sum_{i=1}^{n} b_i X_i + \sum_{i=1}^{n} b_{ii} X_i^2 + \sum_{i=1}^{n-1} \sum_{j=2, j>i}^{n} b_{ij} X_i X_j \quad (1)$$

where X_i are the process parameters, n is the number of the factors (i.e. four in this study, i.e. pressure P, TCP source power T, bias power B, and Cl_2 content C), and Y is the response. For a full quadratic model with four factors, there are 15 coefficients.

The models for all responses are presented in Table 2. For example, the etch rate of undoped polysilicon can be modified by the following equation:

$$\begin{aligned} ER = 2572.67 + 0.67P + 439.67T + 179.42B + 446.08C - 109.75P^2 - 28.00T^2 - 43.12B^2 \\ + 6.88C^2 + 58.25PT + 78.50PT - 46.75PC + 38.50TB + 38.75TC + 77.25BC \end{aligned} \quad (2)$$

Table 2
Summary of model coefficients (Eq. (1)) and adjusted R^2 (accuracy of model fit) for the responses

Model coefficient	Term	Undoped poly-Si etch rate (Å/min)	Undoped poly-Si uniformity (%)	Undoped poly/SiO_2 selectivity (a.u.)	Undoped poly/PR selectivity (a.u.)	N^+ poly-Si etch rate (Å/min)	N^+ poly-Si uniformity (%)	P^+ poly-Si etch rate (Å/min)	P^+ poly-Si uniformity (%)
b_0	Const.	2572.67	1.60333	8.75900	2.23267	2633.33	1.67667	2469.00	1.56000
b_1	P	0.67	−0.34583	1.64267	0.20458	−0.17	−0.34917	−20.33	−0.46417
b_2	T	439.67	0.32583	−1.06050	−0.15042	455.83	0.32833	408.42	0.42417
b_3	B	179.42	0.13583	−1.42058	−0.33808	190.67	0.13167	212.75	0.23667
b_4	C	446.08	−0.61917	−1.41892	−1.77108	483.67	−0.58917	424.50	−0.57333
b_{11}	P^2	−109.75	0.09917	−0.19712	−0.07542	−103.21	0.05167	−103.29	0.11125
b_{22}	T^2	−28.00	−0.01583	0.28337	0.06283	−39.46	0.03792	−62.67	−0.00625
b_{33}	B^2	−43.12	−0.12083	0.16600	0.17108	−59.96	−0.12708	−60.17	−0.00000
b_{44}	C^2	6.88	0.06667	0.10000	0.76408	19.04	0.04167	−1.29	0.19500
b_{12}	$P*T$	58.25	−0.02500	−0.34200	−0.03325	73.50	−0.02750	65.50	−0.05750
b_{13}	$P*B$	78.50	0.06750	−0.19275	0.05700	−13.25	0.17500	−19.00	0.06500
b_{14}	$P*C$	−46.75	0.02500	−0.72825	−0.37100	−61.75	0.08000	−62.50	−0.03000
b_{23}	$T*B$	38.50	−0.05250	0.08225	−0.02175	25.50	−0.12250	33.75	0.07750
b_{24}	$T*C$	38.75	−0.08500	0.06175	0.16275	82.50	−0.12000	44.00	−0.20250
b_{34}	$B*C$	77.25	−0.05750	0.47625	0.56950	85.25	−0.20250	87.50	−0.05250
Adjusted R^2		0.965	0.891	0.976	0.933	0.994	0.878	0.996	0.837

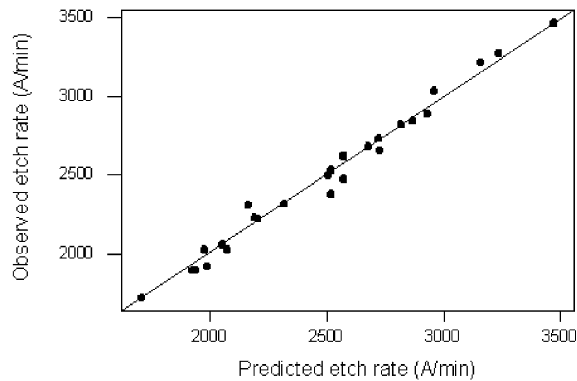


Fig. 1. Comparison of the observed etch rate with the etch rate predicted by Eq. (1).

where ER is the etch rate of the undoped polysilicon in Å/min. An adjusted R^2-value of 0.965 is obtained from the analysis of variance, indicating that this model as fitted explains 96.5% of the variability of the etch rate. Fig. 1 shows the excellent fit to the observed values. From Eq. (2), there exists an obvious positive effect of increasing TCP source power and Cl_2 content for the etch rate of undoped polysilicon. The coefficient values of T (439.67) and C (446.08) are greater than other items of the equation. It means that these two corresponding factors affect the response item ER most, i.e. large values of these coefficients indicate that TCP source power and Cl_2 content dominate the etch rate in these experiments.

Models for other responses could be obtained by a similar approach. As shown in Table 2, TCP source power and Cl_2 content also dominate the etch rate of other polysilicon doping types. All models exhibit excellent good fit with large R^2-values close to 1.

Fig. 2 shows the dependence of the undoped polysilicon etch rate on Cl_2 content and inductive TCP power. The etch rate dramatically increases with both increasing Cl_2 content and TCP power. This may be due to the increase in plasma density of reactive species with these two factors. The

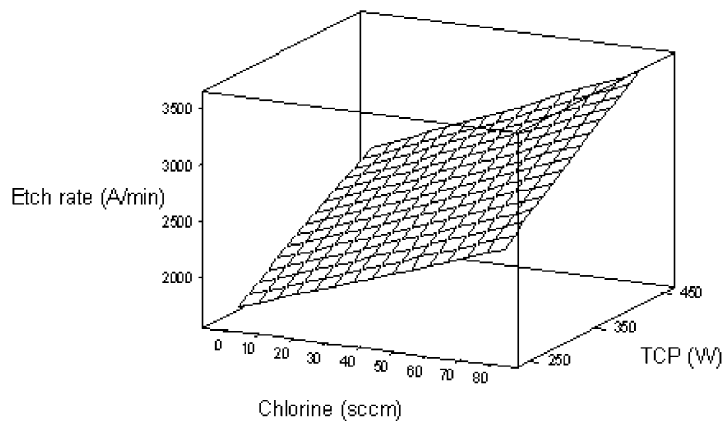


Fig. 2. Undoped polysilicon etch rate response surface as a function of Cl_2 content and TCP source power.

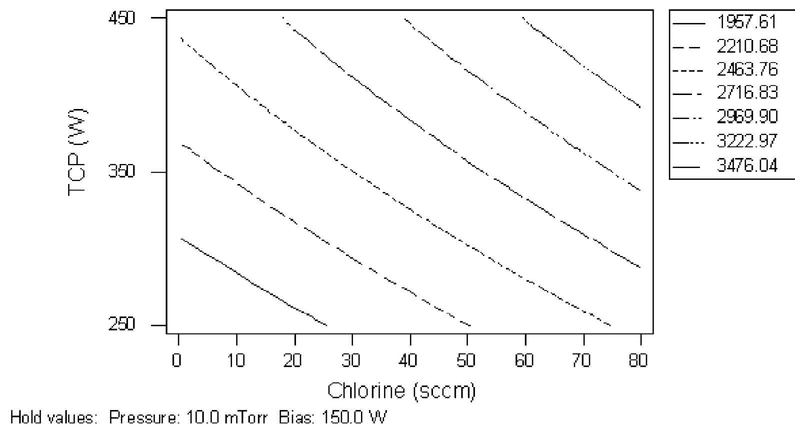


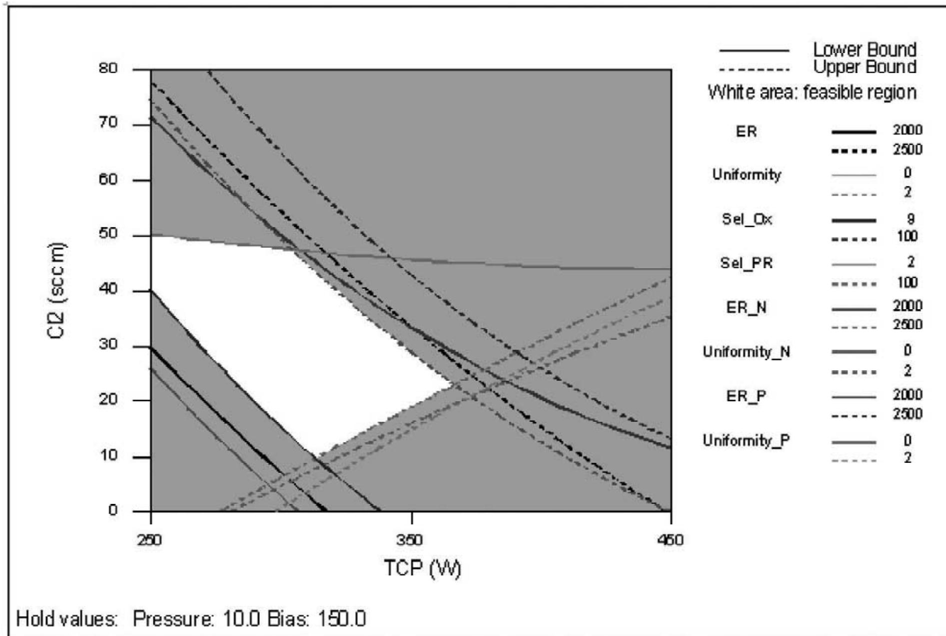
Fig. 3. Contour plot of the undoped polysilicon etch rate as a function of Cl_2 content and TCP source power.

corresponding contour plot is shown in Fig. 3. Response surface plot and contour plot show how a response variable relates to two factors based on a model equation. All response surface plots and contour plots can be drawn in the same manner.

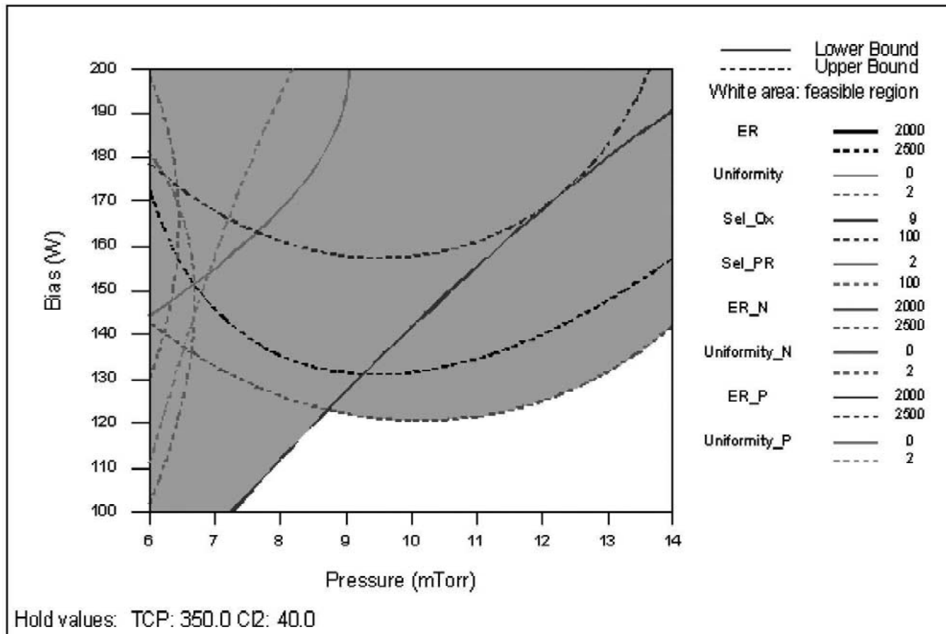
In a contour plot, the fitted response model is viewed as a two-dimensional surface where all points that have the same fitted value are connected to produce contour lines. An overlaid contour plot represents how each response relates to two continuous design variables, while holding all other variables in the model at specified levels [5,16,17]. Fig. 4(a) shows an overlay plot for the responses in this study. To diminish the etch rate differences between different doping types, the contours consist of etch rate (for all doping types) between 2000 and 2500 Å/s; and set other specifications including uniformity (for all doping types, defined as $(ER_{max} - ER_{min})/2ER_{ave})) < 2\%$, selectivity to $SiO_2 > 9$, and selectivity to photoresist > 2. The white area shows the range of TCP power and Cl_2 content where the criteria for all response variables are satisfied. Fig. 4(b) shows the satisfied parameter range for pressure and bias power.

From Fig. 4, a combined optimal condition was selected from the white areas. The selected optimized parameters are shown in Table 3. The corresponding performance of the optimized main etch step is shown in Table 4. It should be noted that recipes used for breakthrough and overetch steps are originally used for undoped poly-Si gate and not specifically optimized in this study. From the experimental results, however, these original recipes appear to be adequate and do not lead to the degradation in etching profile. A typical end-point detection (EPD) result used in the main etch step is illustrated in Fig. 5. Regardless of different poly-Si etch rates in different doping types, precise detection can be obtained under the optimized recipe as shown in this figure.

Figs. 6 and 7 show the cross-section SEM morphology of the etched patterns located at the wafer center and edge, respectively. Anisotropic profile is achieved despite the doping types and pattern location, and no micro-trenching phenomenon of sidewall is observed. The results indicate that the optimized recipe can be successfully applied for etching polysilicon with various doping types and concentrations.



(a)



(b)

Fig. 4. Region of the optimum found by overlaying all responses.

Table 3
Parameters for optimized etch process

Parameters	Breakthrough	Main etch (optimized)	Over etch
Chamber pressure (mTorr)	5	12	25
TCP power (W)	250	310	250
Bias power (W)	200	120	150
Cl_2 (sccm)	80	35	0
HBr (sccm)	0	125	150
O_2 (sccm)	0	0	2

Table 4
Performance for optimized main etch process

Doping type	Performance		
	n^+	Undoped	p^+
Etch rate (Å/min)	2233	2194	2084
Uniformity (%)	1.12	1	1.01
Selectivity (to SiO_2)	~10	~10	~10

3.2. Plasma-induced damage characterization

In this work, we focused on the characterization of plasma charging damage on p-channel MOS devices, since no significant difference is observed among the n-channel MOSFET devices with various antenna sizes. No noticeable antenna effect is found in the capacitor test structures. However, significant dependence on the antenna size is observed on transistor test structures. Specifically, in the measurement condition of $J = 100$ mA/cm^2, 50% Q_{bd} (charge-to-breakdown) is 48.2 C/cm^2 for small

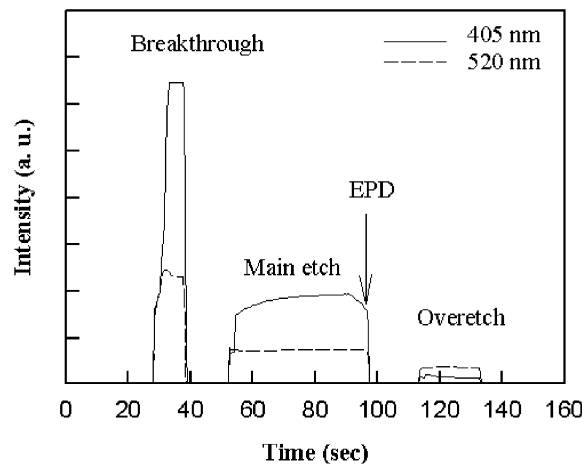


Fig. 5. Typical EPD trace for simultaneously etching polysilicon of different doping types.

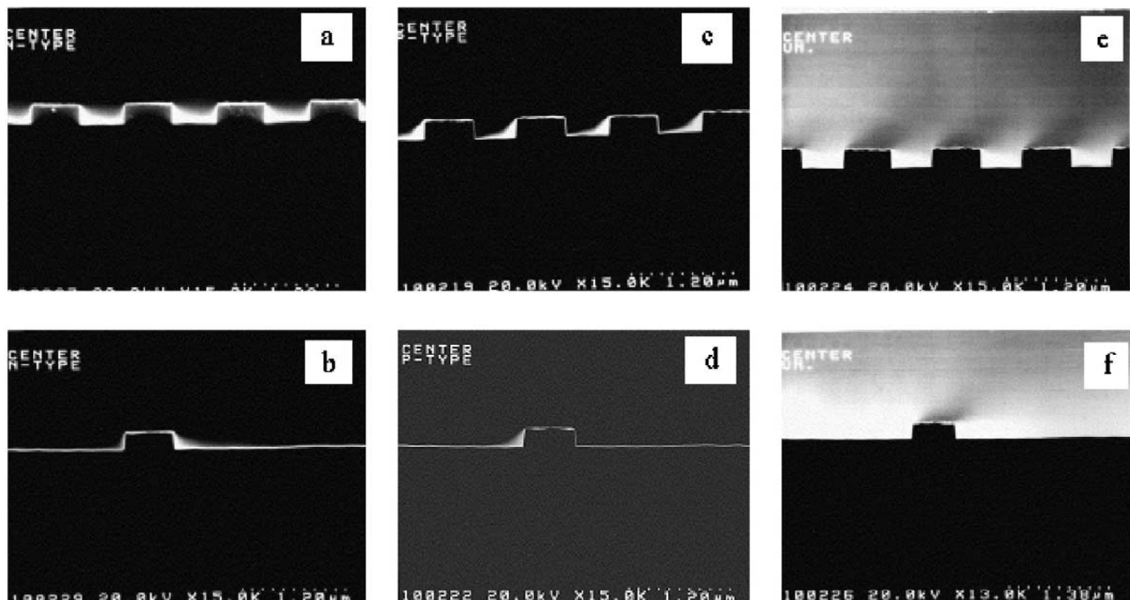


Fig. 6. SEM micrographs of the simultaneously etched profiles (dense or isolated) for (a, b) n^+, (c, d) p^+, and (e, f) undoped poly-Si with the process sequence listed in Table 2. These test patterns are located at the wafer center with nominal line width of 0.5 μm.

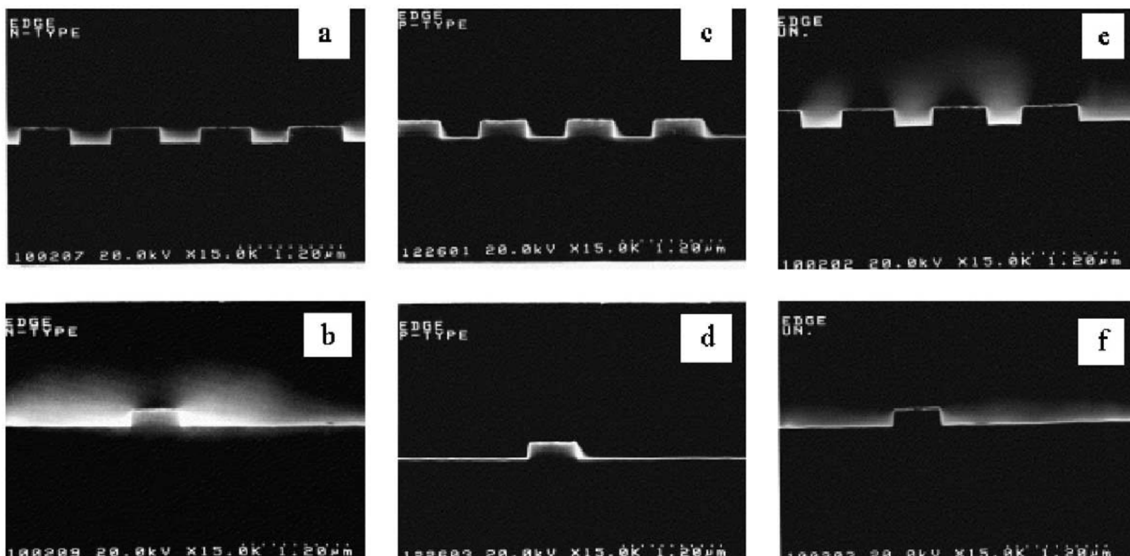


Fig. 7. SEM micrographs of the simultaneously etched profiles (dense or isolated) for (a, b) n^+, (c, d) p^+, and (e, f) undoped poly-Si with the process sequence listed in Table 2. These test patterns are located at the wafer edge with nominal line width of 0.5 μm.

Table 5
50% Q_{db} for capacitors and transistors with small and large antenna structures

	Small antenna (L_p = 330 μm for capacitor, 140 μm for transistor)	Large antenna (L_p = 766 000 μm for capacitor, 320 000 μm for transistor)
50% Q_{bd} value for capacitor (C/cm^2) (area: 20×20 μm^2)	6.2	5.6
50% Q_{bd} value for transistor (C/cm^2) (area: 1×10 μm^2)	48.2	29.9

antenna structure, compared to 29.9 C/cm^2 for large antenna structure. Table 5 lists the results of Q_{bd} tests for p-channel capacitors and transistors, respectively, with edge-intensive poly-gate antenna.

The above findings indicate that test structures play an important role in affecting the plasma damage. The major difference between the capacitor and the transistor test structures is that all poly-Si gate edges in the former group lie exclusively over the field oxide, while parts of the poly-Si gate edge lie over the active region in the latter group. Previously, it has been shown that oxide damage at the gate edge of a transistor, caused by energetic ion or photon bombardment during plasma gate etching, may aggravate the plasma charging damage [18]. This reasonably explains why the antenna effect is more severe in Table 5.

This damage difference was further confirmed by measuring threshold voltage difference between two adjacent transistors with large and small antenna, respectively, so as to minimize the effect due to non-uniform oxide thickness. The results (i.e. $dV_{th} = V_{th}$ (L_p = 32 cm) − V_{th} (L_p = 140 μm)) consistently show a slight negative shift in V_{th} on large antenna transistors, as illustrated in Fig. 8. The charge

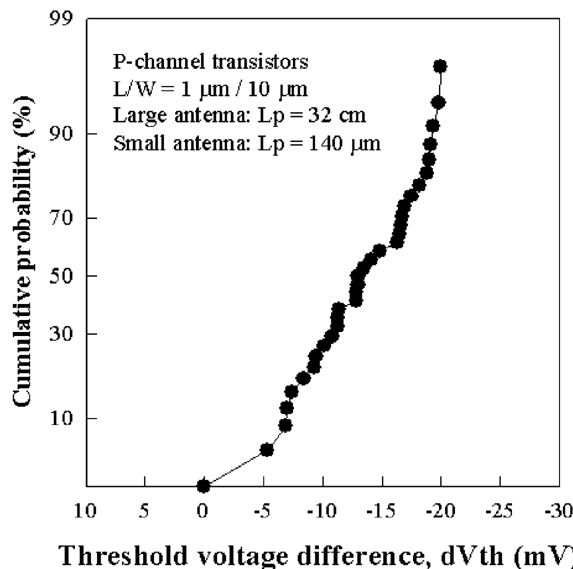


Fig. 8. Threshold voltage difference between a large and a small antenna device that are located nearby. A negative shift is observed for the large antenna device.

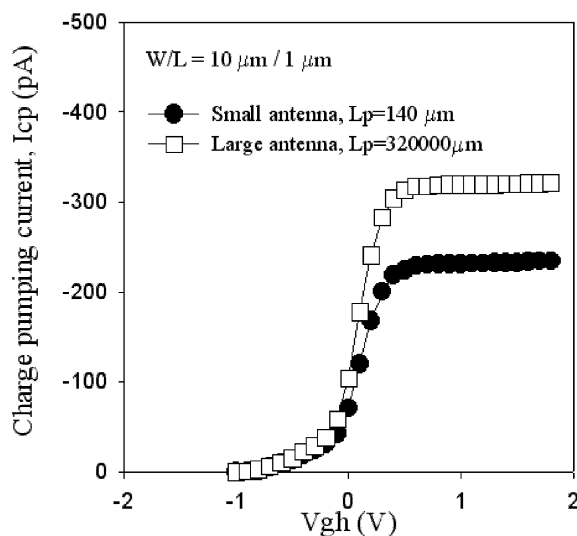


Fig. 9. Typical results of charge pumping current performed on PMOS transistors.

pumping technique was also employed to further analyze these devices. Charge pumping current I_{cp}, which is an indication of interface state density, also confirms that interface state density is typically 1.3–1.5 times larger for the large antenna transistors, as shown in Fig. 9. Nevertheless, it should be noted that the interface state density is in the order of 10^{10} cm^{-2} eV^{-1} for both large and small antenna transistors, suggesting only minimal charging damage. However, this also indicates that H_2/N_2 anneal could not fully passivate the interface defects induced by plasma damage.

4. Conclusion

In this paper, the feasibility of using a commercially available etcher to simultaneously etch n^+, p^+, and undoped poly-Si gate layers has been investigated thoroughly by response surface methodology. Our results indicate that high etching rate, superior uniformity, and profile control can be simultaneously achieved with the obtained optimized recipe. By the RSM optimization, the etch rate differences between different doping types are decreased and excellent end-point detection (EPD) characteristics can be obtained. In addition, only minor plasma charging damage has been observed. A universal recipe for polysilicon films with different doping types therefore appears to be feasible for a commercial TCP etcher, thus simplifying deep sub-micron CMOS process integration.

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