Electrical properties of SiN/GaN MIS diodes formed by ECR-CVD

Kow-Ming Chang [a,*], Chao-Chen Cheng [a], Chia-Ching Lang [b]

[a] *Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsin-Chu 300, Taiwan, ROC*
[b] *Tyntek Corporation, Hsin-Chu Science-Based Industrial Park, Hsin-Chu 300, Taiwan, ROC*

Abstract

Silicon nitride (SiN) film was deposited at 300 °C as the insulating layer of a GaN-based metal–insulator–semiconductor (MIS) diode by using electron cyclotron resonance chemical vapor deposition (ECR-CVD) with silane-to-nitrogen (SiH_4/N_2) flow ratio of 5/45. The deposited film had the refractive index of 1.9–2.0 and the relative dielectric constant of 6. Capacitance–voltage (C–V) characteristics were measured at 1 MHz and interface state densities were obtained by Terman's method. The negative fixed charge density of the SiN film was 1.1×10^{11} cm^{-2} and its breakdown field was greater than 5.7 MV/cm even at 350 °C. The value of the interface state density was less than 4×10^{11} cm^{-2} around the mid-gap and its minimum was 5×10^{10} cm^{-2} eV^{-1} at 0.6 eV below the conduction band edge. From these results, the SiN film deposited by ECR-CVD is a promising gate dielectric for high temperature GaN-MISFET application. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: GaN; Silicon nitride; ECR; Gate dielectric; MISFET

1. Introduction

Gallium nitride (GaN) is considered as a superior material for applications in high-power and high-frequency transistors operating at elevated temperatures [1], owing to the properties of wide bandgap, high breakdown field, high electron mobility and good thermal stability. During the past years, there have been many studies in the development of metal semiconductor field effect transistors (MESFETs), high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). However, the performance of these devices was not so good as expected. For MESFETs and HEMTs, the main problem is the lack of a stable schottky contact [2,3], which must have the low leakage current as well as the reproducible barrier height at the working temperature. For HBTs [4], forming p-GaN base with high conductivity is difficult due to a low carrier concentration and a poor ohmic contact. These problems can be overcome by using a metal insulator semiconductor FET (MISFET) approach as the type of metal oxide semiconductor FET applied in silicon.

MISFET approach requires an insulator layer as the appropriate gate dielectric, which generates low interface state densities (D_{it}) with GaN and itself can tolerate a high breakdown field (E_{bd}). The candidate dielectrics under investigation presently include Ga_2O_3 [5], AlN [6,7], gadolinium gallium garnet (GGG) [8,9], Gd_2O_3 [10], SiO_2 [11–13], and silicon nitride (SiN) [14]. GGG was the first gate candidate to be used in a depletion mode device practically. However, the interface state densities were rather high with a minimal value of 4×10^{11} cm^{-2} eV^{-1} near the mid-gap. A thin layer of single-crystal Gd_2O_3 could be grown epitaxially on GaN with low D_{it} values, but the oxide film contained a high concentration of dislocations that would cause the breakdown field to be quite low. It was necessary to deposit a capping layer of SiO_2 to improve the breakdown field from 0.3 to 0.8 MV/cm. Recently, Gaffey et al. [15] declared that a stacked multi-layer of $SiO_2/SiN/SiO_2$ (ONO)

* Corresponding author. Fax: +886-3-5731887.
E-mail address: kmchang@cc.nctu.edu.tw (K.-M. Chang).

exhibited a breakdown field of 12.5 MV/cm and an interface state density of 5×10^{10} cm^{-2} eV^{-1} by using jet vapor deposition (JVD) followed by annealing treatment at 600 °C for 1 h. Nakasaki et al. [16] did a pioneering work that a single layer of SiN film deposited by electron cyclotron resonance chemical vapor deposition (ECR-CVD) also exhibited a low interface state density. However, their study was mainly focused on N$_2$-plasma cleaning process and was not complete on the device application.

In this study, we concentrate on investigating the electrical properties of SiN/GaN metal–insulator–semiconductor (MIS) diodes and the SiN film deposition process. The fixed charge density and the interface state density were obtained by analyzing the high-frequency capacitance–voltage (*C–V*) curves. Leakage current–voltage (*I–V*) curves and breakdown field data were measured at room temperature and other high temperatures, respectively. The mechanism of carrier transport in the MIS diode was proposed and discussed. Finally, the electrical characteristics of all candidate dielectrics were addressed and compared.

2. Experiment

The samples used in this study were n-type GaN grown on sapphire substrates by metal organic chemical vapor deposition. The grown epitaxial layers consisted of (0 0 0 1)-oriented buffer layer, unintentionally doped GaN, and Si-doped n-GaN. The electron carrier concentration of the n-GaN layer was 2×10^{17} cm^{-3} and the thickness was 2 μm. The samples were cleaned by hot acetone, HCl (17% vol.) and NH$_4$OH (5% vol.) prior to loading into the ECR-CVD chamber.

As shown in Fig. 1, the ECR-CVD system injected nitrogen (N$_2$) gas to the ECR zone to generate high-density plasma. The plasma reacted with the silane gas (SiH$_4$), which flowed from a gas ring, to form silicon nitride film on the sample. During the deposition process, the sample holder was heated to 300 °C and rotated to obtain a dense and uniform film. The working pressure was 1.33×10^{-3} mbar, and the flow rate of SiH$_4$ and N$_2$ were controlled at 5 and 45 sccm, respectively. The microwave power was 250 W with 2.45 GHz and was accompanied by a magnetic field of 875 G in the resonance zone. The film thickness was 70 nm with the deposition rate of 5 nm/min. Aluminum (Al) was then deposited by electron beam evaporation followed by etching and lithography processes to form the circular MIS capacitors with various diameters.

A Keithley 590 analyzer was used to measure the high-frequency (1 MHz) capacitance with a bias sweep rate of 100 mV/s from accumulation to depletion modes. This sweep rate was chosen according 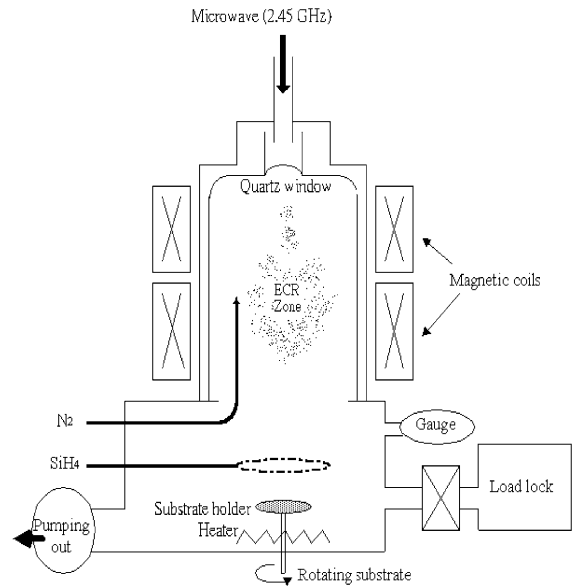to the adequate response time of the interface carriers. Current–voltage (*I–V*) measurements were performed using an HP 4156 semiconductor parameter analyzer. A positive gate voltage was applied on a diode such that most of the bias was added on the dielectric film directly because the underlying semiconductor was in an accumulation mode.

Fig. 1. Schematic sideview of the ECR-CVD system.

3. Results and discussion

The properties of SiN film deposited by ECR-CVD are strongly dependent on the flow ratio of SiH$_4$/N$_2$ and other deposition parameters. Preliminary results showed that both the dielectric constant and the breakdown voltage of the film would reach the maximal values with an optimal flow ratio. The electrical properties relate to the optical constants of the film directly. For saving the cost of GaN epitaxial wafers, the processing parameters must be checked by depositing films on silicon wafers. The optical constants and the thickness can be obtained by reflectance and ellipsometry. As shown in Fig. 2, the refractive index of SiN film was controlled at 1.9–2.0 and extinction coefficient was close to zero in the visible wavelength. The corresponding relative dielectric constant was 6, which was measured at 1 MHz. The film quality was high and reproducible by this checking procedure.

Fig. 3 shows the *C–V* curve with the gate voltage swept from 5 to −12 V. Initially, the diode was in the accumulation state and the capacitance was as high as the intrinsic value of SiN film. As the gate voltage went forward to the negative region, the diode suffered from
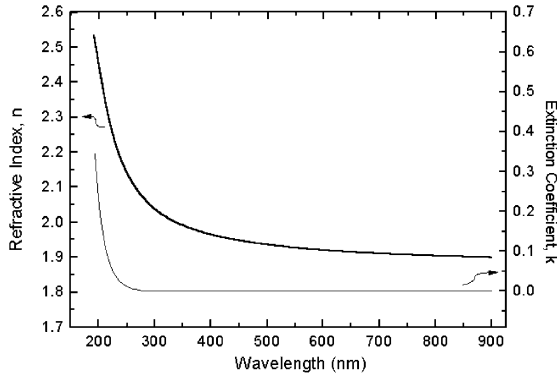
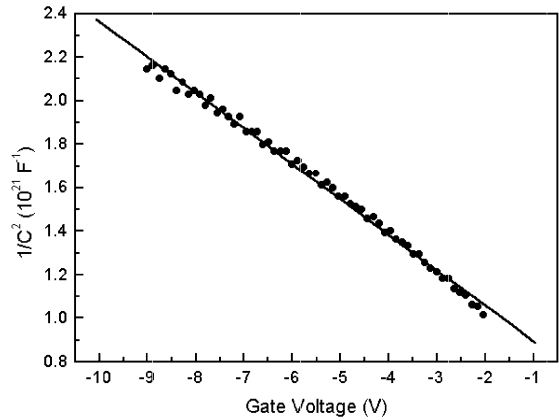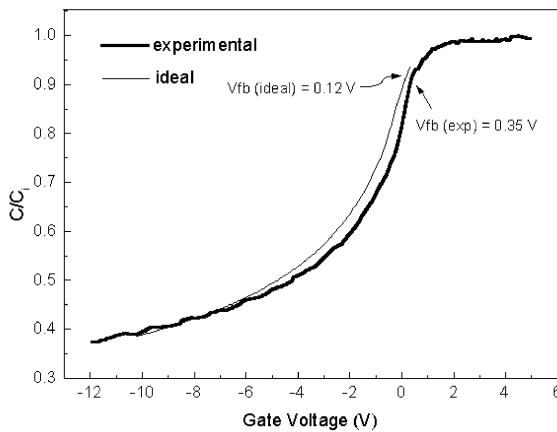Fig. 2. Optical constants of silicon nitride film deposited by ECR-CVD.

Fig. 3. Typical C–V curve of SiN/GaN-MIS diode.

depletion and the capacitance decreased. The net donor concentration of 2.2×10^{17} cm^{-3} could be extracted by fitting $1/C^2$–V data in the depletion region as shown in Fig. 4. Assuming that there was no fixed charge and interface state density in the SiN film, an ideal C–V curve could be calculated and obtained as presented in Fig. 3. In the calculation, the electron affinity, effective density of states in the conduction band, relative dielectric constant of GaN and the work function of Al were taken to be 4.1 eV, 2.6×10^{18} cm^{-3}, 9, and 4.28 eV, respectively. The flat-band voltage (V_{fb}) of an ideal MIS diode would be located at 0.12 V, while the experimental V_{fb} was positioned at 0.35 V. Consequently, a fixed negative charge density of 1.1×10^{11} cm^{-2} was obtained from this V_{fb} shift. The interface state densities (D_{it}) could be also calculated from the difference between the experimental C–V curve and the ideal one. Following Terman's analysis [17], the values of D_{it} were deduced as shown in Fig. 5. The distribution shows that the values of D_{it} are less than 4×10^{11} cm^{-2} eV^{-1} around the mid-

Fig. 4. Experimental and fitting curves of $1/C^2$–V.

gap region and have a minimum value of 5×10^{10} cm^{-2} eV^{-1} at 0.6 eV below the conduction band edge. Some of these results are consistent with Nakasaki's work, but there is an energy shift of D_{it} distribution probably because the deposition conditions have been tuned finely in our work.

The leakage I–V curves at different temperatures are demonstrated in Fig. 6. The SiN/GaN MIS diode was driven by the positive bias and the electron carriers accumulated on the surface of GaN. Therefore, most of the gate voltage fell in the SiN layer. At room temperature, the breakdown voltage had a high value of 11.6 MV/cm. It would decrease as the temperature rose, but a fair value of 5.7 MV/cm could be still obtained at 350 °C. Before breakdown, a major part of the leakage current was in the range from 10^{-9} to 10^{-4} A/cm^2. According to the fitting results of various models, no single conduction mechanism dominated in the leakage behavior. The leakage behavior cannot be explained solely by Frenkel–Poole emission model as demonstrated in SiN/Si MIS diodes [18]. From the XPS work done by Nakasaki et al. [16], the interface of SiN/GaN has the
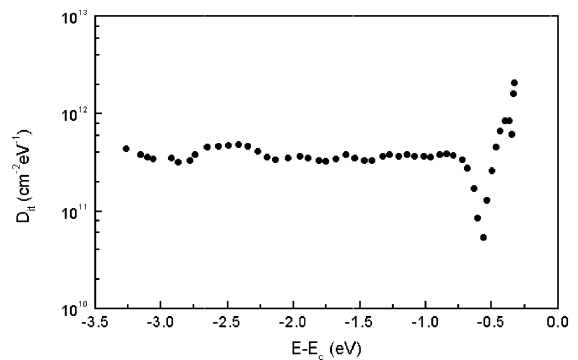

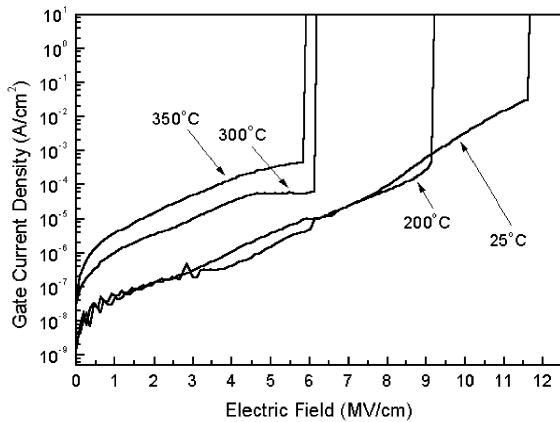Fig. 5. Distribution of interface state densities deduced from Terman's analysis.

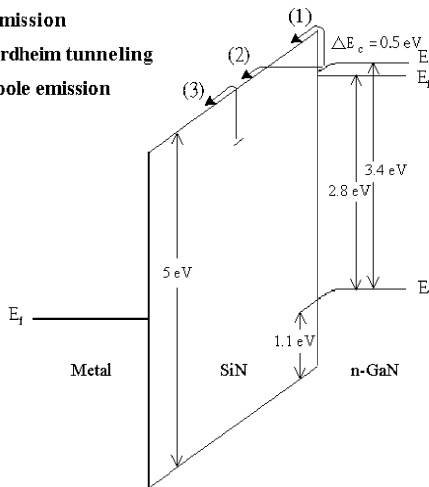Fig. 6. *I–V* curves of SiN/GaN-MIS diode at different temperatures.

Fig. 7. Band diagram illustrating mechanisms of gate leakage currents in SiN/GaN diode.

valence band offset of 1.1 eV, so the conduction band offset can be deduced to be 0.5 eV. As shown in Fig. 7, this low offset value would result in the leakage conduction contributed by both Schottky emission and Fowler–Nordheim tunneling. Therefore, there are three major conduction mechanisms in a SiN/GaN MIS diode.

We compared the characteristics between SiN dielectric and other dielectrics as listed in Table 1. Silicon nitride film deposited by ECR-CVD owned a high breakdown field and a low interface state density as well. These excellent properties make SiN suitable for fabricating GaN-based MISFET devices. Of course, the leakage and breakdown performance of SiN was inferior to those of ONO owing to the moderate bandgap width of 5 eV. However, the higher dielectric constant of silicon nitride may compensate this weakness. In addition, the processing temperature of ECR-CVD is the lowest among the techniques of other candidate dielectrics [19].

4. Conclusion

Silicon nitride deposited by ECR-CVD has been investigated as a gate dielectric of GaN-MIS diode. This dielectric has a negative fixed charge density of 1.1×10^{11} cm^{-2} and a breakdown field of 11.6 MV/cm at room temperature. Before breakdown, a major part of the leakage current was in the range from 10^{-9} to 10^{-4} A/cm^2. Interface state densities were less than 4×10^{11} $cm^{-2} eV^{-1}$ around the mid-gap and the minimum value was 5×10^{10} $cm^{-2} eV^{-1}$ at 0.6 eV below the conduction band edge. In comparison with GGG and Gd_2O_3, silicon nitride exhibited not only low charge densities but also high breakdown fields. The low deposition temperature would also benefit the fabrication of the advanced device structure. Consequently, SiN is a promising gate dielectric for high temperature GaN-MISFET application.

Table 1
Comparison of the characteristics between SiN dielectric and other dielectrics

Material	GGG [8,9]	Gd_2O_3 [10]	ONO [13]	SiN
Structure	Amorphous	Single crystal + SiO_2 layer	Amorphous	Amorphous
Deposition method	E-beam	ECR	JVD	ECR-CVD
Deposition temperature	550 °C	650 °C	600 °C 1 h anneal	300 °C
Dielectric constant, ε_r	14.2	11.4	3.9	6
Bandgap (eV)	4.7	4.4	9.0	5.0
Fixed charge density (cm^{-2})	3.0×10^{11}	NA (high)	$<1 \times 10^{11}$	1.1×10^{11}
Interface state density (cm^{-2})	4.2×10^{11}	NA (low)	5×10^{10}	5×10^{10}
Breakdown field (MV/cm)	12.5	0.8	11.6	11.5

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