An Improved Two-Frequency Method of Capacitance Measurement for $SrTiO_3$ as High-*k* Gate Dielectric

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***Abstract*—An improved two-frequency method of capacitance measurement for the high-*k* gate dielectrics is proposed. The equivalent circuit model of the MOS capacitor including the four parameters of intrinsic capacitance, loss tangent, parasitic series inductance, and series resistance is developed. These parameters can be extracted by independently measuring the capacitor at two different frequencies. This technique is demonstrated for high-*k* $SrTiO_3$ gate dielectrics and the results show that the calibrated capacitances are invariant over a wide range of frequency. In addition, the extracted loss tangent, inductance and resistance are independent on gate voltage and frequency. The effect of series resistance on the frequency dispersion of the capacitance can be also explained by this model. These results indicate that this modified technique can be incorporated in the routine capacitance–voltage (C–V) measurement procedure providing the physically meaningful data for the high-*k* gate dielectrics.**

***Index Terms*—MOS capacitor, capacitance measurement, frequency dispersion, STO gate dielectric.**

I. Introduction

RECENTLY, with the emerging industrial requirement of the ultrathin gate oxides (Equivalent oxide thickness (EOT) $<$ 3 nm), many new high-*k* gate dielectrics have been studied because they can provide much less leakage current than the traditional SiO_2. For the MOS devices, the capacitance measurement is one of the most fundamental method to characterize the electrical properties of the high-*k* gate dielectrics. However, the capacitance measurements for those devices often show large variations at high frequencies. This phenomenon may not be due to the intrinsic dielectric dispersion of the material. Recently, Barlage *et al.* [1] demonstrated that the dielectric constant of HfO_2 and ZrO_2 are invariant with respect to the frequency. We have also studied the dielectric properties of BST thin films by incorporating accurate thru-reflect-line (TRL) calibration [2], [3] and found that the dielectric constants of BST are independent of frequency from 200 MHz to 20 GHz. Therefore, the frequency dispersion of the capacitance measurement of the high-*k* materials may be caused by the extrinsic parasitic effects rather than the intrinsic material properties.

Yang and Hu [4] have first proposed a two-frequency method to improve the capacitance measurement of the MOS capacitor for the ultrathin gate oxides. In their method, a series resistance R_s was added to the equivalent circuit model. The intrinsic capacitance (C_0) and the shunt resistance (R_p) were assumed to be frequency-independent parameters and could be extracted by capacitance measurement at two different frequencies. However, we have found that their method may not apply to the high-*k* gate dielectrics properly. With the same EOT, the leakage currents of the high-*k* gate dielectrics are often much lower than those of the SiO_2. In addition, the equivalent circuit model of the MOS capacitor is the small-signal model rather than the DC model. Therefore, dissipation factor (D) is more relevant to the ac dissipation of the materials, or equivalently the loss tangent. In this situation, the shunt resistive part of the equivalent circuit should be modeled by the loss tangent of the high-*k* gate dielectric rather than simply a constant resistance. According to the well-known Kramers–Kronig relation, if the dielectric constant of the material is frequency independent, the loss tangent must also be independent on frequency. Therefore, we assume that both the capacitance (C_0) and loss tangent ($\tan\delta$) are frequency independent. This assumption is different from that R_p is independent on frequency [4], which may not have proper physical meaning. In addition, the external probes and equipment wiring may cause parasitic inductances that are found to be several micro Henry [5]. These parasitic inductances cause large errors in the high frequency capacitance measurement. Therefore, loss tangent ($\tan\delta$) and parasitic series inductance (L_0) are employed in our modified four-element equivalent circuit model for the MOS capacitor.

II. Theory

For the equivalent circuit of the four-element model, the complex impedance is given by

$$Z(\omega) = R_s + j\omega L_0 + \frac{\tan\delta - j}{\omega C_0(1+\tan\delta^2)}. \tag{1}$$

Since the ordinary capacitance–voltage (C–V) measurements provide parallel-mode C-D raw data, the parameters can be derived from the measured impedances as the following:

$$\tan\delta = \frac{D_1 f_2 C_2(1+D_2^2) - D_2 f_1 C_1(1+D_1^2)}{f_2^2 C_2(1+D_2^2) - f_1^2 C_1(1+D_1^2)}(f_1+f_2) \tag{2}$$

$$C_0 = \frac{\tan\delta}{1+\tan\delta^2}\frac{C_1C_2(1+D_1^2)(1+D_2^2)(f_2-f_1)}{D_1 f_2 C_2(1+D_2^2) - D_2 f_1 C_1(1+D_1^2)} \tag{3}$$

$$R_s = \frac{D_2}{2\pi f_2 C_2(1+D_2^2)} - \frac{\tan\delta}{2\pi f_2 C_0(1+\tan\delta^2)} \tag{4}$$

$$L_0 = \frac{1}{(2\pi f_2)^2 C_0(1+\tan\delta^2)} - \frac{1}{(2\pi f_2)^2 C_2(1+D_2^2)} \tag{5}$$

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where C_1 and C_2 are the measured capacitances, and D_1 and D_2 are the measured dissipation factors at frequencies f_1 and f_2, respectively. Equations (2)–(5) can be calculated step-by-step and all the intrinsic and extrinsic parameters can be extracted at various gate voltages and pairs of frequency. The four-element model is more relevant compared to the previous three-element model [4] because the measured complex impedances at two different frequencies would provide four independent equations. However, the three-element model is not able to provide a consistent result to satisfy all the above equations.

III. Application Examples and Discussion

In this experiment, $SrTiO_3$ (STO) was chosen to demonstrate the capacitance measurements for the high-*k* gate dielectric because STO posses a very high dielectric constant and low loss tangent. In addition, STO [6] can be epitaxially grown on silicon substrates with good interfacial properties. P-type 4-in (100) silicon wafers with resistivity of $1 \sim 5\,\Omega$-cm were used as the substrate in this experiment. After standard RCA cleaning, 8-nm SiON film was thermally grown at 950 °C in pure N_2O gas in furnace. The SiON was then removed by HF dip. Nitrogen was moderately incorporated to alleviate the reaction of the silicon surface into SiO_x thin interface layer during the high-temperature growth of STO gate dielectric, resulting in better EOT and lower interface trap densities. After SiON was removed, 25-nm STO thin films were deposited by radio frequency magnetron sputtering at 450 °C. Detailed description of the process treatments and dielectric properties of the STO thin films will be reported in another paper [7]. Aluminum was used as the probe pads and ohmic contact for the backside of the silicon substrates.

The capacitance of STO gate dielectric with area of 7×10^{-4} cm^2 was measured by HP 4284A at various frequencies, and the results are shown in Fig. 1. The deviation of the accumulation capacitance is larger than 6%. The leakage current density shown in the inset of Fig. 1 is below 10^{-4} A/cm^2 at -3 V, indicating that the direct tunneling of STO gate can be neglected. The inset of Fig. 2 shows the improved four-element equivalent circuit model for the MOS capacitors with high-*k* gate dielectrics. The result of calculated capacitances based on this model (Fig. 2) indicates that the calibrated capacitances at each pair of frequency coincide with each other very well, and the variation of capacitance is reduced to be less than 0.1%. The quantum mechanical curve fitting [8] is also shown in Fig. 2, in which the EOT is extracted to be 3 nm. The measured C–V curves are in good agreement with the theoretically fitted curve, indicating that the interface trap density is low.

The calculated loss tangent, series resistance, and parasitic inductance are shown only at the accumulation region ($V_G < -1.5$ V). Beyond the accumulation region, the measured dissipation factors (D_1 and D_2) fluctuated significantly between negative and positive values. This phenomenon is attributed to the thermal noise. When the MOS capacitor is biased at depletion and inversion regions, it causes thermal generation of electron-hole pairs at the depletion region, resulting in thermal noise during the capacitance measurement. Therefore, the capacitance measurements at depletion and inversion regions may not be adequate for extracting the circuit parameters.

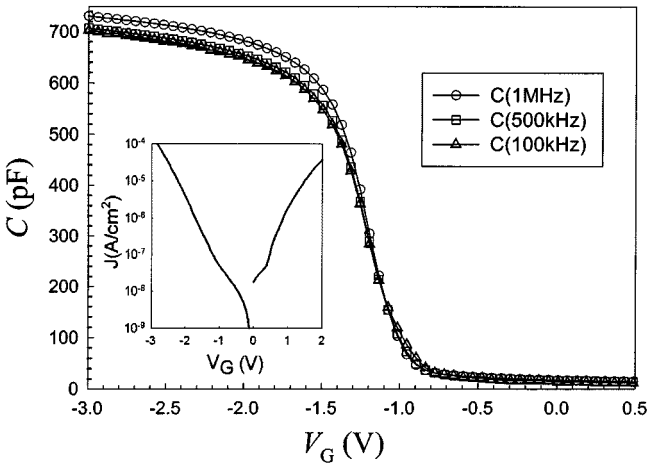

Fig. 1. Measured capacitances of MOS capacitors with STO gate dielectric at three different frequencies. The inset is the plot of leakage current density versus gate voltage.

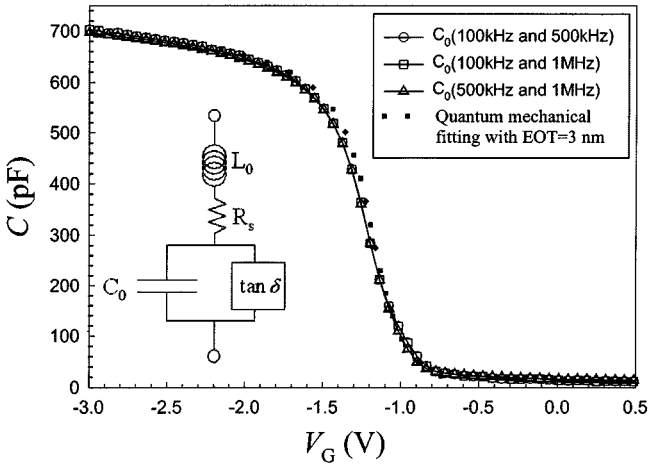

Fig. 2. Calculated capacitances by the four-element model at different pairs of frequency. The dotted line is the quantum mechanical fitted curve with EOT = 3 nm.

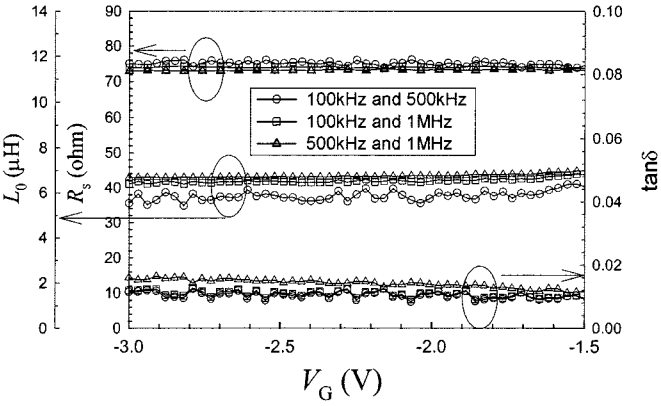

Fig. 3. Calculated loss tangent, series resistance, and parasitic inductance by the four-element model at various gate voltages and pairs of frequency.

The extracted loss tangent shown in Fig. 3 is 0.015, indicating the STO gate dielectric is very low-loss. The extracted series resistance and parasitic inductance are 75 Ω and 6.5 μH, respectively. The extracted parasitic inductance is close to the reported

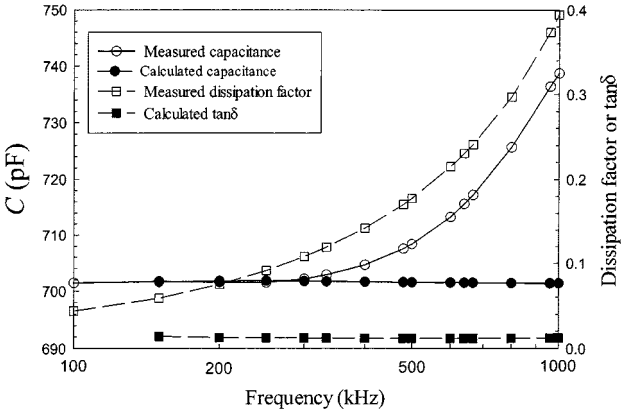

Fig. 4. Frequency dispersion of the STO gate dielectrics before and after the four-element model calibration at frequencies ranging from 100 kHz to 1 MHz. The two-frequency calculation are carried out by fixing $f_1 = 100$ kHz and varying f_2. The gate voltage is fixed at -3 V.

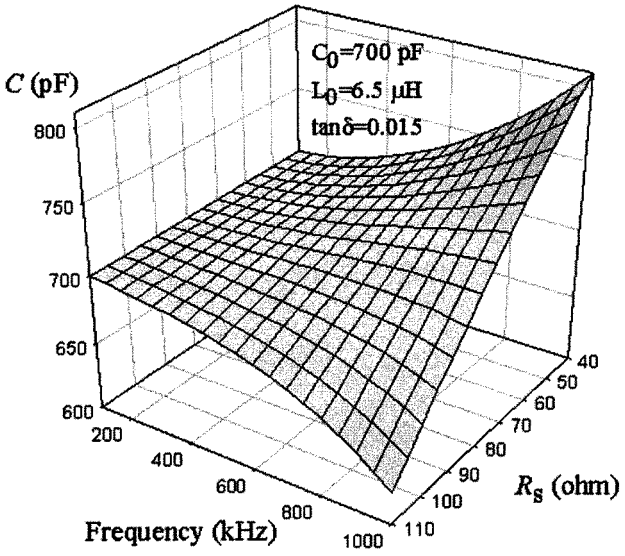

Fig. 5. Effect of series resistance on the measured capacitance as a function of frequency. The simulation results are calculated according to the equivalent circuit model in the inset of Fig. 2. $C_0 = 700$ pF, $L_0 = 6.5\ \mu$H, and $\tan\delta = 0.015$ in this calculation.

results [5] in the order of magnitude. The calculated $\tan\delta$, R_s and L_0 are basically independent on gate voltage and frequency, indicating that the results are self-consistent with the assumption of this model. The extracted series resistance is reasonable compared with the spreading resistance of the substrate that can be roughly estimated by

$$R_s \sim \text{resistivity} \times \text{thickness} \div \text{capacitor area} \sim 100\,\Omega. \quad (6)$$

It shows slight difference in R_s among several different samples because of the variations of the substrate resistivity and the aluminum contact resistance.

The frequency dispersion of the capacitance, measured dissipation factor and calculated $\tan\delta$ are shown in Fig. 4. The measured capacitances and dissipation factors increase with respect to the frequency, while the calculated capacitances and loss tangents by our method are invariant with respect to the frequency. This result indicates that the frequency dispersion of the high-*k* gate dielectrics can be effectively eliminated by this method. In addition, our method provides the merit that the loss tangent of the material can be extracted, which is rarely mentioned in the previous literatures for the MOS capacitors. We have also measured other samples and found that the capacitances of some samples decrease with respect to the frequency (not shown here). The behavior of frequency dispersion of the capacitance is found to be related to the series resistance. Fig. 5 shows the simulation result of the effect of series resistance on the frequency dispersion of the capacitance. Lower R_s results in the increasing capacitances with respect to the frequency, while higher R_s results in the opposite behavior. This simulation result shows that the measured capacitance is sensitive on the series resistance. The present improved two-frequency method can effectively provide the calibration of the capacitance measurement.

IV. Conclusions

A four-element model for the MOS capacitor is proposed. The experimental results of the capacitance measurements of STO gate dielectrics confirm the accuracy and consistency of our model. This method can be incorporated in the routine robust C–V measurement procedures providing physically meaningful data for the high-*k* gate dielectrics.

References

[1] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, A. Murthy, B. Roberds, P. Stokley, and R. Chau, "High-frequency response of 100 nm integrated CMOS transistors with high-*k* gate dielectrics," in *IEDM Tech. Dig.*, 2001, pp. 10.6.1–10.6.4.

[2] H. T. Lue and T. Y. Tseng, "Application of on-wafer TRL calibration on the measurement of microwave properties of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 48, pp. 1640–1647, June 2001.

[3] H. T. Lue, T. Y. Tseng, and G. W. Huang, "A method to characterize the dielectric and interfacial properties of metal – insulator – semiconductor structures by microwave measurement," *J. Appl. Phys.*, vol. 91, no. 8, pp. 5275–5282, 2002.

[4] K. J. Yang and C. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Trans. Electron Devices*, vol. 46, pp. 1500–1501, July 1999.

[5] A. Nara, N. Yasuda, H. Satake, and A. Toriumi, "Applicability limits of the two-frequency capacitance measurement technique for the thickness extraction of ultrathin gate oxide," *IEEE Trans. Semiconduct. Manufact.*, vol. 15, pp. 209–213, May 2002.

[6] K. Eisenberg, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopad, W. J. Ooms, L. Salem, S. Bradshaw, and C. D. Overgaard, "Field effect transistor with $SrTiO_3$ gate dielectrics," *Appl. Phys. Lett.*, vol. 76, no. 10, pp. 1324–1326, 2000.

[7] C. Y. Liu, H. T. Lue, and T. Y. Tseng, "Effects of nitridation of silicon and heat treatment on the dielectric properties of $SrTiO_3$ gate dielectrics," *Appl. Phys. Lett.*, to be published.

[8] [Online.] Available: www.device.eecs.berkeley.edu/qmcv/html. Berkeley Device Group, Berkeley, CA.