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High power $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ enhancement-mode PHEMT for low-voltage wireless communication systems

S.H. Chen, Li Chang, E.Y. Chang, J.W. Wu and Chun-Yen Chang

A 20 mm-wide enhancement-mode pseudomorphic high-electron-mobility transistor (E-PHEMT) has been developed. The device has high transconductance of 490 mS/mm, and high maximum drain current of 350 mA/mm due to the use of an $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$-based structure for carrier confinement. At 1.9 GHz and 3.0 V, the E-PHEMT shows 34.1 dBm (128 mW/mm) output power with power-added efficiency (PAE) of 64.5%. At 2.4 V, the maximum saturated output power is 32.25 dBm and maximum PAE is 78.5%. The E-PHEMT demonstrates excellent power performance at 1.9 GHz and below 3 V.

Introduction: High-performance power amplifiers can provide sufficient output power with smaller device periphery, resulting in smaller chip area and reduced production cost. For cellular handset application in modern wireless communication, a low-voltage-operation power amplifier is desired to decrease the weight and size of the handsets. Pseudomorphic high-electron-mobility transistors (PHEMTs) [1–3] have shown superior power performance at high-frequency and low-voltage operation and have been widely studied to characterise and improve their performance. In recent years, enhancement-mode (E-mode) device technology has drawn the attention of many researchers. This is due to E-mode devices requiring only single-voltage supply for operation, thus avoiding the use of negative voltage in the circuit, and the resulting simpler design and further reduced production cost.

In this Letter a high performance E-mode PHEMT (E-PHEMT) [4–8] with $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ hetero-interface structure is developed based on the well-designed epi-structure, device layout and manufacturing process. The developed E-PHEMT achieves single-voltage and low-voltage operation simultaneously and demonstrates very high power and efficiency performance at 1.9 GHz.

Device structure and manufacturing process: The epi-layers of the E-PHEMT were grown by molecular beam epitaxial (MBE) on the 3-inch GaAs wafer. The epi-structure consists of an GaAs buffer layer, AlGaAs/GaAs superlattice, upper and lower $Al_{0.3}Ga_{0.7}As$ spacers, an $In_{0.2}Ga_{0.8}As$ channel layer which is sandwiched between the two spacers, two Si planar-doped layers, $Al_{0.3}Ga_{0.7}As$ Schottky layer, and the top GaAs capping layer. AlGaAs with Al mole fraction of 0.3 is used as the Schottky layer to increase the barrier height and the conduction band discontinuity between AlGaAs and InGaAs layer. Two Si-planar-doped layers with doping concentration of $4\times10^{12}/cm^2$ and $1\times10^{12}/cm^2$ were used to supply high carrier concentration in the quantum well at the $Al_{0.3}Ga_{0.7}As$ and $In_{0.2}Ga_{0.8}As$ interface.

The manufacturing process of the E-PHEMT includes mesa isolation, AuGe/Ni/Au ohmic metal deposition, gate definition by deep-UV lithography, gate recess by citric acid-based solution, Ti/Pt/Au gate metal deposition, silicon nitride passivation by plasma enhanced chemical vapour deposition (PECVD), contact via and gold-plated air-bridge formation. After the front-side process was finished, the wafer was thinned to 4 mil. The gate-to-source spacing of the E-PHEMT is 2 μm. The manufactured device has total gate width of 20 mm and gate length of 0.5 μm.

Device performance: Fig. 1 shows the I-V characteristics of the 120 μm-wide device. The values of V_T, maximum transconductance and maximum drain current (Imax, at $Vgs = 1$ V) density of the manufactured E-PHEMT are 0.09 V, 490 mS/mm and 350 mA/mm, respectively. The high Imax is due to the use of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ layers. Ron is 3.1 Ω-mm which is defined at $Vgs = 1.0$ V. V_k is 0.31 V defined as Vds when Ids reaches 100 mA/mm at $Vgs = 1.0$ V. Combining high Imax with low V_k makes the developed E-PHEMT suitable for power applications under low voltage.

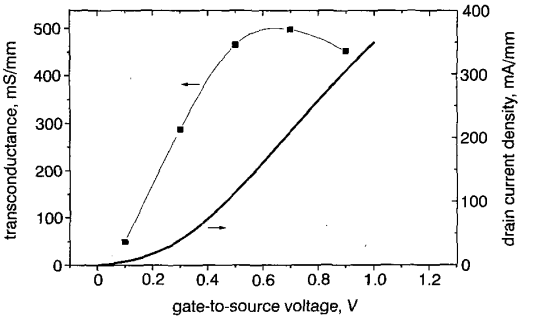

Fig. 1 *I-V characteristics of 120 μm E-PHEMT*
Device biased at $Vds = 2.5$ V

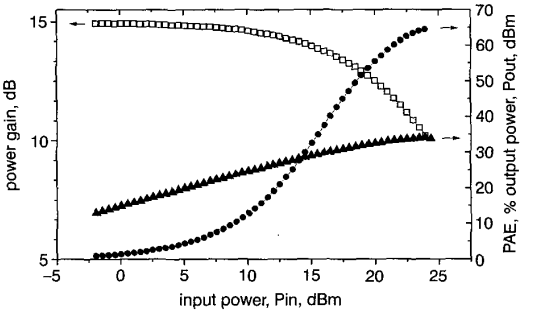

Fig. 2 *Power performance of 20 mm E-PHEMT*
Device biased at $Vds = 3.0$ V and 1.9 GHz, idle current = 700 mA
□ gain • PAE ▲ Pout

The power performance of the E-PHEMT was evaluated at 1.9 GHz. As shown in Fig. 2, at drain bias of 3 V and idle current of 700 mA, the E-PHEMT demonstrated a saturated output power of 34.1 dBm (2.57 W, 128 mW/mm) with associated power-added efficiency (PAE) of 64.5%. The E-PHEMT demonstrated higher output power density than previous reported results which are measured at 3.5 V and near 0.85 GHz operation [4–6].

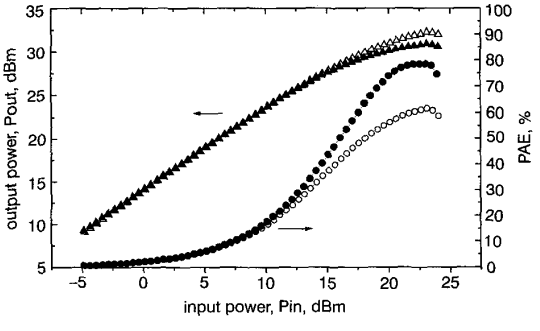

Fig. 3 *Power performance of 20 mm E-PHEMT matched for maximum output power and PAE, respectively*
Device biased at $Vds = 2.4$ V and 1.9 GHz, idle current = 500 mA
□ Pout (max Pout match) ▲ Pout (max PAE match)
○ PAE (max Pout match) • PAE (max PAE match)

When the drain bias is 2.4 V and the idle current is 500 mA (7% of Imax), the power performance matched for maximum output power and PAE is shown in Fig. 3. The E-PHEMT was first tuned for maximum output power. The device delivered a saturated output power of

32.25 dBm with associated PAE of 61.45% at 2.4 V. When the E-PHEMT was matched for maximum PAE the device demonstrated a very high maximum PAE of 78.5% with output power of 30.82 dBm. The linear power gain is 14.18 dB.

The accomplishment of excellent power performance of the E-PHEMT at high frequency and low voltage is due to: (i) the use of $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ hetero-interface which increases the conduction band discontinuity for the quantum well, resulting in high current density and consequently high output power; (ii) precisely controlled gate recess process results in better current control capability by gate bias, and hence high transconductance and high power gain; (iii) the gate-to-source spacing is 2 μm, resulting in low knee voltage, which improves performance at low voltage.

Conclusion: An $Al_{0.3}Ga_{0.7}As/In_{0.2}Ga_{0.8}As$ E-PHEMT has been developed for high power applications. The E-PHEMT has V_T of 0.09 V, low V_k of 0.31 V, high maximum gm of 490 mS/mm, and high Imax of 350 mA/mm. At 1.9 GHz, the E-PHEMT shows 34.1 dBm (128 mW/mm) output power with PAE of 64.5% at 3 V bias. Maximum saturated output power of 32.25 dBm and maximum PAE of 78.5% are achieved at 2.4 V bias. The E-PHEMT exhibits excellent power performance with high power density and PAE at low bias voltage compared to previous reported works. The results show the E-PHEMT has great potential for power applications in wireless communication systems.

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Si/SiGe *n*-channel modulation-doped field effect transistor on air

S.M. Li and K. Fobelets

Si/SiGe *n*-channel modulation-doped field effect transistors (MODFETs) have been fabricated on a 10 μm-thick membrane by removal of the Si substrate and SiGe virtual substrate under the device layers. The membrane devices, surrounded by air, were characterised after thinning and compared to the unthinned characteristics. A large reduction of the off-currents of the MODFETs on air, due to an increase in substrate resistance, has been measured, making them more suitable for low-power applications.

Introduction: *N*-channel Si/SiGe modulation-doped field effect transistors (MODFETs) are grown on Si using a relaxed graded SiGe virtual substrate (VS) to accommodate the lattice constant difference between Si and SiGe. In this way, a strained Si quantum well can be defined for electron conduction sandwiched between relaxed SiGe layers. For low-power operation, with devices biased in the subthreshold region [1], it is important to isolate the device layers from the substrate to minimise leakage currents through the substrate. This can be done using a *p*-doped VS underneath the *n*-doped device layers. Theoretically this reversed biased *pn* junction offers good isolation from the substrate. However, we measured substantial leakage currents through the substrate in VS-based SiGe MODFETs despite recent quality improvements of the VS material. TEM investigations on similar devices have shown the existence of dislocations which occur perpendicular to the *pn* junctions [2], allowing currents through into the substrate. These substrate currents increase the off-currents in the device and should be minimised for low-power operation.

Different approaches can be undertaken to avoid leakage currents into the non-ideal SiGe VS: (i) the use of SiGe-on-insulator (SGOI) [3] equivalent to SOI, (ii) the use of direct bonding techniques [4] to define SiGe-on-insulator, or (iii) the removal of the Si substrate and SiGe VS using processing techniques. In this Letter, the third approach has been taken to fabricate SiGe MODFETs on air. In this approach the SiGe MODFETs are first fabricated using conventional processing technology for Si CMOS with reduced thermal budget. Devices are characterised before membranes are etched, by removal of the Si substrate and SiGe VS.

Fabrication: To remove the substrate underneath the already processed devices, special precautions need to be taken to avoid deterioration of the devices during this post-processing stage. High-temperature processes normally used to protect the surface of Si wafers for deep wet etching steps as used in micro-machining are not allowed since these would destroy the quality of the metal contacts and would deteriorate the abrupt heterojunctions due to germanium and doping segregation. Therefore a new technique has been developed to enclose the devices in an SiO_2 box, produced by thermal oxidation on Si substrates. Thermal SiO_2 was shown to have an excellent resistance to TMAH, the chemical used for removing the Si and SiGe VS substrates. The thickness of the remaining VS after thinning is measured, using an optical microscope, to be around 5 μm. More precise control of the thickness of the membrane under the device layers can be achieved by incorporating etch stop layers above the VS during growth. The thinned devices were also successfully bonded onto an insulating substrate (glass), which made them more robust for measurement, though careful probing is still needed.

The device layer structure is, from bottom to top: *p*-Si substrate; $Si_{1-x}Ge_x$ graded VS, x: 0 – >30%, $p = 5 \times 10^{17}$ cm^{-3}; 500 nm $Si_{0.7}Ge_{0.3}$ constant composition layer, $p = 5 \times 10^{17}$ cm^{-3}; 200 nm $Si_{0.7}Ge_{0.3}$ unintentionally doped (un) setback; 8 nm Si strained QW (un); 5 nm $Si_{0.7}Ge_{0.3}$ spacer (un); 30 nm $Si_{0.7}Ge_{0.3}$ supply layer, $n = 5 \times 10^{17}$ cm^{-3}; and a 35 nm SiO_2 low-temperature LPCVD gate oxide. The unintentionally doped layers have a doping density of $n = 10^{16}$ cm^{-3} *n*-type. Al/Si, on implanted material, is used for source-drain contacts, while the gates are *n*-type polySi. The LPCVD gate oxides were chosen to restrict the thermal budget on the samples. Gate leakage currents tend to be high and are on average 0.08 mA at 1 V increasing to 0.3 mA at 3 V V_{GS}. The gate length and width are 3 and 600 μm, respectively. The threshold voltage is around $V_T = 1.5$ V.