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Self-aligned fabrication of thin-film transistors with field-induced drain

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Abstract

Thin-film transistor (TFT) devices with either a top or a bottom sub-gate were fabricated and characterized. The top sub-gate scheme allows the self-aligned formation of main-gate with respect to the sub-gate. On the other hand, the bottom sub-gate scheme features a self-aligned field-induced drain with a sidewall spacer located on its top to set the effective field-induction-drain (FID) length. Unlike the conventional TFTs, the FID serves to distribute the high drain electric field and thereby eliminates gate-induced drain leakage-like off-state leakage current. Superior device performance is realized with the bottom sub-gate structure. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: Thin-film transistor; Field-induced drain; Leakage

1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been used in a wide variety of applications. They are receiving increasing attention as they represent the most promising candidates for integrating switching elements and peripheral drivers in high-performance large-area active matrix liquid-crystal display (AMLCD) system. The feasibility of integrating peripheral driver circuits directly on the same substrate greatly improves the display system reliability and also lowers system cost by reducing the number of external connections [1,2].

However, an anomalous off-state leakage current that increases with drain bias and gate bias has been the key show-stopper for conventional poly-Si TFTs [3]. This undesirable off-state leakage current makes poly-Si TFTs unacceptable in many high-performance switching circuit applications. For example, the off-state leakage current should be <0.1 pA per micrometer of channel width to keep a high-voltage holding ratio [4]. The cause of the off-state leakage current is generally attributed to field emission of electrons via grain boundary traps as a result of the high electric field near the drain junction [3]. In order to reduce the electric field near the drain, some methods, such as lightly doped drain (LDD) [5–7], and field-induction-drain (FID) structures [8,9], have been proposed.

For TFTs with the LDD structure, the off-state leakage is reduced by a lower channel electric field near the heavily doped drain. However, the on-current also tends to degrade significantly due to increase in parasitic resistance introduced by the LDD region.

The FID approach sets an undoped offset region in the active channel layer between the drain and the region directly underneath the gate. A field-plate (or a sub-gate) is used to induce an electrical junction in the offset channel regions. The electrical junction serves to distribute the electrical field between the gate and the drain electrodes, thus reduces the peak field strength. Unlike the LDD approach, the FID structure is inherently free from any implant damage associated with the LDD region. In fact, the combination of a reduced drain electric field and the damage-free feature is

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believed to be responsible for the observed low off-state leakage in TFTs with FID [10]. It has also been shown that, by applying a proper bias to the field-plate, the on-current will not be adversely affected. However, the original FID approach is susceptible to photomasking misalignment error [8–10], a major drawback inherent in its fabrication process because the length of the FID region is set by two separate photolithographic steps.

In this paper, two new self-aligned TFT processes have been developed. Two types of sub-gate architectures, namely, bottom and top sub-gates, have been employed for FID formation. For the top sub-gate scheme, the main-gate could be self-aligned to the sub-gate. While for the bottom sub-gate devices, a self-aligned sidewall spacer located on top of the drain offset region is used to set the effective FID length. A bottom sub-gate situated underneath the drain offset region is used to electrically induce the field-induced-drain. Therefore, unlike the conventional off-set-gated TFTs with their effective FID length defined by two separate lithography steps, the new self-aligned field-induced drain (SAFID) is completely immune to the photomasking misalignment errors.

2. Experiments

2.1. Fabrication of SAFID TFT with top sub-gate

Fig. 1 depicts a fabrication flow and cross-sectional view of a SAFID TFT with top sub-gate. A 50 nm CVD amorphous thin Si film was deposited at 550 °C, and transformed into polycrystalline phase by a solid-phase re-crystallization (SPC) at 600 °C for 24 h to serve as the active device layer. Subsequently, a nitride (50 nm)/n^+ poly-Si (200 nm)/LPTEOS (20 nm) stacked layer was deposited. Then, the sub-gate was patterned and etched to expose the nitride layer (Fig. 1(a)). Next, the self-aligned sidewall spacers were formed by the deposition of an oxide layer and subsequent reactive-ion-etching (Fig. 1(b)). Then, the nitride layer was etched in H_3PO_4 at 150 °C with the poly-Si layer serving as a stopping layer (Fig. 1(c)). A 20 nm CVD oxide layer was then deposited to form the gate insulator. A third poly-Si film was deposited and patterned to form the top-gate (i.e., main-gate). Finally, self-aligned source/drain regions were formed by a heavy-dose implant (Fig. 1(d)). For n-channel transistors, As^+ implant with a dosage of 5×10^{15} cm^{-2} at 20 keV was used. The implanted dopants were subsequently activated in N_2 at 600 °C for 12 h. Wafers then followed a standard back-end processing to form the contact pads, and received a plasma treatment at 250 °C in NH_3 for 1 h before measurements.

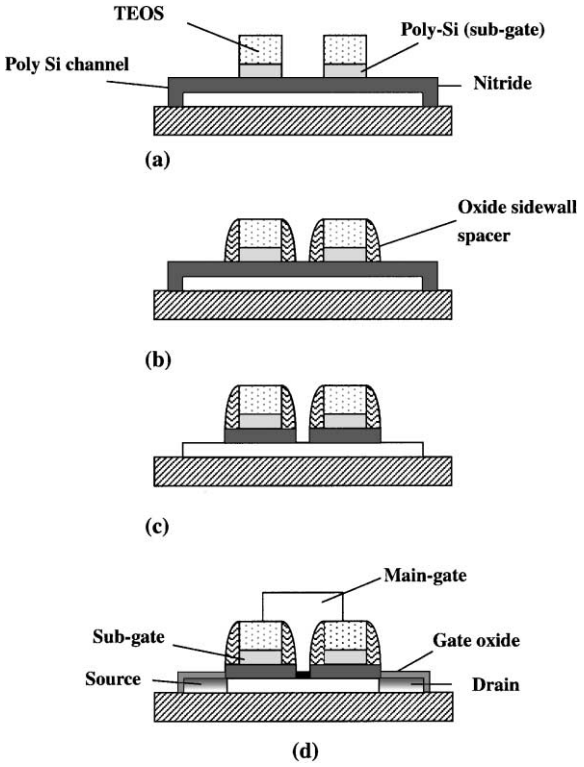

Fig. 1. Key process flow for TFT with top sub-gate.

2.2. Fabrication of SAFID TFT with bottom sub-gate

Briefly, a 100 nm highly doped poly-Si layer was first deposited on an oxidized silicon substrate by low pressure chemical vapor deposition (LPCVD). The doped poly-Si film was then patterned to form individual sub-gate (or field plates). Next, a 100 nm CVD nitride was deposited by LPCVD (Fig. 2(a)), followed by the deposition of a thick LPTEOS (550 nm) oxide layer. Chemical mechanical polishing (CMP) was then applied to planarize the wafer surface and expose the nitride layer on top of the sub-gate (Fig. 2(b)). It should be noted here that the nitride layer serves not only as the isolating dielectric between the field plate (i.e., sub-gate) and the active device layer in the final device structure, it also serves as a stopping layer to enhance process control during CMP polishing. Afterwards, a 50 nm CVD amorphous thin Si film was deposited at 550 °C, and transformed into polycrystalline phase by a SPC at 600 °C for 24 h (Fig. 2(c)) to serve as the active device layer. A 20 nm CVD oxide layer was then deposited to form the gate insulator. A third poly-Si film was deposited and patterned to form the top-gate, followed by the formation of a self-aligned sidewall. Finally, self-aligned source/drain regions were formed by a heavy-dose implant (Fig. 2(d)). For n-channel transistors, As^+ implant

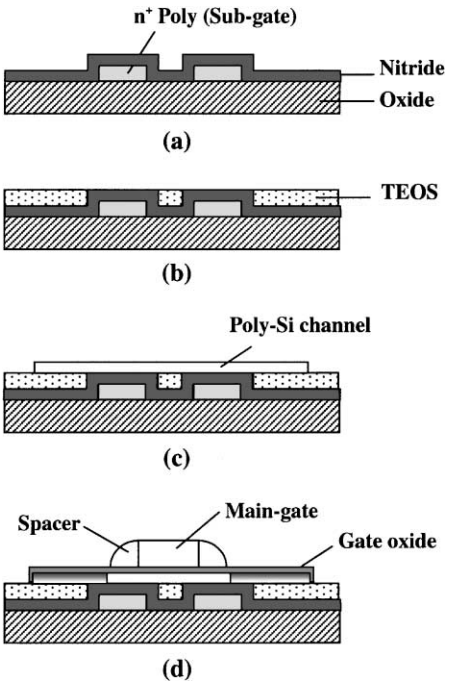

Fig. 2. Key process flow for SAFID TFT with bottom sub-gate.

with a dosage of 5×10^{15} cm^{-2} at 20 keV was used. The implanted dopants were subsequently activated in N_2 at 600 °C for 12 h. Wafers then followed a standard back-end processing to form the contact pads, and received a plasma treatment at 250 °C in NH_3 for 1 h before measurements. Poly TFTs with conventional structure (e.g., without the sub-gate) were also fabricated alongside to serve as the control.

3. Results and discussion

Fig. 3 shows typical subthreshold characteristics of the SAFID TFT devices with a bottom sub-gate bias of 40 V and a drain bias of 15 V. Well-behaved transfer characteristics and high on/off current ratio ($\sim 10^7$) are achieved in the SAFID TFT. As shown in Fig. 4, the off-state current of the SAFID TFT is much lower than that of the conventional TFT control. Specifically, the leakage current of SAFID TFT is 10 times smaller at $V_G = 0$ V and 100 times smaller at $V_G = -5$ V, compared to the conventional TFT control. This is because, under identical gate bias, the FID induced by the sub-gate could effectively reduce the peak field near the drain region, thus reducing the off-state leakage while maintaining a current drive capability comparable to that of the conventional TFT.

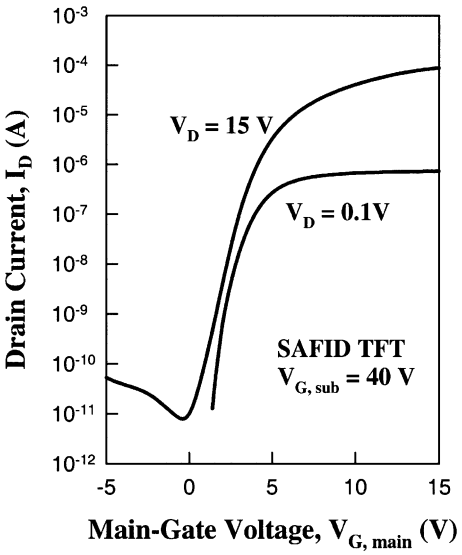

Fig. 3. Subthreshold characteristics of the SAFID TFT. L/W of the device is 2 μm/10 μm.

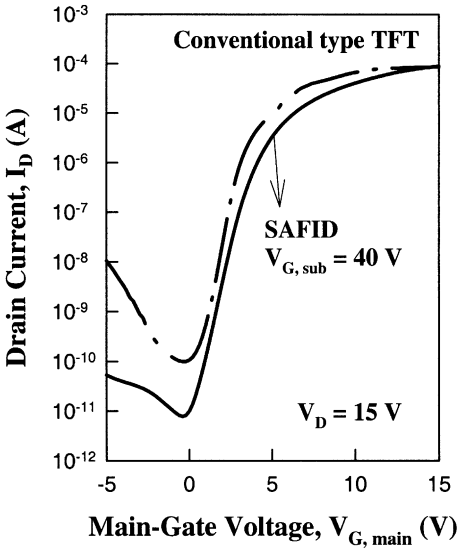

Fig. 4. Comparison of subthreshold characteristics between SAFID and conventional TFT devices. $L/W = 2$ μm/10 μm.

The important roles of the bottom sub-gate bias on the device operation are illustrated in Fig. 5. It can be seen that even by applying a proper main-gate bias, the SAFID TFT still cannot be effectively turned on with zero sub-gate bias. This is because under such condition, the field-induced source and drain are not formed, and thus the switching behavior of the device is prohibited. It is interesting to note here that the leakage current at negative main-gate voltage region can even be lowered

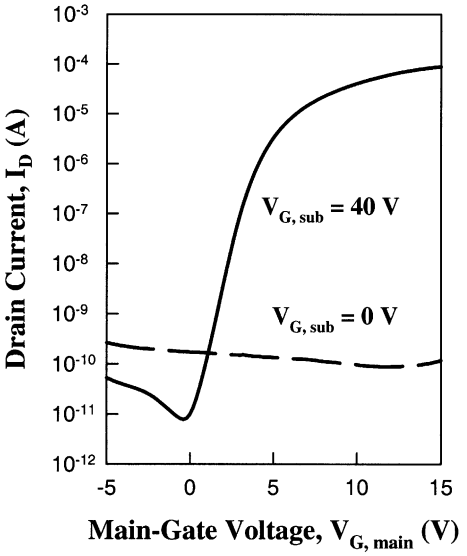

Fig. 5. Effects of the bottom sub-gate bias on the transfer characteristics of SAFID TFT.

when the sub-gate bias is applied. The cause of this phenomenon is still not very clear at this moment, and is presumably related to defects present at the channel/nitride interface induced during CMP processing.

A comparison between the transfer characteristics of the device with top and bottom sub-gate is shown in Fig. 6. Note that the $V_{G,sub}$ applied on the device with top sub-gate is 15 V, which is lower than that with bottom sub-gate (i.e., 30 V), accounting for the different nitride thickness used in the two cases. It is seen that that the top sub-gate device exhibits poorer performance. This is ascribed to the high resistive channel regions underneath the inner spacer (see Fig. 7), resulting in degraded on-current.

4. Conclusions

We have proposed and successfully demonstrated two self-aligned TFT processes that allow the realization of field-induced drain structures. The first one features a bottom sub-gate (or field plate), and a top self-aligned sidewall spacer is used for setting the effective length of the FID region. While the other one features a top sub-gate that allows the main-gate to be self-aligned to the sub-gate. These new structures, unlike previous versions of TFTs with FID, are therefore not susceptible to photomasking misalignment errors. Excellent on/off current ratio has been successfully demonstrated for TFTs with bottom sub-gate. The top sub-gate scheme, however, exhibits poor device performance, which is

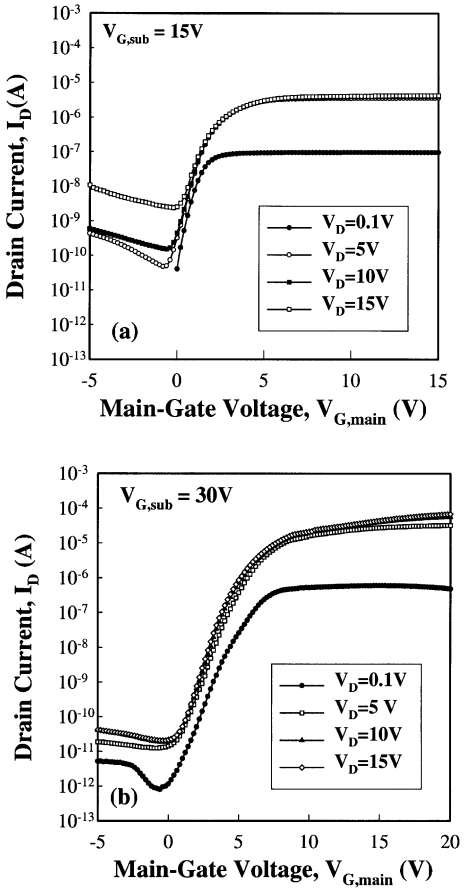

Fig. 6. Comparison of subthreshold characteristics between TFTs with (a) top sub-gate and (b) bottom sub-gate. L/W = 2 μm/10 μm.

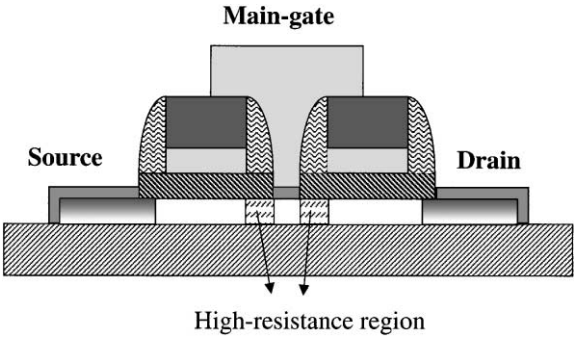

Fig. 7. Cross-sectional view of a TFT with top sub-gate showing the high-resistance channel regions directly underneath the inner spacers.

ascribed to the introduction of high parasitic resistance in the channel region directly underneath the inner spacers.

Acknowledgements

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