



Impact of nitrogen and/or fluorine implantation on deep-submicron Co–silicide process

T.Y. Chang^{a,*}, T.F. Lei^a, T.S. Chao^b, S.W. Chen^a, L.M. Kao^a, S.K. Chen^c,
A. Tuan^c, T.P. Su^d

^a Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, 1001-1 Ta Hsueh Road, Hsinchu, Taiwan

^b National Nano Device Laboratory, 1001-1 Ta Hsueh Road, Hsinchu, Taiwan

^c Air Products Asia, Taipei, Taiwan

^d San Fu Co. Ltd., Hsinchu, Taiwan

Received 30 July 2001; received in revised form 2 October 2001; accepted 2 January 2002

Abstract

In our previous study, using NF_3 annealed poly-Si to improve gate oxide integrity for Co–silicide process has been proposed [SSDM, 1998, p. 164]. It is very interesting and important to know the mechanism of both F and N incorporation in the SiO_2 and Co–silicide. In this study, F and/or N will be implanted into poly-Si with/without Co–silicide process, to identify the interaction of N and F in the SiO_2 and Co–silicide process. In our work, we will describe the optimized structure and F/N incorporation for Co–silicide process. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: Gate oxide integrity (GOI); Co–silicide; Fluorine and nitrogen implantation; Leakage performance; Breakdown charge and stress induce leakage current (SILC)

1. Introduction

In deep-submicron CMOS devices, reduction of gate, source and drain parasitic resistance without a junction leakage problem is a key issue [2,3]. The conventional Ti–silicide process does not lead to significant junction leakage, but it is difficult to achieve a low gate resistance in narrow regions. The Co–silicide process is an attractive alternative to the Ti–silicide process due to its relatively linewidth-independent sheet resistance [2]. This is because the transformation of the crystal phase from high resistivity C49 to low resistivity C54 is hard. However, the Co–silicide process has a high leakage problem, which is a result of non-uniform CoSi_2/Si interface or Co spiking [4,5]. CoSi_x spikes of abnormal growth under the Co–silicide film are found to be the

origin of the localized leakage currents. These CoSi_x spikes grow rapidly at annealing temperatures between 400 and 450 °C for 30 s when the Co_2Si is formed, and drastically dissipate while annealing between 800 and 850 °C for 30 s [6]. Another problem is its irreproducible yield on narrow lines, partly attributed to a silicide thinning effect at the edge of the silicide lines. It is found that the thickness of Co–silicide on the LOCOS edge is reduced due to the water contamination from the field oxide [7].

On the other hand, reliability of the gate oxide becomes more stringent than ever before as the device size scales down to the deep-submicron level. Current leakage will become a critical factor for the scaling down of the gate oxide thickness for the deep-submicron device, especially for the low field leakage current before F–N tunneling. It has reported that the reliability of MOS capacitors can be improved by introducing minute amounts of fluorine in thermal oxide [8]. Using nitrogen implant through a poly-Si gate MOS structure to improve thin-gate characteristics has also been proposed

* Corresponding author. Tel.: +886-3-5712121; fax: +886-3-5724361.

E-mail address: panda.ee86g@nctu.edu.tw (T.Y. Chang).

[9]. In a previous study, we have demonstrated a novel technique, using NF_3 annealing poly-Si gate, to incorporate both F and N to improve the gate oxide integrity [1]. In this work, fluorine and/or nitrogen will be implanted into poly-Si to identify the mechanism of both F and N incorporation in the SiO_2 and Co-salicide.

2. Experimental

MOS capacitors were fabricated on (100) oriented p-type Si wafer. First, a field oxide with a thickness about 550–600 nm was thermally grown on the silicon wafer by wet oxidation at 1100 °C for 50 min. The active areas were then defined by photolithography and wet-chemical-etched by BOE (buffered oxide etcher) solution. After the standard RCA cleaning process, the gate oxide with 4.5 nm thickness was formed in dry oxidation furnace at 900 °C in diluted O_2 gas ($\text{N}_2:\text{O}_2 = 10:1$). The poly-gate was deposited by low-pressure chemical vapor deposition (LPCVD) and then different fluorine and/or nitrogen amounts were implanted. Arsenic ion implantation (40 keV, 2×10^{15}) was used to reduce gate resistance and a 1000 °C 30 s RTA process for impurity activation. Following activation, the poly-gate regions were defined by the photolithography and wet-etched solution. The thickness of Co film was 20 nm and a Mo film of about 20 nm was deposited on the Co film by electron-beam evaporation system at the same time. The Mo film was used to prevent the oxidation of Co by O_2 . A two-step annealing process was used for silicidation. During the first step annealing, the Co film selectively reacted with the exposed poly-Si at 550 °C for 30 min in a dry N_2 furnace to form CoSi. After selective etching off the unreacted Co and Mo films, the samples were annealed in the second step annealing at 850 °C for 30 min to form CoSi_2 . The solution for etching Mo was $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ in the ratio of 1:1:5, and the solution for etching Co was $\text{HCl} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ in the ratio of 1:1:6 at 75–85 °C.

3. Results and discussion

The use of NF_3 annealed poly-gate to improve oxide quality for Co-salicide process has been reported. Fig. 1 shows the distribution of the leakage current at 2 V for different NF_3 annealing times. It is found that the leakage current of oxide with NF_3 annealing is significantly reduced. It is suggested that both N and F species can simultaneously neutralize the dangling bonds in the oxide. We believe the leakage paths, dominated by assistance of interface traps, can be effectively suppressed by the N and F incorporation at the interface using NF_3 annealing. However, it would be interesting for us to understand which the dominating mechanism between

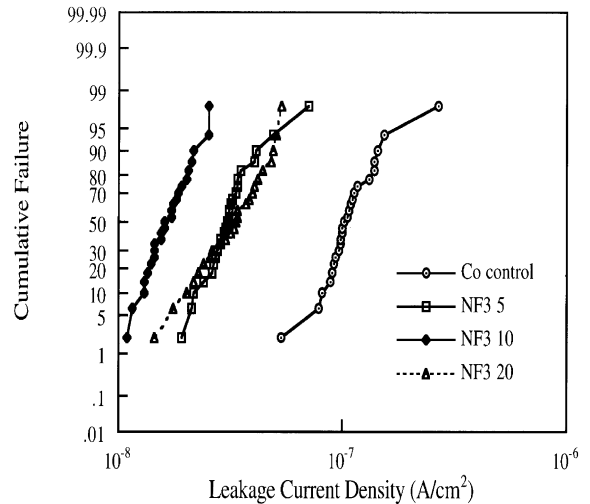


Fig. 1. The distribution of leakage current at 2 V for different NF_3 annealing times.

Si–N and Si–F in improving oxide integrity is. In this work, fluorine and/or nitrogen will be implanted into poly-Si by Co-salicide process to identify the mechanism of both F and N incorporation in the SiO_2 and Co-salicide.

The breakdown field distribution of different fluorine implantations is shown in Fig. 2. It is found that the fluorine implantation seems to have no effect on gate oxide breakdown field. Fig. 3 illustrates the breakdown field distribution of different nitrogen implantations. Nitrogen implantation would cause slight degradation

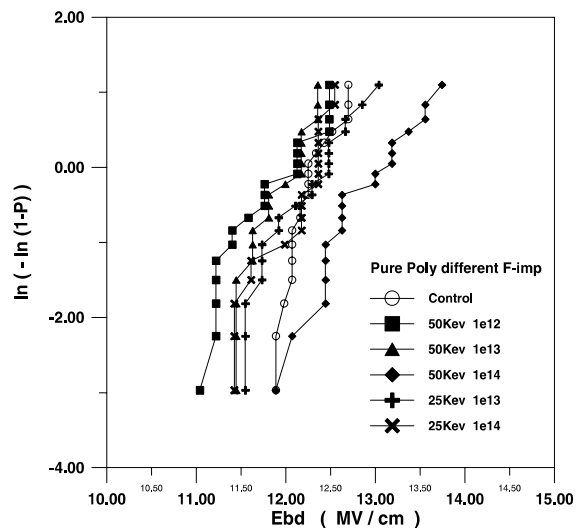


Fig. 2. Breakdown field distribution of different fluorine implantations.

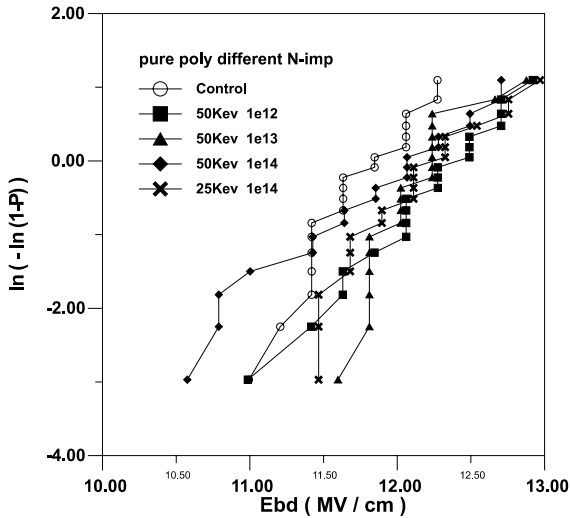


Fig. 3. Breakdown field distribution of different nitrogen implantations.

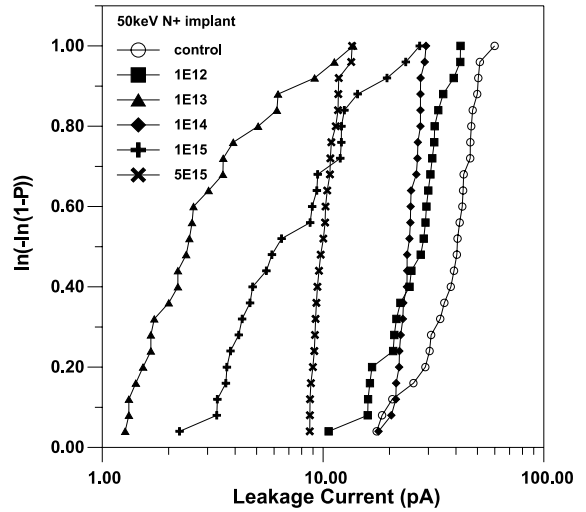


Fig. 5. The leakage current distribution of different nitrogen implantations.

of oxide breakdown field. The fluorine or nitrogen implantation could not better the oxide breakdown field.

The Weibull distribution plots of low field leakage determined by testing 25 samples of different fluorine implantation are shown in Fig. 4. The leakage performance of low dosage fluorine implantations is better than that of higher dosages. Furthermore, it is found that implantation with low energy would cause leakage problems. From this information, it is clear that fluorine implantation at low dosages with high energy is the optimized condition. Fig. 5 presents the Weibull distribution plots of low field leakage for different nitrogen

implanted samples. Similar to the fluorine implantation, the leakage performance of lower nitrogen implantation is better than that of the higher. There seems to be an optimum condition to improve low field leakage.

Charge-to-breakdown, measured under constant current stress in Fowler–Nordheim tunneling region, is a good way to determine the reliability of gate oxide. The breakdown charge is determined by constant current density (-100 mA/cm^2) multiplied by the time to breakdown. The Weibull plots of charge-to-breakdown for different fluorine implantations are presented in Fig. 6. As the implanted energy and density increase, the

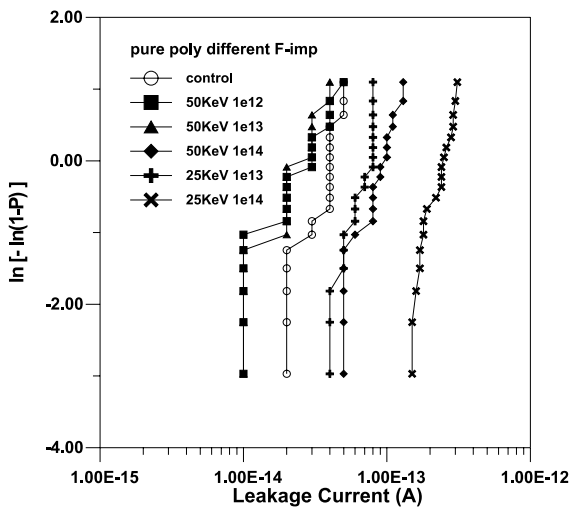


Fig. 4. The leakage current distribution of different fluorine implantations.

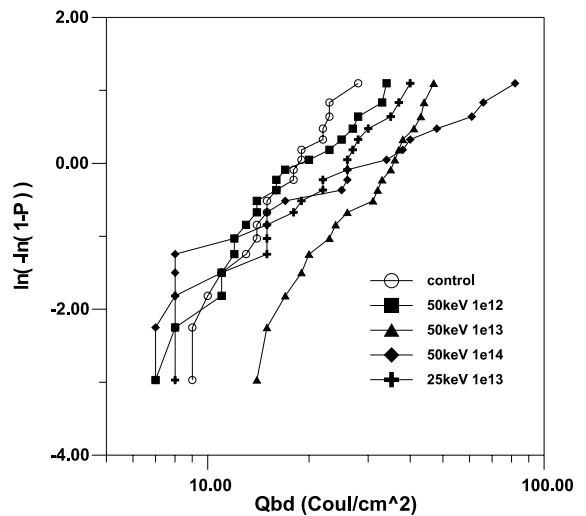


Fig. 6. The Weibull plots of charge-to-breakdown for different fluorine implantations.

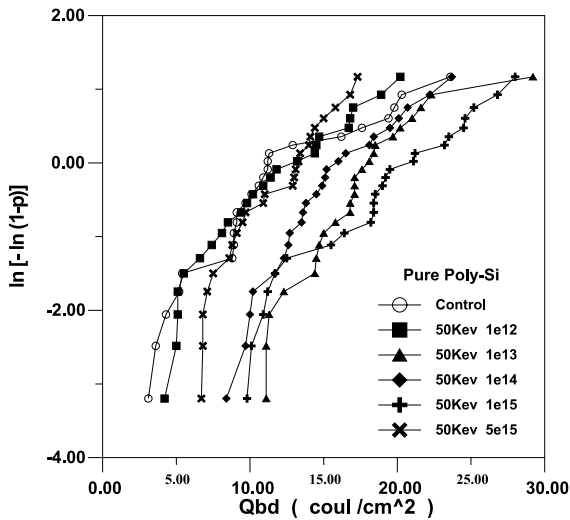


Fig. 7. The Weibull plots of charge-to-breakdown for different nitrogen implantations.

breakdown charge is larger. It is usually thought that the dangling bonds at the Si/SiO₂ interface are terminated by fluorine incorporation, leading to lower interface traps. Moreover, Si-F is a stronger bond, thus improving oxide integrity and Si-F would alleviate the local stress at poly-Si/oxide interface. Fig. 7 show the Weibull plots of charge-to-breakdown for different nitrogen implantations. It is found that implantation with higher dosages would improve breakdown charge, but becomes worse above a critical point. It is suggested that oxide breakdown results from either oxide weak spots or electric field enhancement due to electron and hole trap. The

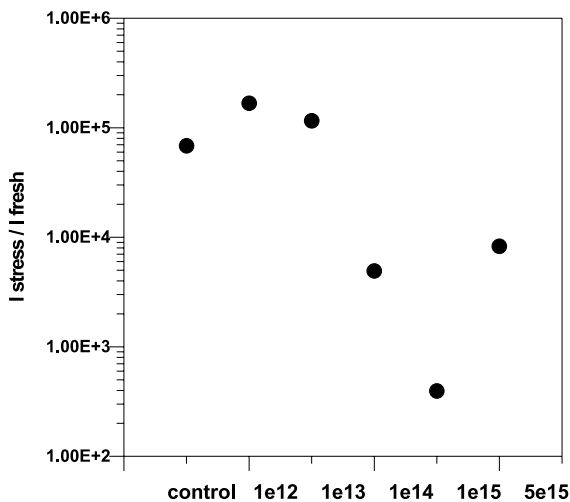


Fig. 8. The ratio of SILC to fresh current for different fluorine implanted conditions.

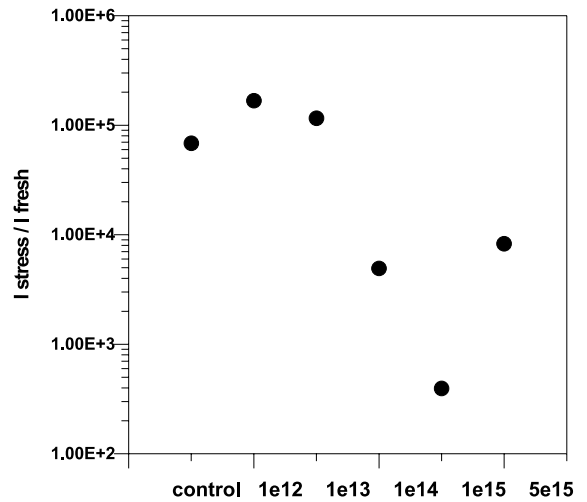


Fig. 9. The ratio of SILC to fresh current for different nitrogen implanted conditions.

nitrogen-rich layer near the Si/SiO₂ interface in the gate oxide, which reduces charge trapping rate and weak oxide spots by replacing strained Si-O bonds with Si-N bonds, results in improving the charge-to-breakdown. Therefore, redundant fluorine or nitrogen implantation would arouse extra traps and degrade oxide breakdown charge. To compare with stress induce leakage current (SILC) phenomenon, constant charge density (-1 C/cm^2) was applied to each sample. It is found that the fluorine doping would effectively reduce SILC effect but excessive fluorine introduces degradation (Fig. 8). Correspondingly, nitrogen doping could suppress SILC effect but redundant nitrogen also increases SILC (Fig. 9).

4. Conclusions

From the results above, it is found that both fluorine and nitrogen implantation could improve the electrical characteristics of Co-salicide process but excessive dosages would cause degradation. The optimized condition for fluorine implantation is $1 \times 10^{13} \text{ cm}^{-2}$ with energy 50 keV. And the optimized nitrogen implanted condition is also $1 \times 10^{13} \text{ cm}^{-2}$ with energy 50 keV. Both nitrogen and fluorine implantation could improve electric characteristics of Co-salicide process, but it needs to be optimized.

Acknowledgements

This work was supported in part by the National Science Council under contract number NSC-89-2215-E-009-095. The authors are grateful to the staff of NDL

for their kind assistance and support during the course of this work.

References

- [1] Chang TY, Lei TF, Chou TS, Lin HC, Huang TY, Chen SK, et al. In: SSDM, 1998. p. 164–5.
- [2] Yamazaki T et al. 21 ps switching 0.1- μm -CMOS at room temperature using high performance Co salicide process. IEDM Tech Dig 1993:906–9.
- [3] Goto K et al. Optimization of salicide process for 0.1 μm CMOS device. In: Symposium on VLSI Technology, 1994. p. 119–20.
- [4] Pfister JR, Mele TC, Limb Y, Jones RE, Woo M, Boeck B, et al. A cobalt salicide CMOS process with TiN-strapped polysilicon gates. *IEEE Electron Dev Lett* 1991;12:350–2.
- [5] Goto K et al. Leakage mechanism and optimized conditions of Co salicide process for deep-submicron CMOS device. *IEDM* 1995:449–52.
- [6] Goto K et al. A new leakage mechanism of Co salicide and optimized process conditions. *IEEE Trans Elec Dev* 1999;46:117–24.
- [7] Maex K et al. Self-aligned CoSi_2 for 0.18 μm and below. *IEEE Trans Electron Dev* 1999;46:1545–50.
- [8] Nishioka Y et al. Hot-electron hardened Si-gate MOSFET utilizing F implantation. *IEEE Electron Dev Lett* 1989: 141–3.
- [9] Hwang H, Ting W, Kwong D-L, Lee J. Improved reliability characteristics of submicronmeter nMOSFETS with oxynitride gate dielectric prepared by rapid thermal oxidation in N_2O . *IEEE Electron Dev Lett* 1991;12:495–7.