Formation of Ni Germano-Silicide on Single Crystalline $Si_{0.3}Ge_{0.7}/Si$

C. Y. Lin, W. J. Chen, C. H. Lai, Albert Chin, Senior Member, IEEE, and J. Liu

Abstract—We have studied the Ni and Co germano-silicide on Si_{0.3}Ge_{0.7}/Si. The Ni germano-silicide shows a low sheet resistance of 4–6 Ω/\Box on both P⁺N and N⁺P junctions, which is much smaller than Co germano-silicide. In addition, small junction leakage currents of 3×10^{-8} A/cm² and 2×10^{-7} A/cm² are obtained for Ni germano-silicide on P⁺N and N⁺P junctions, respectively. The good germano-silicide integrity is due to the relatively uniform thickness as observed by cross-sectional TEM.

Index Terms-Co, Ni, SiGe, silicide.

I. INTRODUCTION

S continuously scaling down the VLSI technology, SiGe becomes more important because of its superior electrical property as compared with Si. The smaller hole effective mass and higher hole mobility are particularly important for improving the current p-MOSFET [1]-[3] and for high-k gate dielectric integration [4]–[7]. Using the high temperature stable SiGe formed by solid-phase epitaxy, ultrathin gate oxide grown on SiGe can achieve comparable integrity with that on Si and the same time achieving ~ 2 times hole mobility improvement [1]–[3]. However, to integrate SiGe p-MOSFET into current VLSI process, high quality silicide [9]-[12] on SiGe is unavoidable. Unfortunately, little study of germano-silicide on single crystalline SiGe can be found in the literature, which may be due to the strong agglomeration [8] at high temperatures. In this study, we have investigated Co and Ni as the silicidation species on SiGe/Si with Ge content as high as 70%. The Ni germano-silicide shows the small sheet resistance of 4–6 Ω/\Box on both N^+P and P^+N junctions, which is much smaller than Co germano-silicide. Small junction leakage currents less than 3×10^{-8} A/cm² and 2×10^{-7} A/cm² are obtained for Ni germano-silicide on respective P^+N and N^+P junctions. The good Ni germano-silicide integrity is due to the relatively uniform thickness as observed by cross-sectional TEM. The achieved good germano-silicide make a further step toward realizing SiGe p-MOSFET for manufacturing.

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Fig. 1. XRD and electron diffraction patterns of $\rm Si_{0.3}Ge_{0.7}$ after ion implantation and post annealing.

II. EXPERIMENTAL

Standard 4-in p- and n-type Si wafers were used in this study. After device isolation, the $\sim 20 \text{ nm Si}_{0.3}\text{Ge}_{0.7}$ is selectively formed in active area by solid phase epitaxy. Although the SiGe layer was consumed after germano-silicidation, the SiGe under the gate oxide is unaffected and the mobility of p-MOSFET is still enhanced by the SiGe channel [1]-[3], [13]. Therefore, better p-MOSFET performance will be expected as long as the source-drain junction leakage current is low. Then 10 KeV B⁺ or 50 KeV As⁺ implantation is performed on the respective nor p-type Si_{0.3}Ge_{0.7}/Si wafers followed by 900–950 °C and 30-60 s RTA for defect reduction and junction formation. The good single crystalline Si_{0.3}Ge_{0.7} after implantation and RTA are confirmed by X-ray diffraction (XRD) and electron diffraction measurements shown in Fig. 1. The high temperature stable SiGe after implantation annealing is an important merit of our developed SiGe that is also formed at high temperatures by solid-phase epitaxy [1]–[3]. Then 10 nm Co or 12 nm Ni was deposited and the deposited metal thickness was carefully calibrated by cross-sectional TEM. For Co germano-silicide, the first step silicidation was performed at 500 °C for 30 s and the second phase transformation was excused at 750 to 1000 °C by RTA [9]–[12]. For Ni germano-silicide, only one-step RTA at 350-700 °C for 30 s was performed. The formed germanosilicide and junction diode were characterized by sheet resistance and leakage current measurements, where the diode area is $700 \times 400 \,\mu\text{m}^2$. The structure property of germano-silicide is investigated by cross-sectional TEM.

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Fig. 2. Sheet resistance comparison of Co and Ni germano-silicide on (a) P^+N and (b) N^+P Si_{0.3}Ge_{0.7}/Si. The inserted figure is the XRD pattern of Ni germano-silicide.

III. RESULTS AND DISCUSSION

Fig. 2(a) and 2(b) show the sheet resistance of Ni and Co germano-silicide on P⁺N and N⁺P Si_{0.3}Ge_{0.7}/Si junctions, respectively. The Ni germano-silicide exhibits superior sheet resistance than Co germano-silicide and low sheet resistance of 6 Ω/\Box and 4 Ω/\Box are achieved on respective P⁺N and N⁺P junctions. From the XRD pattern inserted in Fig. 2(a), the formed phase is mono-germano-silicide that is the reason to achieve such low sheet resistance. Besides, the measured sheet resistance is very close to the results of Ni germano-silicide on poly crystalline Si_{0.8}Ge_{0.2} [8]. The obtained low sheet resistance from 400 to 600 °C suggests Ni germano-silicide have good thermal stability and large process margin over this temperature range.

We have used cross-sectional TEM to study the structure property of formed germano-silicide. Fig. 3(a) and 3(b) show the Ni and Co germano-silicide formed at 500 and 900 °C on N⁺/P Si_{0.3}Ge_{0.7}/Si junction, respectively. A relatively uniform thickness and smooth surface of Ni germano-silicide is observed, which explains the measured good sheet resistance shown previously in Fig. 1. In contrast, much rougher thickness



(a)



Fig. 3. Cross-sectional TEM of (a) Ni and (b) Co germano-silicide on N^+P Si_{0.3}Ge_{0.7}/Si.

and strong agglomeration are observed in Co germano-silicide that gives the higher sheet resistance. The possible reason may be due to the required higher silicidation temperature used for Co germano-silicide.

We have further studied the junction characteristics of Ni germano-silicide. Figs. 4(a) and 4(b) show the junction leakage current of Ni germano-silicide on P+N and N+P Si_{0.3}Ge_{0.7}/Si junctions, respectively. The leakage current of P+N Ni germano-silicide junction decreases as silicidation temperature increasing from 300 to 500 °C and a minimum leakage current of $< 3 \times 10^{-8}$ A/cm² is obtained at 500 °C formation temperature. Slightly raise of leakage current was then found with the increasing silicidation temperature. The leakage current of N⁺P Ni germano-silicide junction shows the similar trend of temperature dependence to P+N junction, but a slightly higher minimum leakage current of $< 2 \times 10^{-7} \text{ A/cm}^2$ is obtained at 600 °C. The drastically increase of leakage current at 700 °C may be due to the strong agglomeration at higher temperatures, which is also consistent with the rapid increasing sheet resistance at this temperature shown in Fig. 2.



(b)

Fig. 4. Junction leakage current of Ni germano-silicide on (a) P+N and (b) N^+P Si_{0.3}Ge_{0.7}/Si.

IV. CONCLUSION

Ni and Co germano-silicides on Si_{0.3}Ge_{0.7}/Si were studied and Ni germano-silicide shows superior sheet resistance than Co germano-silicide. Low sheet resistance of 4–6 Ω/\Box is obtained on both P⁺N and N⁺P Si_{0.3}Ge_{0.7}/Si and small junction leakage currents of $< 3 \times 10^{-8}$ and 2×10^{-7} A/cm² are measured on respective junctions. The developed good Ni germano-silicide is important for SiGe p-MOSFETs.

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REFERENCES

- Y. H. Wu and A. Chin, "High temperature formed SiGe p-MOSFETs with good device characteristics," *IEEE Electron Device Lett.*, vol. 21, pp. 350–352, July 2000.
- [2] Y. H. Wu, A. Chin, and W. J. Chen, "Thickness dependent gate oxide quality of thin thermal oxide grown on high temperature formed SiGe," *IEEE Electron Device Lett.*, vol. 21, pp. 289–292, June 2000.
- [3] Y. H. Wu and A. Chin, "Gate oxide integrity of thermal oxide grown on high temperature formed Si_{0.3}Ge_{0.7}," *IEEE Electron Device Lett.*, vol. 21, pp. 113–115, Mar. 2000.
- [4] S. J. Lee, H. F. Luan, C. H. Lee, T. S. Jeon, W. P. Bai, Y. Senzaki, D. Roberts, and D. L. Kwong, "Performance and reliability of ultra thin CVD HfO₂ gate dielectrics with dual poly-Si gate electrodes," in *VLSI Tech. Dig.*, 2001, pp. 133–134.
- [5] X. Guo, X. Wang, Z. Luo, T. P. Ma, and T. Tamagawa, "High quality ultra-thin (1.5 nm) TiO₂-Si₃N₄ gate dielectric for deep sub-micron CMOS technology," in *IEDM Tech. Dig.*, 1999, pp. 137–140.
- [6] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, "Device and reliability of high-K Al₂O₃ gate dielectric with good mobility and low D_{it}," in VLSI Tech. Dig., 1999, pp. 135–136.
- [7] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality La₂O₃ and Al₂O₃ gate dielectrics with equivalent oxide thickness 5–10 Å," in *VLSI Tech. Dig.*, 2000, pp. 16–17.
- [8] J. H. Ku, C. J. Choi, S. Song, S. Choi, H. Fujuhara, H. K. Kang, and S. I. Lee, "High performance pMOSFETs with Ni(Si_xGe_{i-x})/Poly-Si_{0.8}Ge_{0.2} gate," in *VLSI Tech. Dig.*, 2000, pp. 114–115.
- [9] C. P. Chao, K. E. Violette, S. Unnikrishnan, M. Nandakumar, R. L. Wise, J. A. Kittl, Q. Z. Hong, and I. C. Chen, "Low resistance Ti or Co salicided raised source/drain transistors for sub 0.13 μm CMOS technology," in *IEDM Tech. Dig.*, 1997, pp. 103–106.
- [10] Q. Z. Hong, W. T. Shiau, H. Yang, J. A. Kittl, C. P. Chao, H. L. Tsai, S. Krishnan, I. C. Chen, and R. H. Havemann, "CoSi₂ with low diode leakage and low sheet resistance at 0.065 μm gate length," in *IEDM Tech. Dig.*, 1997, pp. 107–110.
- [11] Q. Xiang, C. Woo, E. Paton, J. Foster, B. Yu, and M. R. Lin, "Deep sub-100 nm CMOS with ultra low gate sheet resistance by NiSi," in *VLSI Tech. Dig.*, 2000, pp. 76–77.
- [12] Y. H. Wu, W. J. Chen, S. L. Chang, A. Chin, S. Gwo, and C. Tsai, "Improved electrical characteristics of CoSi₂ using HF-vapor pretreatment," *IEEE Electron Device Lett.*, vol. 20, pp. 320–322, July 1999.
- [13] Y. Taur and T. K. Ning, Fundamentals of Modern VLSI Devices. Cambridge, U.K.: Cambridge Univ. Press, 1998, p. 196.