# Impacts of Gate Structure on Dynamic Threshold SOI nMOSFETs

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***Abstract*—The effects of different substrate-contact structures (T-gate and H-gate) dynamic threshold voltage silicon-on-insulator (SOI) nMOSFETs (DTMOS) have been investigated. It is found that H-gate structure devices have higher driving current than T-gate under DTMOS-mode operation. This is because H-gate SOI devices have larger body effect factor ($\gamma$), inducing a lager reduction of threshold voltage. Besides, it is found that drain-induced-barrier-lowering (DIBL) is dramatically reduced for both T-gate and H-gate structure devices when devices are operated under DTMOS-mode.**

***Index Terms*—Dynamic threshold MOS (DTMOS), H-gate, silicon-on-insulator (SOI), T-gate.**

## I. Introduction

SILICON-ON-INSULATOR (SOI) devices are greatly competitive for the ULSI era due to the significantly improved electrical properties compared with bulk devices, especially for high-speed and low-voltage/power applications [1]. The most important feature that establishes the SOI technology as a strong option for next generation of ULSI circuits is that it provides perfect isolation between individual device cells. However, for partially depleted (PD) SOI devices, it has the floating body effects which are due to instability of body potential because of the insulation between SOI layer and the silicon substrate by buried oxide [2]. In this letter, we use T-gate and H-gate structures (which is one side substrate contact and two sides substrate contacts, respectively) to improve this drawback [3], [4]. Besides, to improve the current drive capability of MOSFETs at low supply voltage (e.g., $V_d < 0.7$ V and below), the conception of dynamic threshold MOS (DTMOS) [5]–[10] for ultralow voltage applications. By shorting the gate to body, the threshold voltage of the device is a function of its gate voltage, i.e., as the gate voltage increases, the threshold voltage drops while the device exhibits the normal threshold voltage in the off-state to maintain a low standby power. To the best of our knowledge, the impacts of gate structure on SOI DTMOS have never been reported in detail. In the present paper we report, for the first time, the comparisons of SOI DTMOS with different substrate-contact structures.

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## II. Experimental

$N^+$ poly-Si gate n-channel MOSFETs were fabricated using boron doped $\langle 100 \rangle$-oriented separation by implanted oxygen (SIMOX) wafers with top silicon thickness $T_{\rm si}$ ranging from 140–190 nm. The buried oxide thickness was 400 nm. Local oxidation of silicon (LOCOS) was performed to fully consume the active silicon layer in the isolation region. Channel implant was performed by $BF_2^+$ (50 keV, $6 \times 10^{12}$ cm$^{-2}$), followed by the growth of a 4-nm gate oxide at 800 °C with *in-situ* HF-vapor cleaning. Afterwards, a 200 nm poly-Si layer was deposited, patterned, and etched to form the transistor gates. A shallow $N^+$ S/D extension implant with As (5 keV, $1 \times 10^{15}$ cm$^{-2}$) was then performed, followed by the formation of a low pressure CVD (LPCVD) TEOS spacer. Then, an As implant at 10 keV with a dose of $5 \times 10^{15}$ cm$^{-2}$ was performed to form the $n^+$-doped source/drain regions. After the deposition of passivation oxide and contact formation, wafers received a rapid thermal annealing (RTA) at 1000 °C for 10 s. Wafers were then processed through a standard backend flow through metallization. Finally, wafers were sintered at 400 °C for 30 min in forming gas.

## III. Results and Discussion

Fig. 1(b) shows the reduction of threshold voltage operated in standard MOSFET mode changes to DTMOS mode of T-gate and H-gate devices (as shown in the Fig. 1(a)). The channel width are 100 $\mu$m. The threshold voltage is measured at $V_D =$ 100 mV at the intercept point on the $V_G$ axis of the $I_d$ versus $V_G$ curve extrapolated from the point of maximum slope. Here $\Delta V_{\rm th}$ is the threshold voltage in MOSFET mode minus the threshold voltage in DTMOS mode. It is worthy to note here that the H-gate structure device (empty circle) has larger threshold voltage reduction than T-gate (solid circle) counterpart. In order to explain this phenomenon, we now consider DTMOS mode. Since the gate is tied to body, namely, the body-to-source junction is "forward biased," the equation of threshold voltage reduction is

$$\Delta V_t = \gamma[(2\psi_B)^{1/2} - (2\psi B - V_{\rm BS})^{1/2}] \quad (1)$$

where $\gamma$ is body-effect factor and equal to $\mathbf{(2\epsilon_S q N_A)1/2/C_{OX}}$. From (1), at the same bias $V_{\rm BS}$, the threshold voltage reduction increases as the value of $\gamma$ increases. The H-gate device has lager value of $\gamma$ (for Si film thickness $=$ 140 nm with $L = 0.35$ $\mu$m, $\gamma$ are 0.376, and 0.286 for H- and T-gate devices, respectively). This can explain why H-gate device has a larger reduction of threshold voltage.

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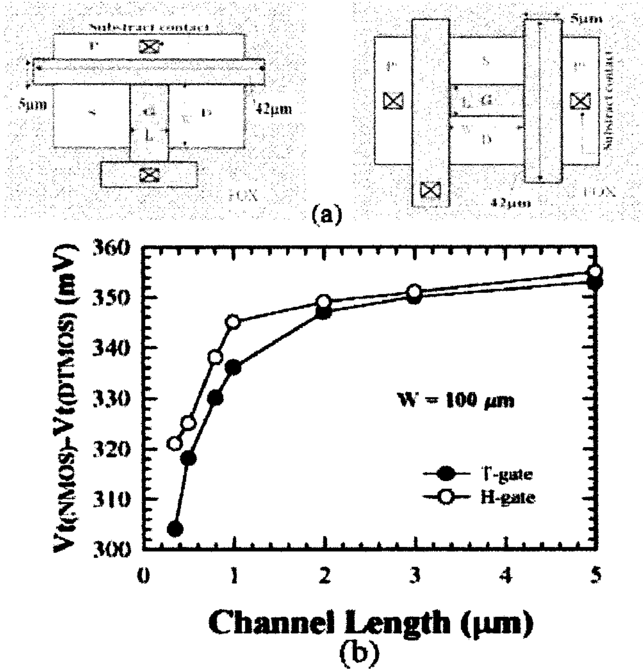


Fig. 1. (a) Structures of T-gate (left) and H-gate (right) with channel width = 100 $\mu$m. (b) Reduction of $V_t$ operated in MOSFET mode changes to DTMOS mode.

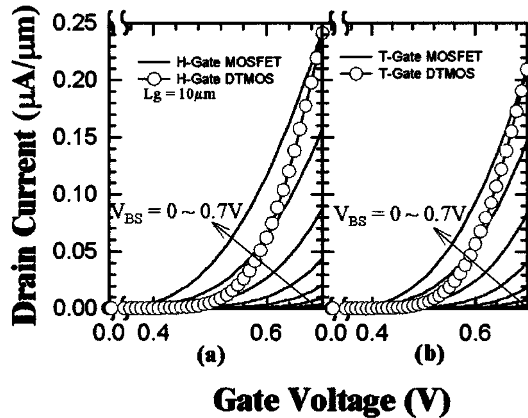


Fig. 2. Drain current versus gate voltage for (a) H-gate (b) T-gate under MOSFET and DTMOS modes.

Fig. 2 shows the drain current versus gate voltage for H-gate and T-gate under MOSFET mode (with different substrate bias, $V_{\rm BS}$) and DTMOS mode. For both H-gate and T-gate, it is quite obvious that devices under DTMOS mode operation can get better subthreshold swing characteristics than conventional MOSFET-mode operation. Besides, comparing H-gate with T-gate devices, we can see that the H-gate devices show higher saturation drain current than the T-gate ones. Regarding the [6], saturation drain current, for long channel

$$I_{D(\rm SAT)} \propto (V_g - V_t)^2. \tag{2}$$

One can get large saturation current if $V_t$ is decreased significantly. As measured in Fig. 1, H-gate exhibits an increased $\gamma$, consequently, H-gate devices show increased drain current than T-gate counterpart as shown in Fig. 2(a) and (b).

Fig. 3 shows the drain-induced barrier lowering, DIBL, of T-gate and H-gate devices in MOSFET mode and DTMOS

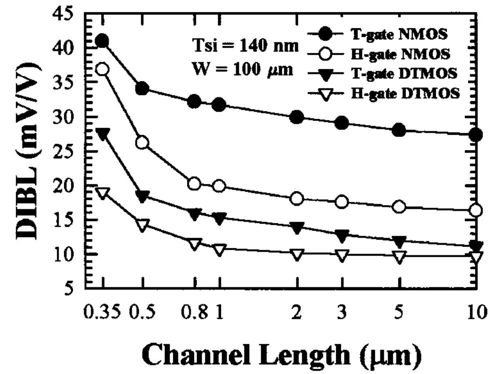


Fig. 3. DIBL of T-gate and H-gate devices in MOSFET mode and DTMOS mode versus channel length.

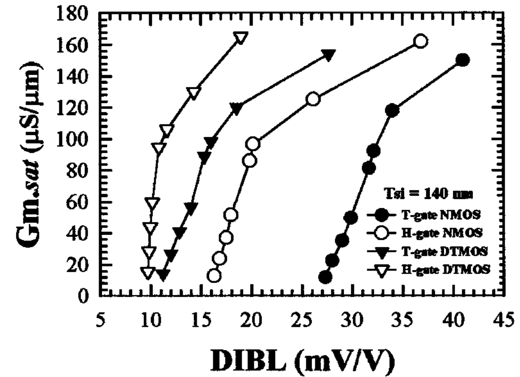


Fig. 4. Gm.sat versus DIBL with T-gate and H-gate devices in MOSFET mode and DTMOS mode.

mode versus channel length. The devices have much lager DIBL under MOSFET mode, especially for T-gate structure. However, when devices are operated under DTMOS mode, DIBL is dramatically reduced for both T-gate and H-gate devices. Because DIBL is the change in the potential energy barrier between the source and channel at the Si interface, it can result from both the built-in p-n junction electric field and the reverse-bias drain voltage. So, under DTMOS-mode operation, the positive $V_{\rm BS}$ provide a forward bias for body-to-source and body-to-drain junction. This thus reduces the built-in electric field of p-n junction and diminishes the effect of the reverse-bias drain voltage. So DIBL is reduced significantly in DTMOS mode. To treat the fair comparison of performances between H-gate and T-gate devices, Fig. 4 shows the saturation transconductance (Gm.sat) versus DIBL with T-gate and H-gate devices in MOSFET mode and DTMOS mode. For a given DIBL, H-gate DTMOS shows higher value of saturation transconductance than T-gate NMOSFET. Besides, the H-gate device operated under DTMOS-mode still has best performance among these four operating modes.

## IV. Conclusion

The characteristics of SOI devices with different gate structures under MOSFET-mode and DTMOS-mode operation are investigated. Since the gate is tied to body, the body-to-source junction is “forward biased,” the threshold voltage of devices will decrease under DTMOS-mode operation. Thus, the devices can have higher driving current, especially for H-gate devices in

this study. Besides, for both T-gate and H-gate devices, DIBL is drastically reduced operating in DTMOS-mode. To compare devices performances, it is worth to note that the H-gate devices show smaller DIBL and higher Gm.sat than the T-gate ones, due to its higher body effect factor.

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