Electrostatic Discharge Protection Design for Mixed-Voltage CMOS I/O Buffers

Ming-Dou Ker, *Senior Member, IEEE*, and Chien-Hui Chuang

***Abstract*—A new electrostatic discharge (ESD) protection circuit, using the stacked-nMOS triggered silicon controlled rectifier (SNTSCR) as the ESD clamp device, is designed to protect the mixed-voltage I/O buffers of CMOS ICs. The new proposed ESD protection circuit, which combines the stacked-nMOS structure with the gate-coupling circuit technique into the SCR device, is fully compatible to general CMOS processes without causing the gate-oxide reliability problem. Without using the thick gate oxide, the experimental results in a 0.35-μm CMOS process have proven that the human-body-model ESD level of the mixed-voltage I/O buffer can be successfully increased from the original $\sim$2 kV to $>$8 kV by using this proposed ESD protection circuit.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, mixed-voltage I/O buffer, silicon controlled rectifier (SCR).**

I. Introduction

TO IMPROVE circuit operating speed and performance, the device dimensions of MOSFET have been shrunk in the advanced deep-submicron integrated circuits. In order to follow the constant-field scaling requirement and to reduce power consumption, the power-supply voltages in CMOS ICs have also been scaled downwards. So, most microelectronic systems require the interfacing of semiconductor chips or subsystems with different internal power-supply voltages. With the mix of power-supply voltages, chip-to-chip interface I/O circuits must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3], [4]. For example, a 5-V interface is generally required for ICs realized in CMOS processes with a normal internal power-supply voltage of 2.5 or 3.3 V. The traditional CMOS I/O buffer with V_{DD} of 3.3 V is shown in Fig. 1(a), with output and input stages. When an external 5-V signal is applied to the I/O pad, the channel of the output pMOS and the parasitic drain–well junction diode in the output pMOS cause the leakage current paths from the I/O pad to V_{DD}, shown by the dashed lines in Fig. 1(a). Moreover, the gate oxides of the output nMOS, the gate-grounded nMOS for input electrostatic discharge (ESD) protection, and the input inverter stage are overstressed by the 5-V input signal. To solve the gate-oxide reliability issue without using the additional thick gate oxide process (also known as dual gate oxides in some CMOS processes [5], [6]), the stacked-MOS configuration has been widely used in the mixed-voltage I/O buffers [7]–[12], and in the power-rail ESD clamp circuits [13]. The typical 3-V/5-V-tolerant mixed-voltage I/O circuit is shown in Fig. 1(b) [8]. The pull-up pMOS, connected from the I/O pad to the V_{DD} power line, has self-biased circuits for tracking its gate and n-well voltages, when the 5-V input signals enter the I/O pad. The maximum output voltage level of such a 3-V/5-V-tolerant I/O buffer is only V_{DD} (3.3 V).

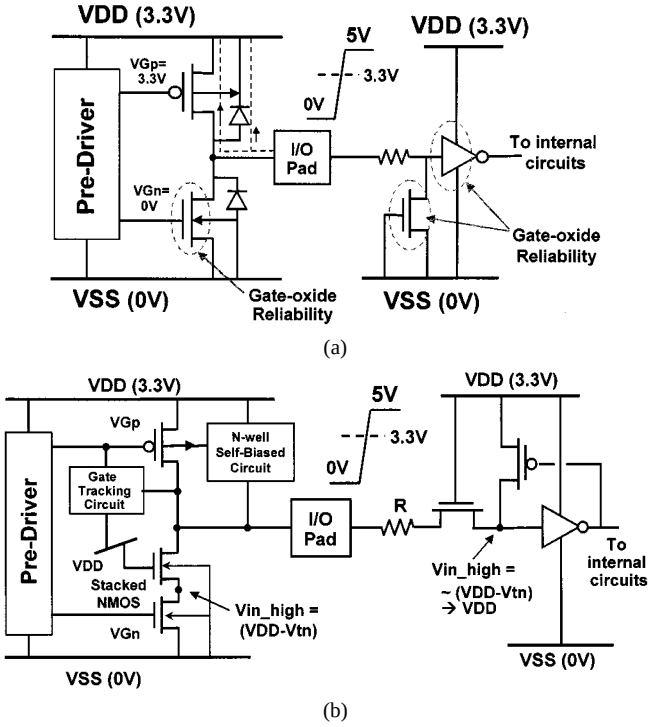

Fig. 1. Typical circuit diagram for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O buffer with the stacked-nMOS and the self-biased-well pMOS.

ESD stresses on an I/O pad have four basic pin-combination modes: positive-to-V_{SS} (PS-mode), negative-to-V_{SS} (NS-mode), positive-to-V_{DD} (PD-mode), and negative-to-V_{DD} (ND-mode) ESD stress conditions [14], [15]. To have high enough ESD robustness of the CMOS output buffer, the CMOS buffer is generally drawn with larger device dimensions and a wider spacing from the drain contact to the poly gate, which often occupy a larger layout area in the I/O cell. The V_{DD}-to-V_{SS} ESD clamp circuits across the power lines of CMOS ICs have been reported to effectively increase ESD

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robustness of CMOS I/O buffers [16]–[18]. The ESD current paths along the traditional CMOS output buffer under the positive-to-V_{SS} ESD stress condition can be discharged through the parasitic diode of pMOS and the V_{DD}-to-V_{SS} ESD clamp circuit to ground. Therefore, the traditional CMOS output buffer cooperating with the V_{DD}-to-V_{SS} ESD clamp circuit can sustain a much higher ESD stress [17]. But, due to the leakage current issue in the mixed-voltage I/O buffer, there is no parasitic diode connected from the I/O pad to V_{DD} power line. Because of the limitation of placing a diode from the pad to V_{DD} in mixed-voltage I/O circuits, the positive-to-V_{SS} ESD voltage zapping on the I/O pad cannot be diverted from the pad to V_{DD} power line, and cannot be discharged through the additional power-rail (V_{DD}-to-V_{SS}) ESD clamp circuit. Such positive-to-V_{SS} ESD current on the I/O pad is discharged through the stacked-nMOS in the snapback breakdown condition. However, the nMOS in stacked configuration has a higher trigger voltage V_{t1} and a higher snapback holding voltage V_{sb}, but a lower secondary breakdown current I_{t2}, as compared to the single nMOS [19]. Therefore, such mixed-voltage I/O circuits with stacked nMOS often have much lower ESD levels under the positive-to-V_{SS} ESD stress condition, as compared to the I/O circuits with a single nMOS [19], [20].

To increase ESD level of such mixed-voltage I/O circuits, some designs with extra multiple diodes in stacked configuration have been added from the I/O pad to the V_{DD} power line [3], [4]. However, while mixed-voltage I/O circuits operate in a high-temperature environment with a high-voltage input, the forward-biased leakage current from the pad to V_{DD} through the stacked diodes with their parasitic vertical p-n-p bipolar junction transistors (BJT) devices must be reduced by some extra circuit designs [21]–[24]. To sustain a high ESD level within a smaller silicon area, the low-voltage-triggering SCR (LVTSCR) device [25]–[27] has been reported as one of the most effective ESD clamp devices in CMOS ICs. But, such an LVTSCR device cannot be directly applied to protect the mixed-voltage I/O buffers due to gate-oxide reliability issue on the thin-oxide nMOS, which is inserted in the LVTSCR device structure without using the thick gate oxide.

In this paper, a new ESD protection circuit is proposed to significantly improve ESD robustness of the mixed-voltage I/O buffers by using the stacked-nMOS triggered SCR device [28]. The new proposed ESD protection circuit, which combines the stacked-nMOS structure with the gate-coupling circuit technique into the SCR device, is fully process compatible for general mixed-voltage I/O circuits without causing the gate-oxide reliability problem. Without using the thick gate oxide, the proposed ESD protection design for 3-V/5-V-tolerant mixed-voltage I/O buffer has been successfully verified in a 0.35-μm CMOS process.

II. On-Chip ESD Protection Circuit With Stacked-NMOS Triggered Silicon Controlled Rectifier

The proposed ESD protection design with the stacked nMOS triggered silicon controlled rectifier (SNTSCR) device for protecting the mixed-voltage I/O buffer is shown in Fig. 2(a).

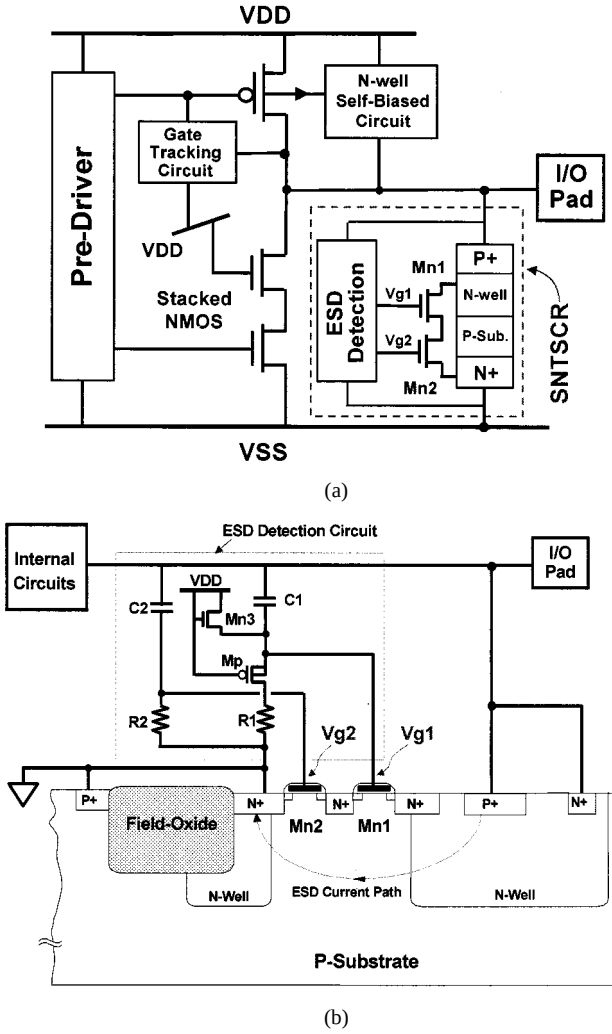


Fig. 2. (a) Proposed ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O buffer. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

The SNTSCR device structure and the ESD detection circuit are shown in Fig. 2(b). The ESD detection circuit, designed by using the gate-coupling technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate biases to trigger on the SNTSCR device during the ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating conditions. Detailed device behaviors, circuit operating principles, and circuit design technique are given in the following.

A. Device Structure and Its Characteristics

The cross-sectional view of the proposed SNTSCR device is shown in Fig. 2(b). This SNTSCR device structure can be realized in general CMOS processes without any extra process modification. In the SNTSCR device, two nMOS transistors (Mn1 and Mn2) are stacked in the cascoded configuration, where the drain of Mn1 is across the junction between an n-well region and the p-substrate. The p+ diffusion, n-well, p-substrate, and n+ diffusion to form a lateral SCR device for ESD current path between the I/O pad and V_{SS} is indicated by the dashed line in

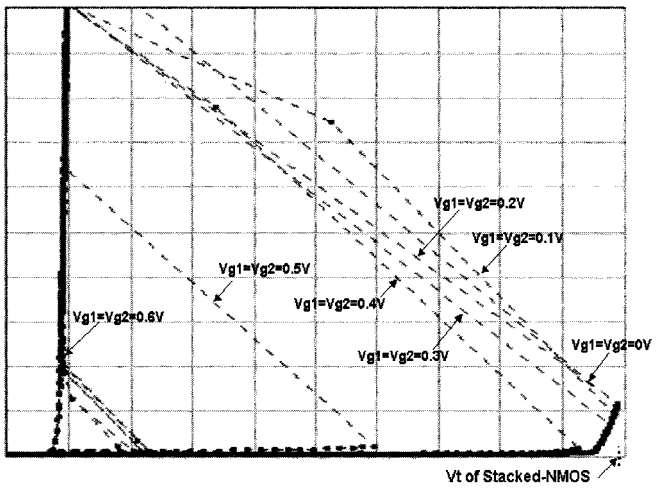


Fig. 3. Measured dc I–V curves of the fabricated SNTSCR device with channel length of 0.35 μm for both Mn1 and Mn2 under different gate biases (X axis: 1 V/div; Y axis: 1 mA/div).

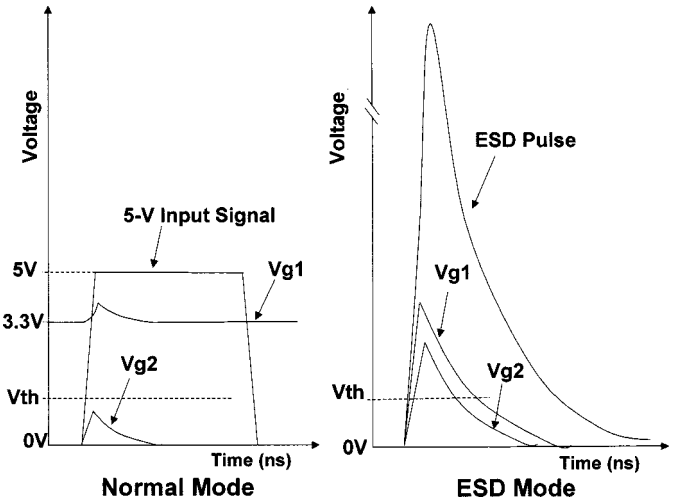


Fig. 4. Gate voltages on V_{g1} and V_{g2} of the SNTSCR device during (a) the normal circuit operating condition, and (b) the ESD stress condition, in a 3-V/5-V-tolerant mixed-voltage I/O circuit.

Fig. 2(b). The purpose of Mn1 and Mn2 connected in stacked configuration is to sustain the high voltage level of input signals without causing gate-oxide reliability issues in the SNTSCR device under the normal circuit operating condition. If only a single nMOS is inserted in the lateral SCR device, such as the traditional LVTSCR [25], the voltage across the gate oxide will be greater than V_{DD} when a high-voltage signal enters into the I/O pad. This causes the gate-oxide reliability issue on the traditional LVTSCR for long-time operation in such mixed-voltage I/O circuits. During ESD stress condition, Mn1 and Mn2 are both turned on by suitable gate-biased design to trigger the lateral SCR on for discharging ESD current. Without using the thick gate oxide in CMOS process, the proposed SNTSCR device has no gate-oxide reliability issue for using to protect the mixed-voltage I/O circuits.

The measured I–V characteristics of a standalone SNTSCR device with channel length of 0.35 μm for both Mn1 and Mn2 under different gate biases of V_{g1} and V_{g2} are shown in Fig. 3. The trigger voltage V_t of the SNTSCR device decreases from 10 to 6 V, when the gate bias increases from $V_{g1} = V_{g2} = 0$ V to $V_{g1} = V_{g2} = 0.5$ V. As $V_{g1} = V_{g2} => 0.6$ V, both the Mn1 and Mn2 are turned on to trigger SNTSCR on, therefore the V_t decreases to around 1–2 V. The holding voltage of the SNTSCR device is around ~1 V, which is not obviously changed by the different layout parameters on the channel length of Mn1 and Mn2 in this investigation. With suitable gate biases on Mn1 and Mn2, the trigger voltage of SNTSCR device can be reduced much lower than the snapback breakdown voltage of the stacked-nMOS (about ~10 V) in the mixed-voltage I/O buffer. Therefore, the new proposed ESD protection circuit with the SNTSCR device can effectively protect the mixed-voltage I/O buffers.

B. Operating Principles

Fig. 4(a) and (b) shows the desired voltage waveforms of the gate biases (V_{g1} and V_{g2}) provided by the ESD detection circuit in the normal circuit operating condition and the ESD stress condition, respectively, in the 3-V/5-V-tolerant mixed-voltage I/O circuit.

In the normal circuit operating condition, the SNTSCR is kept off, so that it does not interfere with the voltage levels of signals on the I/O pad. At such a normal state, the Mn3 in Fig. 2(b) acts as a resistor to bias the gate voltage (V_{g1}) of Mn1 at V_{DD}. But, the gate of Mn2 is grounded through the resistor R_2. When the I/O pad is applied with a high input voltage (5 V), the center common n+ region between the Mn1 and Mn2 transistors has a voltage level of about $V_{DD} - V_{thn}$ (where V_{thn} is the threshold voltage of nMOS). So, all the devices in the ESD protection circuit can meet the limited electrical-field constraint of gate-oxide reliability during the normal circuit operation condition. When the voltage of the I/O pad transfers from 0 to 5 V, the coupled gate voltage V_{g2} of Mn2 through the capacitor C_2 is designed to be below the threshold voltage of nMOS, as that shown in Fig. 4(a). The coupled voltage through the capacitor C_1 can also increase the gate voltage of Mn1, when the voltage on the I/O pad transfers from 0 to 5 V. The pMOS (Mp) in Fig. 2(b) is therefore designed to clamp the excessive voltage once the voltage of Mn1's gate increases to $V_{DD} + V_{thp}$ (where V_{thp} is the magnitude of the threshold voltage of Mp). The corresponding voltage waveforms on V_{g1} and V_{g2} are illustrated in Fig. 4(a), when the voltage on I/O pad transfers from 0 to 5 V. By suitable design on the ESD detection circuit, the SNTSCR can be kept off under the normal circuit operating condition. Moreover, the pMOS (Mp) can further clamp the gate voltage of Mn1 to ensure gate-oxide reliability on Mn1, even if the I/O pad has a high input voltage level.

During the positive-to-V_{SS} ESD stress condition, a positive high ESD voltage is applied to the I/O pad with V_{SS} grounded but V_{DD} floating. In this ESD stress condition, the gate of Mp is grounded since the initial voltage level on the floating V_{DD} power line is zero. So, the Mp is turned on, but the Mn3 is off. The capacitors C_1 and C_2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed higher than the threshold voltage to turn on Mn1 and Mn2 for triggering the

SNTSCR device on, before the devices in the mixed-voltage I/O circuit are damaged by ESD energy. The corresponding voltage waveforms on V_{g1} and V_{g2} are illustrated in Fig. 4(b), when the positive-to-V_{SS} ESD voltage is applied to the I/O pad. When the SNTSCR is triggered on, the ESD current is mainly discharged from the I/O pad to V_{SS} through this SNTSCR device. The characteristics of lower trigger voltage and low holding voltage of the gate-coupling SNTSCR device can safely protect the thin gate oxide in the mixed-voltage I/O circuits, as well as sustain a much higher ESD level within a smaller silicon area.

III. Design and Simulation of ESD Protection Circuit

A. Design Optimization on the ESD Detection Circuit

The purpose of the ESD detection circuit is to provide the suitable gate biases for the SNTSCR device under the normal circuit operating condition and ESD stress condition. To obtain suitable gate biases, it is important to determine the values of the coupling capacitors C_1 and C_2 and the sustaining resistors R_1 and R_2. Based on the above operating principles, the suitable values of C_1, C_2, R_1, and R_2 to meet the desired circuit operation in different CMOS processes can be adjusted and finely tuned by using HSPICE simulation.

The dependence between the coupling capacitance and the sustaining resistance can be investigated by HSPICE simulation with different turn-on time periods on Mn1 and Mn2. A 0–5-V input waveform with a rise time of 10 ns is used to simulate a 5-V input signal applied to the I/O pad, when the mixed-voltage I/O circuit is under normal circuit operating condition with V_{DD} bias of 3.3 V. The HSPICE-simulated voltage waveforms on V_{g1} and V_{g2} are shown in Fig. 5(a), when the $C_1 = C_2$ is chosen at 20 fF and the $R_1 = R_2$ is chosen at 130 kΩ. The coupled voltage on V_{g2} in Fig. 5(a) is smaller than V_{thn} ($\sim$0.6 V), therefore the SNTSCR is not triggered on. The coupled voltage on V_{g1} is further limited to $\sim$3.8 V after the rising transition of the input 5-V signal, which is clamped by the pMOS Mp in Fig. 2(b).

The SNTSCR device should be triggered on by the ESD detection circuit during the ESD stress condition, before the devices in the mixed-voltage I/O circuit are broken down by the overstress ESD voltage. A 0–10 V ramp voltage waveform with a rise time of 5 ns is therefore used to simulate the rising transition of ESD voltage, before the mixed-voltage I/O circuit is broken down by ESD voltage. Under the positive-to-V_{SS} ESD stress condition, V_{DD} is floating with an initial voltage level of 0 V. The HSPICE-simulated voltage waveforms on V_{g1} and V_{g2} under such an ESD stress condition are shown in Fig. 5(b), when the $C_1 = C_2$ ($R_1 = R_2$) is still kept at 20 fF (130 kΩ). The coupled voltage on V_{g1} and V_{g2} in Fig. 5(b) are both greater than V_{thn} ($\sim$0.6 V). From the measured results shown in Fig. 3, the SNTSCR is turned on when the V_{g1} and V_{g2} are greater than 0.6 V. Therefore, the SNTSCR can be triggered on to discharge ESD current before the mixed-voltage I/O circuit is broken down by ESD voltage.

To further investigate the dependence between the coupling capacitors C_1, C_2 and sustaining resistors R_1, R_2 to trigger on the SNTSCR device under ESD stress condition, a turn-on time is further defined in Fig. 5(b) as the time period when the coupled voltages on V_{g1} and V_{g2} are both greater than the nMOS

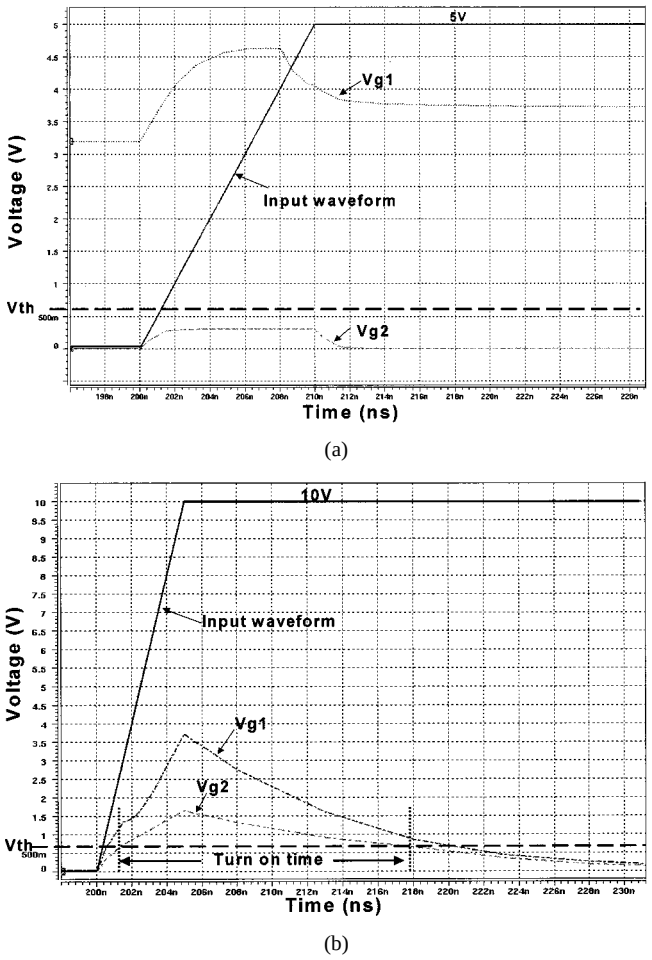


Fig. 5. HSPICE-simulated results under (a) the normal circuit operating condition with a 5-V input signal, and (b) the ESD stress condition with a 10-V rising voltage, on the I/O pad.

threshold voltage V_{thn} under such a 0–10 V rising transition. In Fig. 5(b), the turn-on time is found to be about $\sim$ 17 ns. This turn-on time can be further adjusted by changing the coupling capacitors and sustaining resistors in the ESD detection circuit. The values of the coupling capacitors C_1, C_2 and sustaining resistors R_1, R_2 are changed and simulated by HSPICE to choose suitable R and C values for different required turn-on times.

Fig. 6 depicts the simulated results on the relation between coupling capacitance $C_1 = C_2$ and sustaining resistance $R_1 = R_2$ under two different turn-on times (10 and 20 ns). The turn-on time can be kept the same by using different values of the coupling capacitance and sustaining resistance. This leads to a more feasible design to realize the ESD detection circuit in different CMOS processes. To obtain a longer turn-on time, the R_1 (R_2) and C_1 (C_2) have to be designed with larger values, but, with too much larger R_1 (R_2) and C_1 (C_2), the SNTSCR could be also trigged on by the normal 0–5 V input signals under the normal circuit operating condition. Therefore, there is a design boundary to choose suitable R_1 (R_2) and C_1 (C_2) to meet the desired circuit operation. Such a design boundary on the coupling capacitance and sustaining resistance can be found by HSPICE simulation, which is shown by the dashed line in Fig. 6. The overdesign region in Fig. 6 means that the coupling capacitance is overdesigned in the ESD

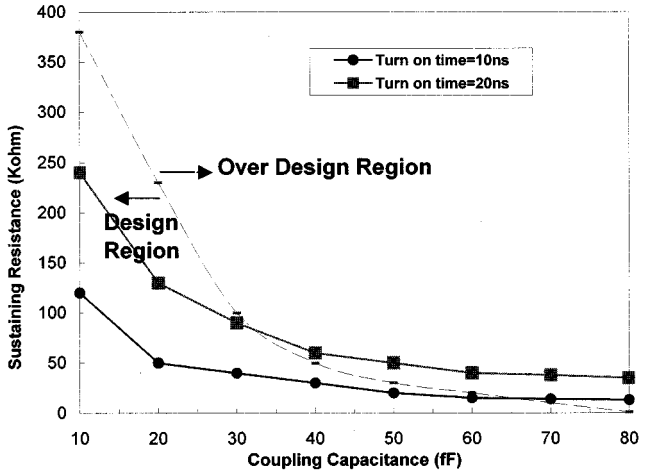


Fig. 6. HSPICE-simulated results on the relation between the coupling capacitance $C_1 = C_2$ and the sustaining resistance $R_1 = R_2$ under different turn-on times.

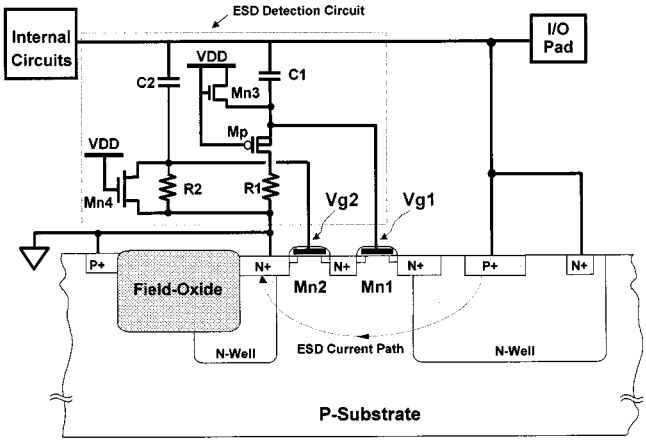


Fig. 7. Modified design on the ESD detection circuit with the SNTSCR device to have a larger design region on the sustaining resistance and coupling capacitance for protecting the mixed-voltage I/O buffer.

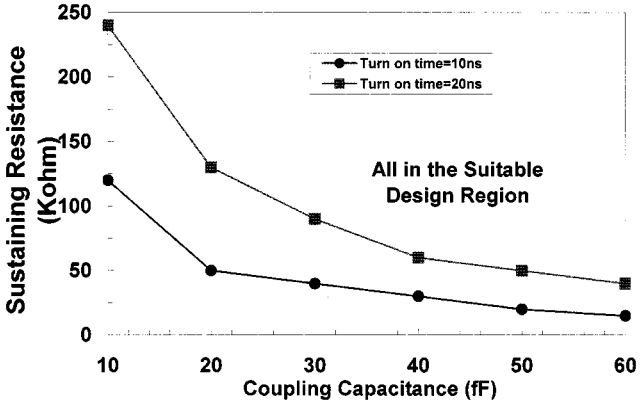


Fig. 8. HSPICE-simulated results on the relation between the coupling capacitance $C_1 = C_2$ and the sustaining resistance $R_1 = R_2$ under different turn-on times of the modified ESD detection circuit in Fig. 7 to have a wider design window.

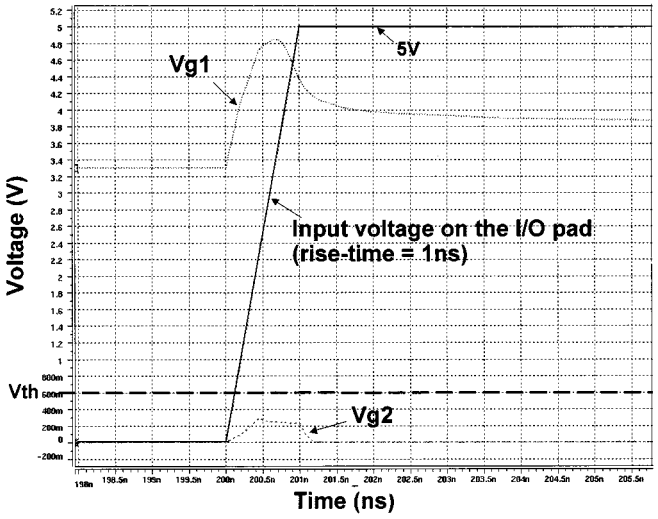


Fig. 9. HSPICE-simulated voltage waveforms on V_{g1} and V_{g2} in the modified circuit of Fig. 7, under normal operating condition with a 5-V input signal of 1-ns rise time on the I/O pad.

detection circuit, which will cause the unexpected turn-on of SNTSCR under normal 5-V input operation. So, the coupling capacitance and sustaining resistance located in the overdesign region is not suitable for practical applications. With the design boundary, the coupling capacitance and sustaining resistance in ESD detection circuit can be still correctly chosen to meet the desired circuit operation for a given CMOS process.

B. Improved Design Window for R and C

To further improve the design region for easily choosing the suitable sustaining resistance and coupling capacitance in general CMOS processes, a modified design on the ESD detection circuit with an additional nMOS (Mn4) is shown in Fig. 7. The extra device, Mn4, is added across the sustaining resistor R_2, which is located between the gate of Mn2 and V_{SS}. The gate of Mn4 is biased at V_{DD}. The gate of Mn4 is better connected to the V_{DD} power line through a diffusion resistor for consideration with the antenna rule issue. Under the normal circuit operating condition, Mn4 is always turned on to clamp the coupling voltage V_{g2} below the threshold voltage V_{thn}, and to keep the Mn2 always off. Therefore, the SNTSCR can be guaranteed off under the normal circuit operating condition.

Under the ESD stress condition, Mn4 is off since the initial voltage level on the floating V_{DD} power line is zero. The voltage V_{g2} coupled to the gate of Mn2 is determined by the sustaining resistance R_2 and the coupling capacitance C_2. Therefore, the suitable design window for the sustaining resistance and coupling capacitance of this modified ESD detection circuit can be obviously improved. The sustaining resistance and coupling capacitance of this modified ESD detection circuit to have the desired turn-on times of 10 or 20 ns are simulated and shown in Fig. 8, where the entire region is suitable for choosing the sustaining resistance and coupling capacitance.

With a device dimension (W/L) of only 10 μm/0.35 μm for Mn4, the V_{g1} and V_{g2} voltage waveforms in this modified circuit, under the normal circuit operating condition with a 5-V input signal applied to the I/O pad, is simulated and shown in Fig. 9, where the input signal has a rise time of only 1 ns. As seen in Fig. 9, even if the rise time of the 5-V input signal is as fast as 1 ns, the coupled V_{g2} voltage waveform during the input

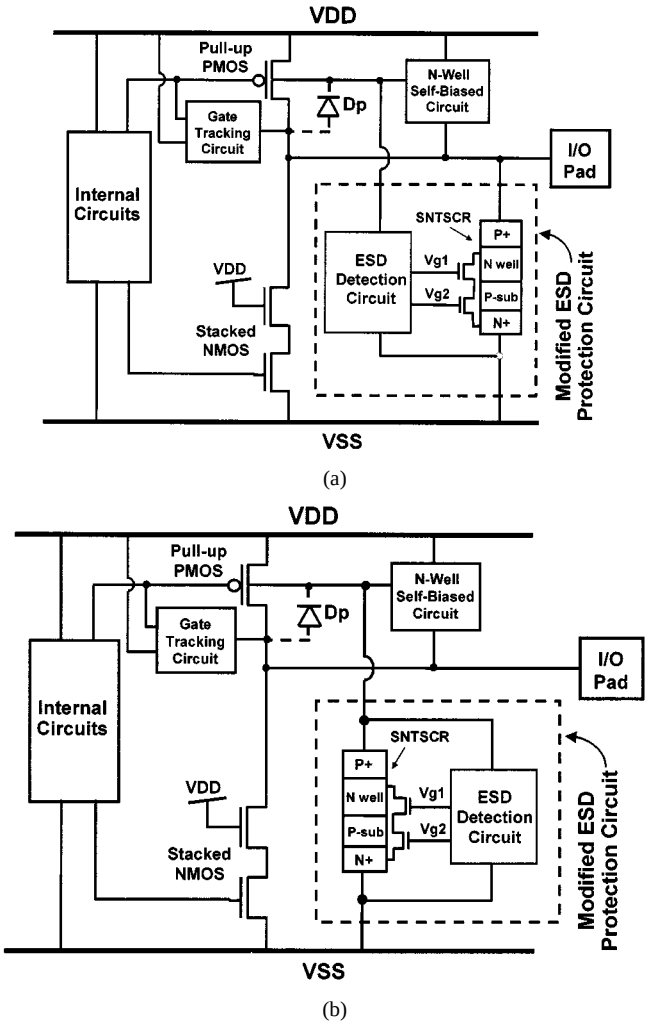


Fig. 10. Modified deign of the ESD protection circuit with the SNTSCR device for the mixed-voltage I/O buffer to have (a) higher noise margin to the I/O signals, and (b) no extra additional parasitic capacitance to the I/O pad.

transition can be kept always smaller than its V_{th}. Therefore, the SNTSCR can be guaranteed off under the normal circuit operating condition by this modified circuit design. By only adding the Mn4 into the ESD detection circuit, it becomes very easy and feasible to determine the suitable values for the coupling capacitance (C_1 and C_2) and the sustaining resistance (R_1 and R_2).

C. Modified Design to Improve Noise Margin of SNTSCR

When the mixed-voltage I/O buffer is under normal circuit operating condition with a high-voltage input signal, the overshooting noise pulse generated from the external circuits or interfaces could be coupled into the I/O pad to accidentally trigger on the SNTSCR in the ESD protection circuit [29]–[32]. To further improve the noise margin of the SNTSCR device in the proposed ESD protection circuit without being accidentally triggered on during normal circuit operating condition, a further modified design is shown in Fig. 10(a). The ESD detection circuit is connected from the self-biased n-well of the pull-up pMOS, where the parasitic drain–well diode Dp between the I/O pad and the n-well essentially exists in the pMOS device structure. Only the noise, higher than the voltage level of the n-well pulsing the cut-in voltage of a diode, can reach to the ESD detection circuit. Therefore, this modified ESD protection design not only has a high ESD level, but also a better noise margin to the input signals on the I/O pad with an overshooting glitch.

Fig. 10(b) shows another modified connection on the ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O buffer. The main purpose of this modified connection on the ESD protection circuit in Fig. 10(b) is to provide the mixed-voltage I/O buffer with a higher ESD robustness but no extra additional parasitic capacitance (generating from the ESD detection circuit and the SNTSCR device) to the I/O pad. With this modified connection, the ESD protection circuit with the SNTSCR device also has a higher noise margin to the overshooting glitch at the I/O pad, during the normal circuit operating condition. Under the positive-to-V_{SS} ESD stress condition, the ESD current first flows through the parasitic diode Dp into the floating n-well of the pull-up pMOS, and then is discharged to V_{SS} through the turned-on SNTSCR device. The coupling capacitance (C_1 and C_2) in the ESD detection circuit and the parasitic junction capacitance in the SNTSCR device are blocked from the I/O pad by the drain–well diode Dp in the pull-up pMOS. This modified design is more suitable for high-speed I/O applications, which often require a lower input loading capacitance to the I/O pad.

IV. Experimental Results

The experimental test chip has been fabricated in a 0.35-μm silicided CMOS process. There is a thin-oxide pull-up pMOS (pull-down stacked-nMOS) device placed between the I/O pad and V_{DD} (V_{SS}). The capacitors (C_1 and C_2), resistors (R_1 and R_2), Mp, Mn3, and Mn4 are composed of the ESD detection circuit for providing suitable gate biases to the SNTSCR device. Capacitors C_1 and C_2 are realized by inserting the metal layer right under the metal bond pad without adding extra layout area to the I/O cell. Their capacitance can be adjusted by changing the overlap area between the metal layer and the bond pad metal. R_1 and R_2 are realized by the n-well resistance, and their resistance can be adjusted by changing the length of the n-well regions in layout.

A. Leakage Current

The leakage current under normal circuit operating conditions is a concern for an ESD protection circuit connected to an I/O pin. The leakage currents of the fabricated mixed-voltage I/O buffers with and without the proposed ESD protection circuit are measured and compared in Fig. 11. The leakage current is measured (using an HP4155) by applying a voltage ramp from 0 to 5 V to the I/O pad under the bias condition of 3.3-V V_{DD} and 0-V V_{SS}. In Fig. 11, the maximum leakage current of the mixed-voltage I/O buffer without (with) the proposed ESD protection circuit under 5-V bias at the I/O pad is 175 (215) pA. The increase of the leakage current from adding the ESD protection circuit is only 40 pA, whereas the SNTSCR device in the ESD protection circuit is drawn with a device width of 60 μm. The mixed-voltage I/O buffer in this measurement has a channel

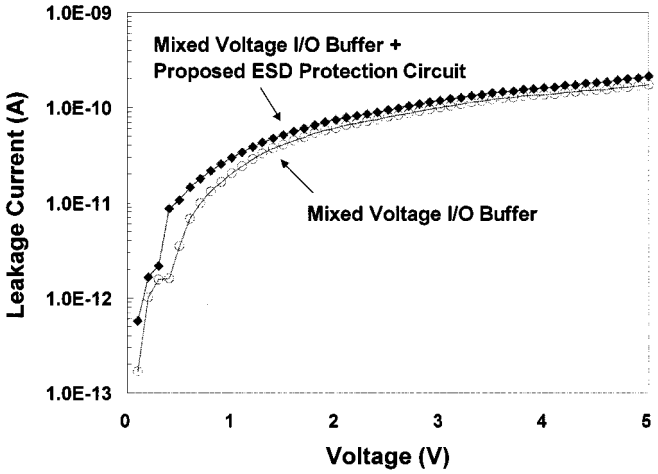


Fig. 11. Comparison of the leakage current of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit. The mixed-voltage I/O buffer in this measurement has a channel width of 180 μm in the stacked-nMOS and a channel width of 360 μm in the pull-up pMOS.

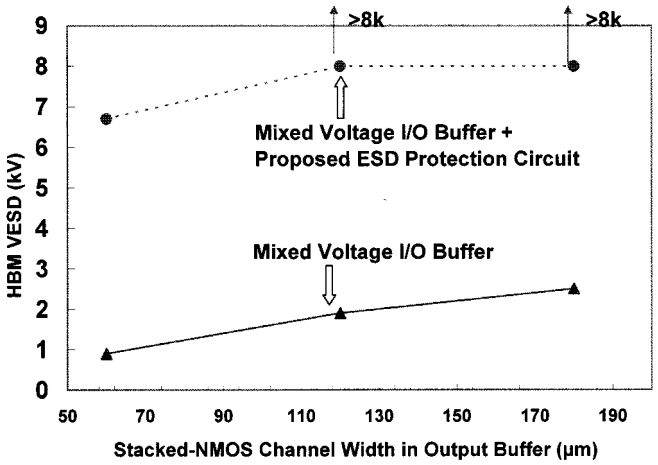


Fig. 12. Comparison of the positive-to-V_{SS} HBM ESD robustness of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit, under different channel widths of the stacked nMOS in the mixed-voltage I/O buffers.

width of 180 μm in the stacked nMOS and a channel width of 360 μm in the pull-up pMOS.

B. ESD Robustness

The positive-to-V_{SS} human-body-model (HBM) [14] ESD levels of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit are measured and compared in Fig. 12. The mixed-voltage I/O buffers with different stacked-nMOS channel widths are also tested as a reference. The HBM ESD level of the mixed-voltage I/O buffer (with stacked-nMOS channel width of 120 μm) can be obviously improved from the original $\sim$2 kV to become greater than 8 kV by the proposed ESD protection circuit with the SNTSCR device. In Fig. 12, all the mixed-voltage I/O buffers protected by the proposed ESD protection circuit have the same SNTSCR device width of 60 μm.

The HBM ESD robustness of the mixed-voltage I/O buffer, with and without the proposed ESD protection design (including the SNTSCR device), under the four pin-combination modes of ESD stress on the I/O pad, is listed in Table I. The stacked nMOS of the mixed-voltage I/O buffer in this ESD test has a W/L of only 60 μm/0.5 μm, and the pull-up pMOS of the mixed-voltage I/O buffer has a W/L of only 120 μm/0.5 μm. The stacked nMOS in the SNTSCR device has a W/L of 60 μm/0.35 μm. As seen in Table I, the ESD levels under the PS-, NS-, and PD-modes have been significantly improved by the proposed ESD protection design with the SNTSCR device. Especially, the PS- and PD-mode ESD levels of the mixed-voltage I/O buffer have a great increase. In Table I, the ND-mode ESD stress is not improved, because the V_{DD}-to-V_{SS} ESD clamp circuit is not included in the test chip in this investigation. During the negative-to-V_{DD} ESD stress, the ESD current may be discharged through the pull-up pMOS, or be first conducted to the V_{SS} power line and then discharged through the V_{DD}-to-V_{SS} ESD clamp circuit to the grounded V_{DD}. Without the V_{DD}-to-V_{SS} ESD clamp circuit in this test chip, the original ESD levels of the mixed-voltage I/O buffer (without SNTSCR device) in the PD- and ND-mode ESD stresses are almost the same of 2.8 kV $\sim$2.9 kV. In the whole-chip layout of a CMOS IC, the turn-on efficient V_{DD}-to-V_{SS} ESD clamp circuit [16]–[18], [21], [24] should be added into the chip layout to improve the ND-mode ESD level of the mixed-voltage I/O buffers and also to avoid unexpected internal ESD damages.

TABLE I
HBM ESD ROBUSTNESS OF THE MIXED-VOLTAGE I/O BUFFER WITH AND WITHOUT THE PROPOSED ESD PROTECTION DESIGN WITH THE SNTSCR DEVICE

HBM ESD Stress / I/O Circuits	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD(+)	ND-Mode VDD(-)
Only Mixed-Voltage I/O Buffer	1kV	3.9kV	2.8kV	2.9kV
Mixed-Voltage I/O Buffer + SNTSCR	6.8kV	5.6kV	6.9kV	2.9kV

Stacked NMOS W/L= 60/0.5 (μm)
Pull-up PMOS W/L= 120/0.5 (μm)
SNTSCR W/L= 60/0.35 (μm)

The transmission line pulse generator (TLPG) with a pulse width of 100 ns is also used to verify the secondary breakdown current I_{t2} of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit, and the measured results are shown in Fig. 13 under the positive-to-V_{SS} ESD stress condition. The I_{t2} of the stacked nMOS with channel width of 180 μm is around 2 A, but it can be increased up to $\sim$7 A by the proposed ESD protection circuit with an SNTSCR device of 60 μm. The measured I_{t2} values are consistent to the HBM ESD level with a factor around 1.5 kΩ. This has further verified the effectiveness of the proposed ESD protection circuit with the SNTSCR device.

The positive-to-V_{SS} machine-model (MM) [15] ESD levels of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit are measured and compared in Fig. 14. The mixed-voltage I/O buffers with different stacked-nMOS channel widths are also tested as a reference. From the measured results, the MM ESD level of the mixed-voltage I/O buffer with a channel width of 120 μm in the stacked nMOS can be significantly improved from the original $\sim$200 V to

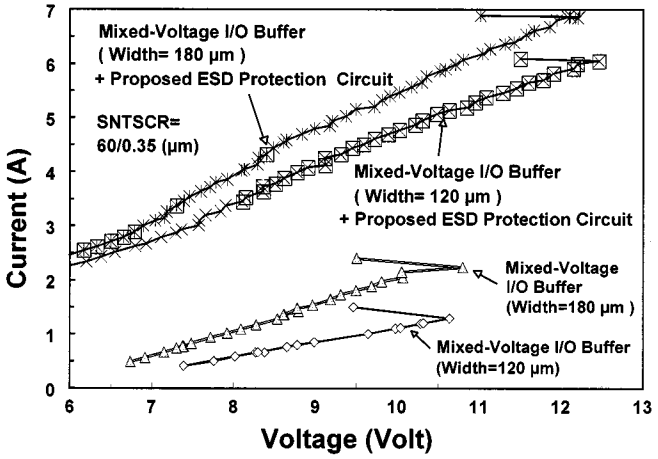


Fig. 13. Comparison of the TLPG-measured I–V curves of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit, under different channel widths of the stacked nMOS in the mixed-voltage I/O buffers.

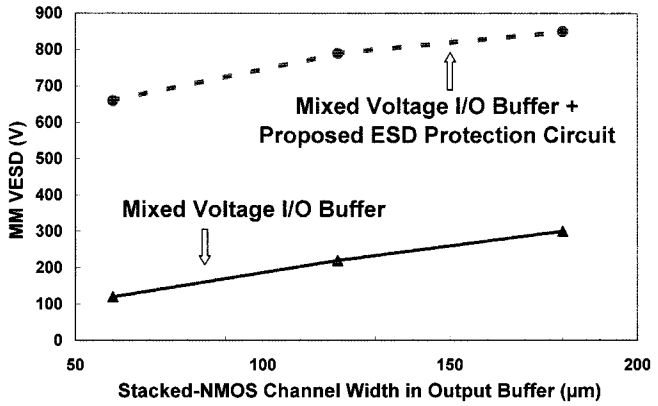


Fig. 14. Comparison of the positive-to-V_{SS} MM ESD robustness of the mixed-voltage I/O buffers with and without the proposed ESD protection circuit, under different channel widths of the stacked nMOS in the mixed-voltage I/O buffers.

become ∼800 V by the proposed ESD protection circuit with an SNTSCR device width of only 60 μm.

C. Turn-on Verification

To verify the turn-on efficiency of the proposed ESD protection circuit, a 0–8 V sharply rising voltage pulse with a rise time of 10 ns is applied to the I/O pad when V_{SS} is relatively grounded but V_{DD} is floating (to simulate the positive-to-V_{SS} ESD stress condition). The stacked nMOS in the output buffer has a snapback breakdown voltage of ∼10 V. Such a 0–8 V voltage pulse applied to the I/O pad does not break down the stacked nMOS of the mixed-voltage output buffer, but the 0–8 V voltage pulse can trigger on the ESD protection circuit to cause a degraded voltage waveform, as that shown in Fig. 15, where the applied 0–8 V voltage pulse is clamped to ∼2 V by the SNTSCR device. The mixed-voltage I/O buffer used in this measurement has the additional device Mn4, as shown in Fig. 7. During the positive-to-V_{SS} ESD stress, the gate of Mn4 is initially kept at 0 V. Therefore, the coupled gate voltage of Mn2 (Mn1) through the capacitor C_2 (C_1) is sustained longer in time by the sustaining resistor R_2 (R_1) in Fig. 7. The SNTSCR device is therefore triggered on by the coupled gate voltages V_{g1} and V_{g2} to

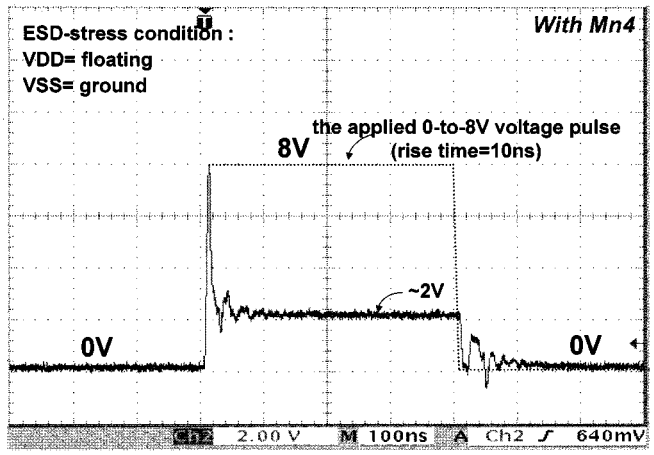
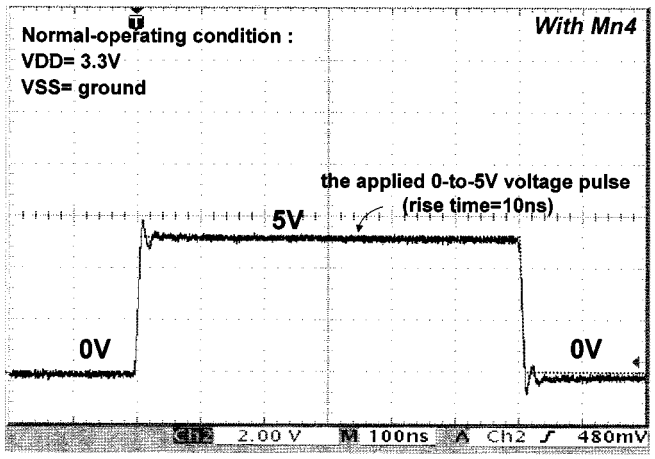
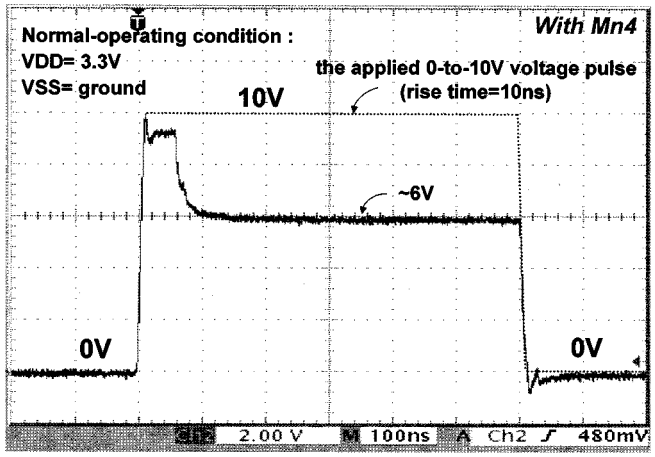


Fig. 15. Measured voltage waveform on the I/O pad triggered by a 0–8 V voltage pulse with a rise time of 10 ns, under the positive-to-V_{SS} ESD stress condition. (Y axis: 2 V/div.; X axis: 100 ns/div.)



(a)



(b)

Fig. 16. Measured voltage waveforms on the I/O pad triggered by (a) 0–5 V and (b) 0–10 V voltage pulses with a rise time of 10 ns, under the normal operating condition with $V_{DD} = 3.3$ V and $V_{SS} = 0$ V. (Y axis: 2 V/div.; X axis: 100 ns/div.)

clamp the voltage on the I/O pad. The degraded voltage waveform has verified the effectiveness of the proposed ESD protection circuit with the SNTSCR device to protect the mixed-

voltage I/O circuits. The transition time of ~10 ns from 8 to 2 V in Fig. 15 is the corresponding turn-on speed of the SNTSCR device realized in this 0.35-μm CMOS process.

In the normal circuit operating condition with the V_{DD} (V_{SS}) biased at 3.3 V (0 V), a 0–5 V input voltage pulse with a rise time of 10 ns is applied to the I/O pad. The voltage on the I/O pad is monitored by a digital oscilloscope. But the applied 0–5 V voltage waveform is not degraded, as shown in Fig. 16(a). The mixed-voltage I/O buffer used in this measurement has the additional device Mn4. During the normal circuit operating condition, the gate of Mn4 is biased at V_{DD} (3.3 V). The coupled gate voltage of Mn2 through the capacitor C_2 is discharged to ground by the turned-on Mn4. So, the SNTSCR device is not triggered on by the normal input signals of 5 V. If the applied voltage pulse is further increased to 10 V under the normal circuit operating condition, the measured voltage waveform on the I/O pad is shown in Fig. 16(b). The applied 0–10 V voltage pulse is clamped to about ~6 V in Fig. 16(b), but not to the voltage level of ~2 V, as shown in Fig. 15. The stacked nMOS has a snapback breakdown of ~10 V and a snapback holding voltage of ~6 V in this 0.35-μm CMOS process. Therefore, the degraded voltage level of ~6 V in Fig. 16(b) is clamped by the stacked nMOS of the mixed-voltage I/O buffer in the snapback region. If the SNTSCR device in the ESD protection circuit is triggered on, the voltage level should be clamped to its holding voltage of ~2 V. However, the applied 0–10 V voltage pulse is only clamped to ~6 V, as shown in Fig. 16(b). This result has further confirmed that the additional Mn4 device (added in the ESD detection circuit) can safely apply the SNTSCR device to protect the mixed-voltage I/O buffer without being unexpectedly triggered under the normal circuit operating condition.

V. Conclusion

A new ESD protection design, using the stacked-nMOS triggered silicon controlled rectifier (SNTSCR) device, has been successfully verified in a 0.35-μm CMOS process. The I–V characteristics of the SNTSCR device with different gate biases and the turn-on behaviors of the ESD protection circuit have been measured to verify its effectiveness. By using the ESD detection circuit with suitable design on the coupling capacitance and sustaining resistance, the SNTSCR device can be fully triggered on within ~10 ns to discharge ESD current. By changing the connection of the ESD protection circuit from the I/O pad to the floating n-well of the pull-up pMOS in the mixed-voltage I/O circuit, the SNTSCR device has a high enough noise margin to the overshooting glitch on the I/O pad, during the normal circuit operating condition. Without using the thick gate oxide, this new proposed ESD protection circuit is fully process compatible with general sub-quarter-micron CMOS processes for effectively protecting the mixed-voltage interface circuits on the input and output pins.

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