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BIST scheme for DAC testing

S.J. Chang, C.L. Lee and J.E. Chen

A low-cost, built-in self-test (BIST) scheme for a digital-to-analogue converter (DAC) is presented. The basic idea is to convert the DAC output voltages corresponding to different input codes into different oscillation frequencies through a voltage controlled oscillator (VCO), and further transfer these frequencies to different digital codes using a counter. According to the input and output codes, performances of a DAC, such as offset error, gain error, differential nonlinearity (DNL), integral nonlinearity (INL), could be effectively detected by simply using digital circuits rather than complex analogue ones. In addition, the annoying DAC output noise could be naturally filtered out by this BIST method.

Introduction: Digital-to-analogue converters (DACs) are commonly used devices in mixed-signal ICs. Non-monotonic behaviour, offset error, gain error, differential nonlinearity (DNL) and integral non-linearity (INL) are important specifications for testing DACs [1–3]. However, one major difficulty in testing these parameters is the requirement of high precision instruments to measure the very small output change under the change of the input code. In addition, the statistical technique [4] was introduced to alleviate the nuisance of noise effect. In this Letter, a built-in seft-test (BIST) DAC scheme, which has high accuracy in extracting the small output change and eliminates the above mentioned noise effect but is low-cost, is proposed.
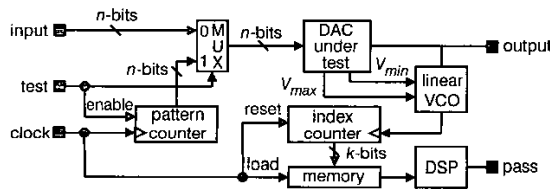

Fig. 1 *BIST scheme for DAC in SOC system*

BIST scheme: The proposed BIST scheme for a DAC is shown in Fig. 1. It comprises (i) a pattern counter as the test pattern generator (TPG), (ii) a multiplexer (MUX) which selects the normal input code or test pattern, (iii) a linear voltage controlled oscillator (VCO) to convert the DAC output voltage, which corresponds to different input codes, to different oscillation frequencies, (iv) an index counter to transfer the oscillation frequencies to digital codes, (v) a memory to store output codes of the index counter, and (vi) a digital signal processor (DSP) which is employed to evaluate the code difference and compare it with a predefined detection threshold.
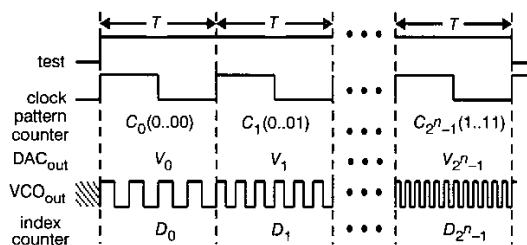

Fig. 2 *Timing diagram of DAC BIST scheme*

Test procedure: First, the minimum reference voltage V_{min} and maximum reference voltage V_{max} of the DAC are applied to the VCO and the corresponding counts, denoted as D_{min} and D_{max}, of the index counter for a unit clock period T are stored in the memory. *test* is then set to activate the pattern counter to generate test patterns. A typical timing diagram for DAC testing is shown in Fig. 2. The pattern counter is increased by 1 at each rising edge of *clock*. For the ith clock period, the DAC receives code C_i from the pattern counter and outputs voltage V_i which is converted to oscillation frequency f_i through the VCO. The index counter is clocked by this oscillation signal and its counts are stored to the memory at the end of this clock period and the index counter is reset to 0 again. The frequency is then transferred to index codes D_i by counting the number of oscillations for an interval of period T.

For a linear VCO [5], the output frequency is linear depending on the input voltage ($\Delta f = K_{VCO} \times \Delta V$, where K_{VCO} is the gain of the VCO). The relation between counts and input frequency of a counter for a constant period is also linear ($D_i = T \times f_i$). Hence, the corresponding relation between input pattern codes and output index ones will reflect the linearity of the DAC under test and its linearity error can be evaluated and detected by simply using digital circuits rather than complex analogue ones.

Test clock period and test precision: Let the minimum output change due to a change of input code by one least significant bit (LSB) of DAC be V_{LSB}. If the gain of the VCO is K_{VCO}, the minimum output frequency change, f_{LSB}, will be $f_{LSB} = K_{VCO} \times V_{LSB}$. To distinguish two given frequencies with minimum difference f_{LSB}, the minimum test period (T_{LSB}) must be $T_{LSB} = 1/f_{LSB}$ to generate two different counts with a difference equal to 1 for these two frequencies. In fact, the test precision could be increased by simply increasing the test period. For example, if the DAC output voltage deviates $0.1V_{LSB}$ from the normal voltage that makes the VCO output frequency deviate $0.1f_{LSB}$, it cannot be differentiated for $T = T_{LSB}$. However, if we increase the period of the test clock to be $T = 10T_{LSB}$, i.e. the count difference equals 10 for normal DAC output voltage, the $0.1f_{LSB}$ deviation will cause a count difference equal to 1. The relationship between period of test clock (T) and the test precision (TP) is: $T = TP \times T_{LSB} = TP/(K_{VCO} \times V_{LSB})$. Total test time for an n-bit DAC is approximately $T \times 2^n$. The maximum number of oscillations in a period is T/f_{max}. Thus, the required length of the index counter (k) is $k = \log_2(TP \times T_{LSB}/f_{max})$.

Specifications evaluation:

(1) *Non-monotonic behaviour testing:* The scheme can easily test the *non-monotonic* fault of the DAC since, for the fault, the DAC will produce decreasing output voltage for an increasing input code. It can be easily detected by simply checking whether $D_{i+1} < D_i$ or not.

(2) *Offset error testing:* Offset error is the difference between the ideal and actual DAC output values when the zero level digital input code is applied. It can be evaluated by: (unit: LSB)

$$Offset\ error = (D_0 - D_{min})/TR$$

(3) *Gain error testing:* Gain error is the difference between the measured output and the ideal output when a full-scale input code is applied. To make the gain error independent of offset error, offset error should be subtracted from the difference. It can be computed by: (unit: LSB)

$$Gain\ error = (D_{2^n-1} - D_{max})/TR - offset\ error$$

(4) *DNL testing:* DNL is a measure of the deviation between the actual analogue output change and the theoretical change of 1 LSB. It can be evaluated by: (unit: LSB)

$$DNL_i = (D_i - D_{i-1})/TR - 1$$

(5) *INL testing:* INL is defined by measuring the deviation of the actual converter output from the straight line of the ideal DAC transfer function. It is the cumulative effect, for any given input, of DNL and can be computed by: (unit: LSB)

$$INL_i = \sum_{j=1}^{i} DNL_j$$

Note that only four index codes, D_{min}, D_{max}, D_i and D_{i-1}, are requested to accomplish all of the above computations for each clock period.

Hence, four k-bit registers could replace the memory to reduce area overhead.

Noise effect reduction: Random noise in the output of the DAC will usually cause measurement error in the conventional sampling method. Multiple samples and an additional evaluation circuit are necessary to reduce the measurement error. In our test scheme, noises that increase the DAC output voltage will speed up the VCO output oscillation. Conversely, oscillation will be slowed down if the DAC output voltage is decreased by noises. Hence, the oscillation frequency is sometimes increased and sometimes decreased during a clock period T. Finally, they will cancel out each other to neutralise the noise effect. Fig. 3 is a simulation result of our BIST scheme for an 8-bit DAC to show the efficiency of noise reduction. Assume the linear VCO is oscillated between 10 and 100 MHz. Given a test precision $TP = 10$, the test period $T = 10 \times 256/(100-10 \text{ MHz}) \approx 28.44$ µs and total test time is approximately $256*T = 7.282$ ms. The ideal DAC output with a maximum $\pm 2V_{LSB}$ random noise is shown in Fig. 3a, and the partial magnified result is shown in Fig. 3b where the grey line is the ideal VCO output. The measured errors of DNL for all input codes are shown in Fig. 3c. This shows that the maximum error is reduced to ± 0.1 LSB for a given $\pm 2V_{LSB}$ random noise.
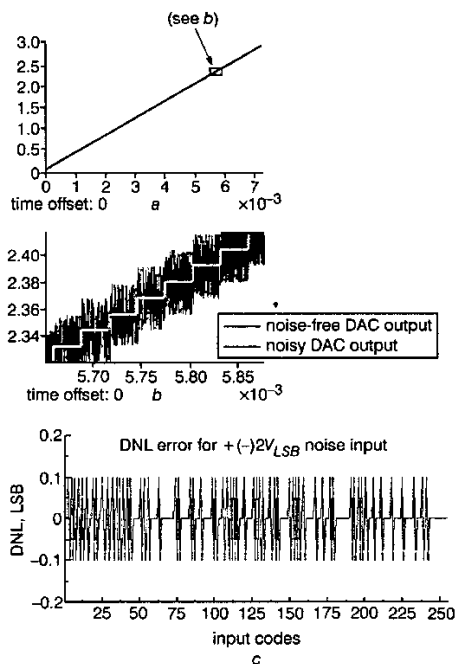

Fig. 3 *Simulation results of BIST scheme with noisy input signal*

a Timing diagram of DAC output
b Partial magnified result (of *a*)
c Measured errors of DNL for all input codes

Conclusion: An efficient BIST scheme to test the non-monotonic behaviour, offset error, gain error, DNL and INL of a DAC is presented. Since most of the added BIST circuits are digital, it has the advantage of low cost and being easily tested compared to conventional analogue BIST schemes. It also has the advantage of reducing the noise effect such that the conventional added statistical analysis circuit employed to alleviate the nuisance of noise is not required. Test precision can be increased simply by longer test time and adding adequate stages of the index counter.

S.J. Chang and C.L. Lee (*Department of Electronic Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, 300, Republic of China*)

E-mail: cllee@cc.nctu.edu.tw

J.E. Chen (*Department of Electrical Engineering, Chung-Hua University, Hsin-Chu, Taiwan, 300, Republic of China*)

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Low-power CSD linear phase FIR filter structure using vertical common sub-expression

Youngbeom Jang and Sejung Yang

A high-speed/low-power canonic signed digit (CSD) linear phase finite impulse response (FIR) filter structure using vertical common sub-expression is proposed. In the conventional linear phase CSD filter, the horizontal common sub-expression method (see Hartley, 1996) has been widely utilised due to the inherent symmetrical filter coefficients. However, use has been made of the fact that the most significant bits of adjacent filter coefficients in the linear phase filter are also equal since they have mostly similar values. Through the example, it is shown that the proposed structure is more efficient in the case where bit precision of implementation is lower.

Introduction: Linear phase finite impulse response (FIR) filters implemented with high-speed/low-power are required in the intermediate frequency (IF) processing block of wireless communication systems. High-speed/low-power implementation of filters is possible if multipliers can be efficiently replaced with adders and subtractors. By especially expressing the multipliers in canonic signed digit (CSD) form instead of 2's complement form, the best results can be obtained [1, 2]. Several methods to reduce further the number of adders and subtractors have been proposed. Among them, the sharing method for common sub-expression has been introduced in [3]. This technique extracts common sub-expression in all CSD coefficients. There are two kinds of common sub-expression forms: horizontal and vertical. Since linear phase filters have symmetric coefficients, they can be implemented efficiently, using the horizontal type of common sub-expressions [4]. In contrast, the vertical type of common sub-expressions destroys the symmetry of filter coefficients. However, in this Letter, we propose the efficient sharing method using vertical common sub-expressions in linear phase FIR filters.

Conventional common sub-expression method: An N-tap linear phase FIR filter has $N/2$ independent coefficients due to its symmetry. Consider the next 11-tap linear phase filter coefficients with CSD form shown in Fig. 1. For notational convenience, -1 is represented by n, and zeros are not represented in Fig. 1. With this filter coefficient table, we compare our proposed method with the conventional one. As shown in Fig. 1, horizontal common sub-expressions exist inherently since filter coefficients of the linear phase filters are symmetric. In order to apply the conventional method, horizontal common sub-expressions are first indicated with bold lines in Fig. 1. These common sub-expressions of $n0n$, $n001$, and $n01$ are then represented as:

$$x_2 = -x_1 - x_1 \gg 2, \quad x_3 = -x_1 + x_1 \gg 3, \quad x_4 = -x_1 + x_1 \gg 2 \quad (1)$$

where $\gg$ represents the shift operation. With these common sub-expressions, the output of the filter can be represented as:

$$
\begin{aligned}
y = {} & x_1 \gg 8 + x_2[-1] \gg 6 + x_3[-2] \gg 3 + x_4[-3] \gg 1 \\
& + x_1[-4] \gg 1 + x_1[-5] + x_1[-6] \gg 1 \\
& + x_4[-7] \gg 1 + x_3[-8] \gg 3 + x_2[-9] \gg 6 \\
& + x_1[-10] \gg 8
\end{aligned}
\quad (2)
$$