A New Approach to Determine the Drain-and-Source Series Resistance of LDD MOSFET's

Steve Shao-Shiun Chung and Jenq-Sheng Lee

***Abstract*—A new method for determining the *intrinsic* drain-and-source series resistance and the effective channel length of LDD MOSFET's is proposed. The method is based on the experimentally measured device *I–V* characteristics and a new parameter extraction procedure. A consistent set of the effective channel length and the gate-voltage-dependent drain-and-source series resistance was thus determined. The comparison between the measured and experimental drain current characteristics shows excellent agreement using the present model values.**

I. Introduction

The determination of drain-and-source series resistance R_{ds} in the lightly doped drain (LDD) MOS device has become an important issue for modeling its *I–V* characteristics since the value of this resistance is comparable with the channel resistance for short-channel devices. The present *I–V* model in SPICE for conventional MOS device has loss in accuracy for LDD MOS devices due to the larger series resistance effect. Various methods for determining the effective channel length along with the drain-and-source series resistance in single-drain (conventional) MOS devices have been reported [1]–[3]. Due to the partial overlap (between the n^- region and the gate) structure in LDD devices, R_{ds} becomes gate-voltage-dependent [4], [5] and so the method for single-drain device cannot be applied any more. Different approaches have been employed to determine this resistance effect. Sheu *et al.* [4] proposed a substrate bias technique to extract the effective channel length and the drain-and-source resistance. However, their way to extract the effective channel length becomes inadequate for *I–V* modeling at different gate voltages. Hu *et al.* [5] presented a measurement algorithm to describe the gate-voltage-dependent feature of the effective channel length and the drain-and-source series resistance. However, a model for practical circuit simulation application is not available. A better way to implement this drain–source resistance effect and an extraction algorithm to extract the above resistance and the effective channel length will be shown in this work.

II. New Method and Extraction Algorithm

Based on the modeling of *I–V* characteristics of LDD MOS devices [6], an LDD MOS device can be considered as an intrinsic MOS device in series with two resistors connected between the drain and source, respectively. These two resistors are gate- and drain-voltage-dependent. In this brief, only the so-called "*intrinsic drain-and-source series resistance*" is investigated, i.e., the resistance that includes the drain and source region measured at low drain–source bias. The drain-voltage-dependent feature and the model were described in [6]. From the *I–V* characteristics of an LDD MOS device operating in the linear region, the total drain-to-source resistance of an LDD MOS device operated in the linear region equals to the drain-and-source side series resistance and the channel resistance given by

$$R_T = R_{ds}(V_{GS}) + r_{ch} \tag{1}$$

where

$$r_{ch} = V'_{DS}/I_D = (1/\beta)(V'_{GS} - V_T - 0.5aV'_{DS})^{-1} \tag{2}$$

$$\beta = \beta_0/[1 + \theta(V_{GS} - V_T)(1 + \eta\, V_{DS})] \tag{3}$$

and

$$\beta_0 = \mu_0 C_{OX}\, W/L. \tag{4}$$

Here, $R_{ds}(= R_d + R_s)$ is the resistance outside the intrinsic MOS device, which includes the drain–source (n^+ and n^- regions), contact, and wiring resistances. For the following extraction, the contact and wiring resistances are assumed small compared with the n^+ and n^- region resistances. V_T is the threshold voltage. V'_{GS} and V'_{DS} are the terminal voltages of the intrinsic MOS device shown in the insert of Fig. 2. η and θ are the mobility degradation factors due to the lateral and transverse fields, respectively. a is the charge sharing factor related to the geometry effect. μ_0 is the low-field surface mobility. L and W are the effective channel length and width, respectively. For a detailed description of these parameters, please refer to [6].

The test structure used consists of a series of n-channel LDD MOS devices fabricated using 0.8-μm CMOS technology. The devices have the same drawn gate width ($W_m = 25\ \mu$m) but varying drawn channel lengths, $L_m = 0.6, 0.7, 0.8, 1.2, 1.5$, and 25 μm. The gate oxide thickness is 14 nm. To determine the effective channel length, L, I_D–V_{GS} characteristics are measured at small V_{DS} (e.g., $V_{DS} = 0.1$ V). Hence, for small V_{DS}, (1)–(3) can be rearranged for various gate voltages as follows:

$$R_T = R_{ds}(V_{GS}) + [(L_m - \Delta L)/\mu_0\, C_{OX} W][1/(V_{GS} - V_T) + \theta] \tag{5}$$

where the denominator term in (2), $V'_{GS} - V_T - 0.5aV'_{DS} \cong V_{GS} - V_T$ by applying $V'_{GS} = V_{GS} - 0.5I_D R_{Ds}$ and $V'_{DS} = V_{DS} - I_D R_{ds}$. Here, $a \cong 1$, $\eta \cong 0$, and $V_{GS} - V_T >> 0.5aV_{DS}$ at small V_{DS}. $L = L_m - \Delta L$, where L_m is the masked channel length and ΔL is the channel length reduction due to process bias and the lateral diffusion. In a similar manner to that of De La Moneda's method [7] by plotting R_T versus $(V_{GS} - V_T)^{-1}$ for the transistors with different channel lengths, a family of curves can be obtained as shown in Fig. 1. Using the least squares fit, the slope of these curves is $1/\beta_0\ (= L_m - \Delta L/\mu_0 C_{OX} W)$. Again, a plot of $1/\beta_0$ against L_m in the insert of Fig. 1 gives a straight line from which the intercept gives ΔL and the slope gives μ_0.

Unlike in the method used by Suciu *et al.* [3] or De La Moneda *et al.* [7], we use the measured data in Fig. 1 and plot R_T versus L_m for a set of transistors at various gate biases, and a family of curves is obtained as shown in Fig. 2. Here, the value of R_{ds} at each $V_{GS} - V_T$ bias can be obtained from (3) by drawing a vertical line at ΔL in Fig. 2 and its intercept with the curves gives R_{ds}. Values of R_{ds} are then plotted against $V_{GS} - V_T$ and can be fitted by an empirical form as shown in Fig. 3 which can be easily implemented in a previous analytical *I–V* model [6]. With various gate voltages applied for LDD structure device, the n^- region is *partially depleted* and results in larger values of resistance at lower gate voltages while it is *fully depleted* at very high gate voltages and as a result exhibits smaller resistances. This confirms the re-

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The authors are with the Department of Electronic Engineering and the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, ROC.

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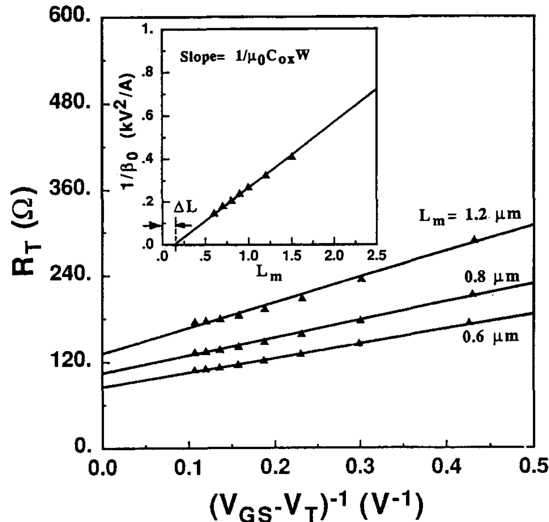

Fig. 1. Plot of R_T versus $(V_{GS} - V_T)^{-1}$ for various channel lengths to determine the effective channel length. $\Delta L = 0.13$ μm and $\mu_0 = 525$ $cm^2/V \cdot s$.

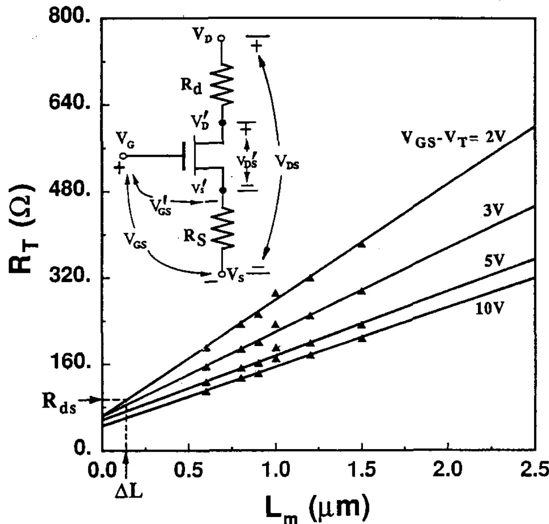

Fig. 2. Plot of R_T versus L_m at various gate voltages for determining R_{ds}. The insert gives the equivalent circuit model of an LDD MOS device.

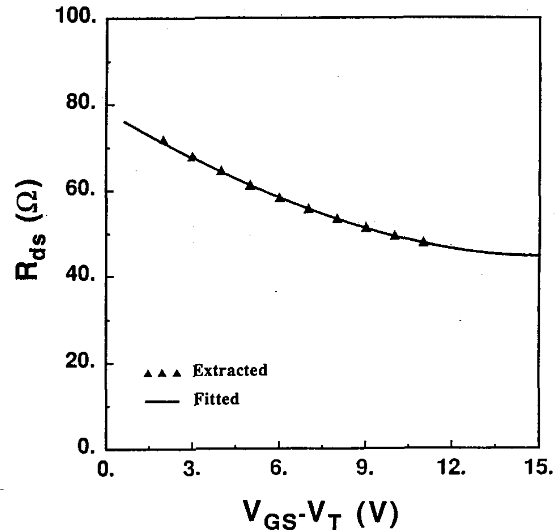

Fig. 3. Variation of the extracted drain-and-source series resistance with the gate voltage. Solid lines can be fitted by an empirical form as $R_{ds} = R_0 + R_1 (V_{GS} - V_T) + R_2(V_{GS} - V_T)^2$, where $R_0 = 78.9$, $R_1 = -4.1$, and $R_2 = 0.12$.

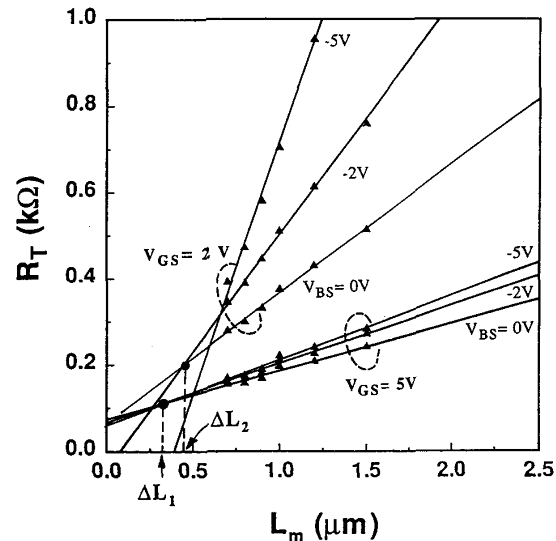

Fig. 4. Extraction of ΔL using the method in [4]. Note that different ΔL's are obtained for different gate voltages, $\Delta L_1 = 0.32$ μm, $\Delta L_2 = 0.44$ μm.

sults in Fig. 3 that R_{ds} decreases with the increasing gate voltages. Furthermore, once ΔL and R_{ds} have been found, θ can be determined as follows. It can be extracted from Fig. 1 by using the limiting value of R_{ds} at very high gate voltages, which is about 45 Ω in this case from Fig. 3. At very high gate voltages, the second term in (5) vanishes and so θ can be calculated from the intercept of the straight lines with the vertical axis using R_{ds} and ΔL values as obtained above. All different channel length devices have different intercept values and so the resultant θ is channel-length-dependent.

III. Comparison with Reported Methods

Comparisons between the present method and the other methods to characterize R_{ds} are described as follows. The results shown in Fig. 4 to determine the ΔL using the method in [4] have been taken for the same device. One ambiguous situation encountered in [4] is that ΔL is not uniquely defined since for different values of gate voltages, we may obtain different values of ΔL. The method in [4] used an arbitrary gate voltage to extract the ΔL value. Also, each curve at the same gate voltage will not necessarily cross at the same point which is even worse due to the experimental uncertainty. This will leave the experimental procedure inaccurate. In the present method, however, ΔL is uniquely defined based on a given set of I-V equations and hence is much better than the previous method. In the modeling of the drain-and-source resistance effect such as in

Suciu *et al.* [3] or De La Moneda *et al.* [7], a fixed value of R_{ds} approaches is obtained (which is about 45 Ω) by the extrapolation of R_T versus L_m or $(V_{GS} - V_T)^{-1}$ at a limiting value of very high gate voltage or $(V_{GS} - V_T)^{-1} = 0$. Unfortunately, these methods can only be applied to a device with gate-voltage-independent drain-and-source resistance (e.g., conventional MOS device). For LDD or partially overlapped drain structure MOS devices, R_{ds} should be gate-voltage-dependent due to the modulation of the depletion regions in the n^- region by the gate voltages. As a consequence, a fixed resistance model [3], [7] will further lose accuracy to model the linear region *I-V* characteristics.

Although the effective channel length, L, or ΔL, is also gate-voltage-dependent as revealed in [5], this will complicate the computation of an *I-V* model for practical circuit simulation application. Hence, for a tradeoff between computational efficiency and accuracy for real applications, gate-voltage-independent property (i.e., constant ΔL is assumed for different gate biases) is assumed and used here. The validity of this assumption can be justified by comparing the modeled and experimental *I-V* characteristics, in which excellent agreements can be achieved by using the present modeled ΔL, R_{ds}, and θ values in our model equations in [6]. Therefore, we believe that the proposed method based on a consistent set of ΔL and R_{ds} should be more reliable than the above methods.

IV. Conclusion

In this brief, a novel approach to extract the drain-and-source series resistance and the effective channel length from the measured *I-V* characteristics of LDD MOS devices has been proposed. The gate-voltage-dependent characteristics of the drain-and-source series resistance have been adequately demonstrated. The procedure is quite simple and the extracted results are well suited for circuit simulation use, such as in SPICE.

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Measurements of Gate Voltage Dependence of Electron Mobility in δ-Doped HFET's

Byung-jong Moon, Seonghearn Lee, Michael Shur, Hadis Morkoç, and Anand Gopinath

***Abstract*—We report the results of the measurements of the gate voltage dependence of the electron mobility in Heterostructure Field Effect Transistors (HFET's) using a spilt *C-V* technique. This method allows us to deduce this dependence without making any assumptions about other parameters such as the threshold voltage. The dependence of the electron mobility in the HFET channel on the gate voltage depends on the heterointerface quality. In some samples, the mobility increases with the increase of the gate voltage. In other samples (grown on a different Molecular Beam Epitaxy machine), the mobility drops to nearly a half of its maximum value at high gate voltages. This means that, in these samples, the electron mobility is strongly dependent on the transverse electric field (similar to an analogous behavior in p- and n-channel MOSFET's).**

The electron and hole mobilities in n- and p-channel Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET's) depend on the gate voltage because the effective transverse electric field determines the degree of localization of the carrier inversion layer at the interface between the semiconductor and gate insulator and thus affects surface scattering. These dependencies must be accounted for in MOSFET modeling (see, for example, [1], [2]). In Heterostructure Field-Effect Transistors, the low-field mobility μ also plays an important role in determining the device performance. In spite of the original name for these devices—High Electron Mobility Transistors (HEMT's)—the values extracted from the *I-V* measured characteristics of short-channel AlGaAs/GaAs HFET's (with gate length of 1 μm or less) are usually quite low (ranging from 500 to 5000 $cm^2/V \cdot s$). A reliable, *in situ* measurement of the field-effect mobility in HFET's is very important for HFET modeling and characterization as well as for a better understanding of physical mechanisms determining the value of the mobility. In addition, the Hall mobility does not always represent the channel mobility. Hence, it is not appropriate to use the Hall mobility as the channel mobility in the modeling.

From the device modeling point of view, it is absurd to use the constant channel mobility regardless of the gate voltage. For the better model, it is necessary to include the dependence of the low-field channel mobility upon the gate voltage.

In n-channel Heterostructure Field Effect Transistors (HFET's), the electron Hall mobility may increase with the gate voltage because the increase in surface carrier concentration leads to a more effective screening of impurity scattering [3]. The effective field-effect mobility exhibits a similar behavior for the same reason [4].

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B. Moon is with Vitesse Semiconductor Corp., Camarillo, CA 93012.
S. Lee is with the Electronics and Telecommunication Research Institute, Daejon, Korea.
M. Shur is with the Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903.
H. Morkoç is with the University of Illinois at Urbana Champaign, the Coordinated Science Laboratory, and the Materials Research Laboratory, Urbana, IL 61801.
A. Gopinath is with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455.

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