Journal of The Electrochemical Society, **149** (7) F69-F72 (2002)
0013-4651/2002/149(7)/F69/4/$7.00 © The Electrochemical Society, Inc.

RF Noise Characteristics of High-*k* $AlTiO_x$ and Al_2O_3 Gate Dielectrics

S. B. Chen,[a] C. H. Huang,[a] Albert Chin,[a,z] J. Lin,[b] J. P. Jou,[b] K. C. Su,[b] and J. Liu[b]

[a]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan*
[b]*United Microelectronic Corporation, Science-Based Industrial Park, Hsinchu, Taiwan*

We have characterized the radio frequency (rf) noise in high-*k* Al_2O_3 and $AlTiO_x$ gate dielectrics, which have respective effective oxide thickness (EOT) of 17.2 and 12.5 Å. The measured noise figure in gate dielectric is material dependent and sensitive to dielectric defect after stress. Although the high-*k* $AlTiO_x$ gate dielectric has lower EOT, it has a higher noise figure than others. From the simulation in our proposed equivalent circuit model, the dominant noise is thermal noise and the reason for increasing noise figure after stress is due to additional parallel resistance by trap-assisted tunneling.
[DOI: 10.1149/1.1482055]

Manuscript submitted October 9, 2001; revised manuscript received January 25, 2002. Available electronically May 23, 2002.

One important direction of next generation metal-oxide semiconductor field effect transistors (MOSFETs) is the replacement of thermal oxide with high-*k* dielectrics. However, the scaling of complementary metal oxide semiconductors (CMOS) has resulted in a strong improvement in the radio frequency (rf) characteristics that causes Si-based CMOS devices currently to be used in rf front-end integrated circuits (ICs) for wireless communication applications. Unfortunately, in spite of the fast progress and good achievement in high-*k* gate dielectric,[1-4] there is no rf performance of high-*k* gate dielectric reported so far. Among various rf performance characteristics, rf noise is one of the important factors for Si MOSFETs because noise is the key characteristic for some rf circuits, such as low-noise amplifiers in rf receivers.[5,6] In addition to channel thermal noise, it is suspected that the noise originating from the large gate leakage current in either conventional SiO_2 or high-*k* gate dielectric may be a serious concern in the noise performance of MOSFETs. In this paper, we have characterized the rf performances of high-*k* Al_2O_3 and $AlTiO_x$ capacitors and compared with thermal SiO_2. The measured noise figure is dependent on material and very sensitive to the existing dielectric defects and stress-induced defects. From analysis using an equivalent circuit model, the noise source is thermal noise and the stress effect generates additional shunt resistance in parallel with capacitor that increases the thermal noise. Therefore, achieving good rf noise characteristics is another important consideration for choosing suitable high-*k* dielectric materials.

Experimental

High-*k* Al_2O_3 and $AlTiO_x$ capacitors with coplanar transmission lines[7,8] fabricated on Si substrates are used for rf noise characterization. First, the n^+ Si bottom transmission line is formed. Then high-*k* Al_2O_3 or $AlTiO_x$ is formed by depositing Al or Ti/Al on HF-vapor passivated Si[9] followed by oxidation and annealing. A more detailed fabrication process of high-*k* Al_2O_3 dielectric can be found elsewhere.[4] It is found in our previous study that the self-limiting oxidation mechanism is one of the important merits of Al_2O_3 for either reproducibility or uniformity control. The advantages of adding Ti-O into Al_2O_3 is to reduce effective oxide thickness (EOT) by adding the very high-*k* TiO_x and at the same time preserve the slow oxygen diffusion through Al-O matrix. Negligible EOT reduction is measured after 800°C annealing due to the Al-O related self-limiting oxidation mechanism like Si_3N_4. Finally, the Al top transmission line is patterned to form the rf high-*k* capacitor. Standard two-port S-parameters and rf noise figures are measured and de-embedded for high-*k* capacitors and 0.18 μm MOSFETs.[7,8] The noise figure and associated gain were measured by an ATN-NP5B noise parameter extraction system up to 6 GHz that covers the most important frequency band for wireless communication.

Results and Discussion

We have first measured the low-frequency characteristics of high-*k* $AlTiO_x$ and Al_2O_3. Figure 1 shows the capacitance-voltage (C-V) characteristics of different dielectric capacitors. The flat C-V characteristics with little capacitance change are due to the highly doped n^+-Si bottom transmission line and the large threshold voltage. The EOT of 12.5 and 17.2 Å are obtained from directly calculating the measured capacitance values without quantum correction.[9] The calculated *k* values of 15 and 9 are obtained for $AlTiO_x$ and Al_2O_3, respectively. Thus, adding Ti-O into Al-O gate dielectric can effectively increase the *k* value.

Figure 2a and b shows the current density *vs.* voltage (J-V) characteristics of various gate dielectrics and the current density change (ΔJ) after constant voltage stress, respectively. The leakage current of $AlTiO_x$ at the bias voltage of 1 V is about three orders of magnitude less than that of conventional SiO_2 at the same EOT reported in the literature.[10] The relatively larger leakage current in $AlTiO_x$ than Al_2O_3 may be due to both smaller bandgap[11] and weaker bond-related higher defects in Ti-O.[4] However, the lower EOT can be obtained for $AlTiO_x$ due to the higher dielectric constant, even

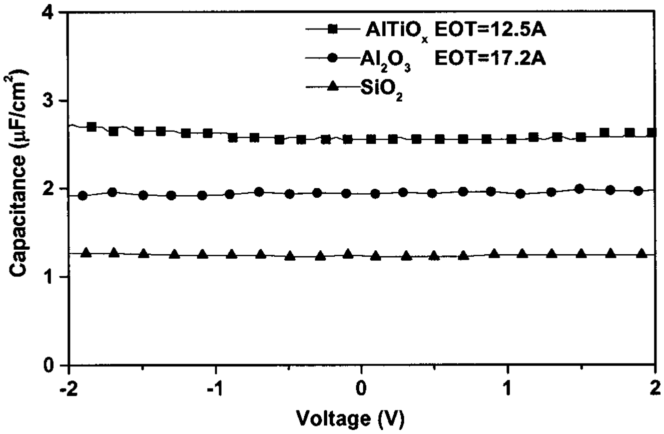

Figure 1. C-V characteristics of the Al_2O_3 and $AlTiO_x$ gate capacitors measured at 100 kHz. Conventional 23 Å SiO_2 is also added for comparison. The measured area is 20 × 20 μm.

[z] E-mail: achin@cc.nctu.edu.tw

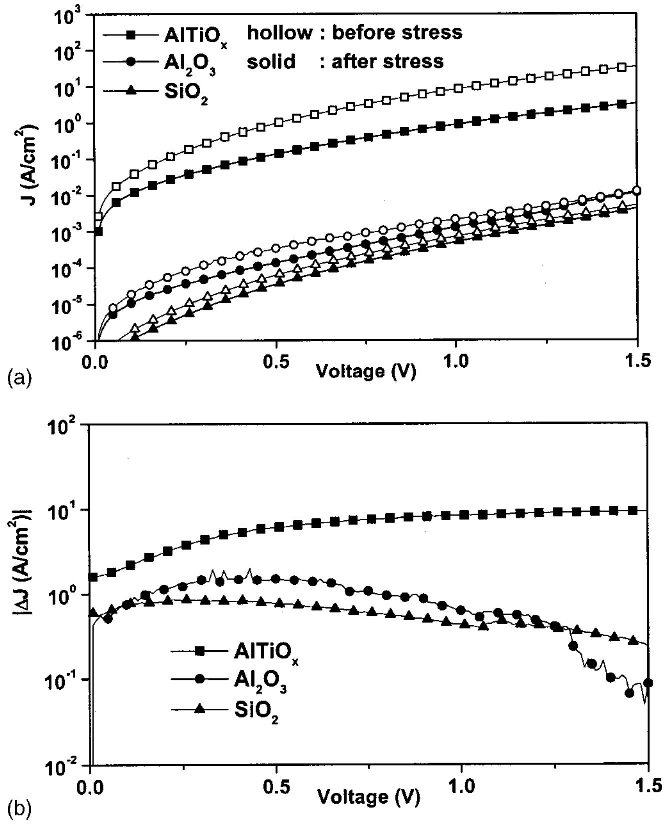

Figure 2. Stress-induced leakage current of the Al_2O_3 and $AlTiO_x$ gate capacitors. Conventional SiO_2 is also added for comparison.

though the bandgap is smaller,[11] and the achieved EOT is smaller than the stacked TiO_2-Si_3N_4 gate dielectric.[3] The larger increasing leakage current in $AlTiO_x$ after stress also indicates the weaker bonding in Ti-O. This increase in stress-induced leakage current (SILC) is caused by the generation of defects during stress that can be further used for noise mechanism study.

To investigate the effect of stress on noise and identify the noise mechanism, we have further measured the rf noise of devices before and after stress. Figures 3a-c shows the measured noise figure as a function of frequency for $AlTiO_x$, Al_2O_3, and SiO_2, respectively. The noise figure in a fresh device increases as increasing k from SiO_2 to $AlTiO_x$. The Al_2O_3 shows the lowest noise figure increase after stress and the $AlTiO_x$ is the worst. Therefore, from the rf noise point of view, the Al_2O_3 gate dielectric performs better than $AlTiO_x$. It is known that the Al-O bond energy is higher than Ti-O; thus, the origin of noise after stress may be related to defect generation and current fluctuation inside the gate dielectric.

We have further investigated the origin of noise. Since the stress effect increases the leakage current by trap-assisted tunneling, the shot noise may be responsible for the rf noise because it originates from the random carrier injection through the energy barrier of the gate dielectric. However, this is unlikely because the shot noise usually decreases rapidly as frequency increases into the gigahertz regime.[12] We have used an equivalent circuit model to further understand the origin of noise. Figure 4 shows the proposed noise model for high-k capacitors. This model contains a gate capacitor (C) in parallel with a resistor (G), which is used to simulate the leakage-current-related loss effect of the capacitor. Because the stress increases the leakage current, additional resistance (R) is added to model the SILC effect.

Figure 5a-c shows the simulated noise figure using the physically based equivalent circuit model for $AlTiO_x$, Al_2O_3, and SiO_2, respectively, where the good matching of measured and modeled results were first obtained before optimizing the noise figure in the model.[5] We have also plotted the measured data for comparison. The good agreement between the measured and modeled noise figure suggests the excellent accuracy of this model. Therefore, the origin of rf noise in the high-k capacitor is due to the loss-related thermal noise.

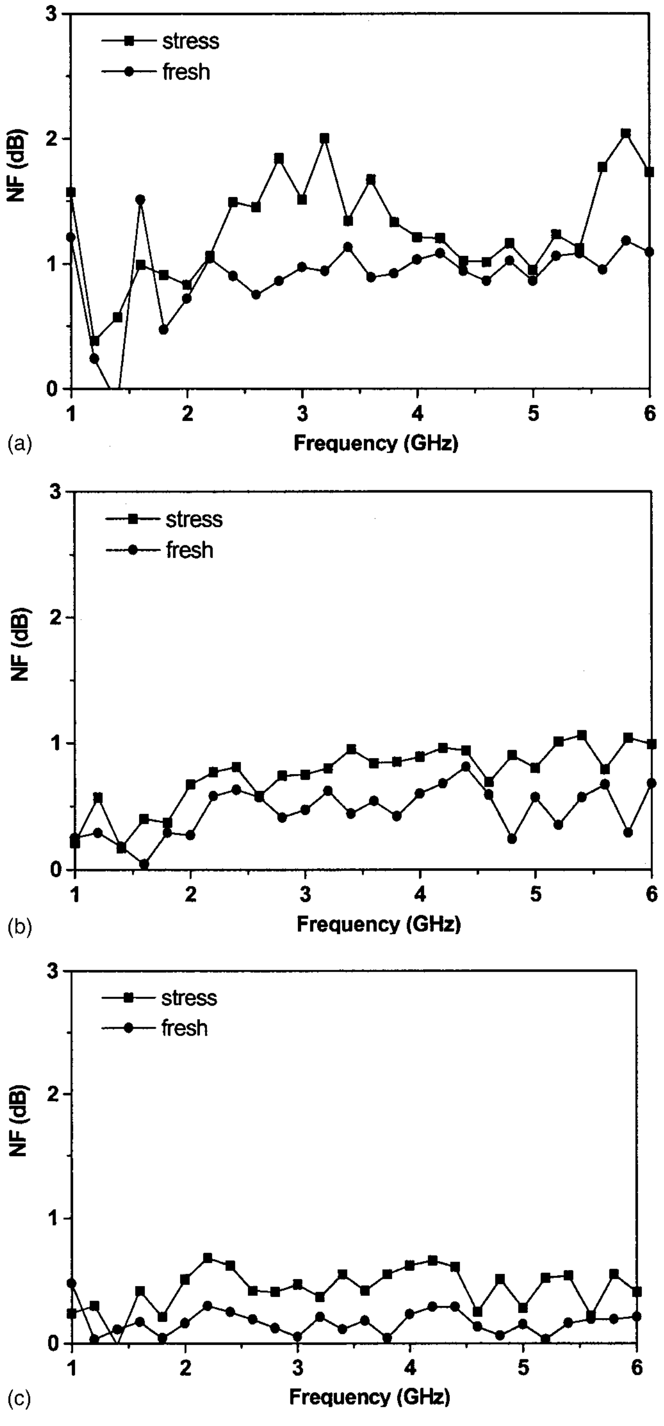

Figure 3. Noise figure spectra of (a) $AlTiO_x$, (b) Al_2O_3, and (c) SiO_2 gate capacitors.

To understand the gate-oxide-related rf noise in MOSFETs, we have also shown the measured and simulated minimum noise figure from a multifingered 0.18 μm MOSFET in Fig. 6a and the equivalent circuit model is in Fig. 6b. The gate oxide for this device is conventional SiO_2 and the thickness is 30 Å. Close matching be-

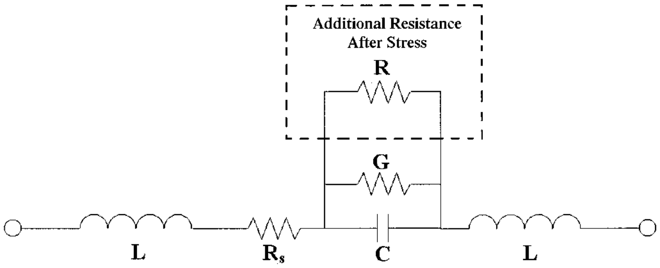

Figure 4. The proposed noise model for gate capacitors.

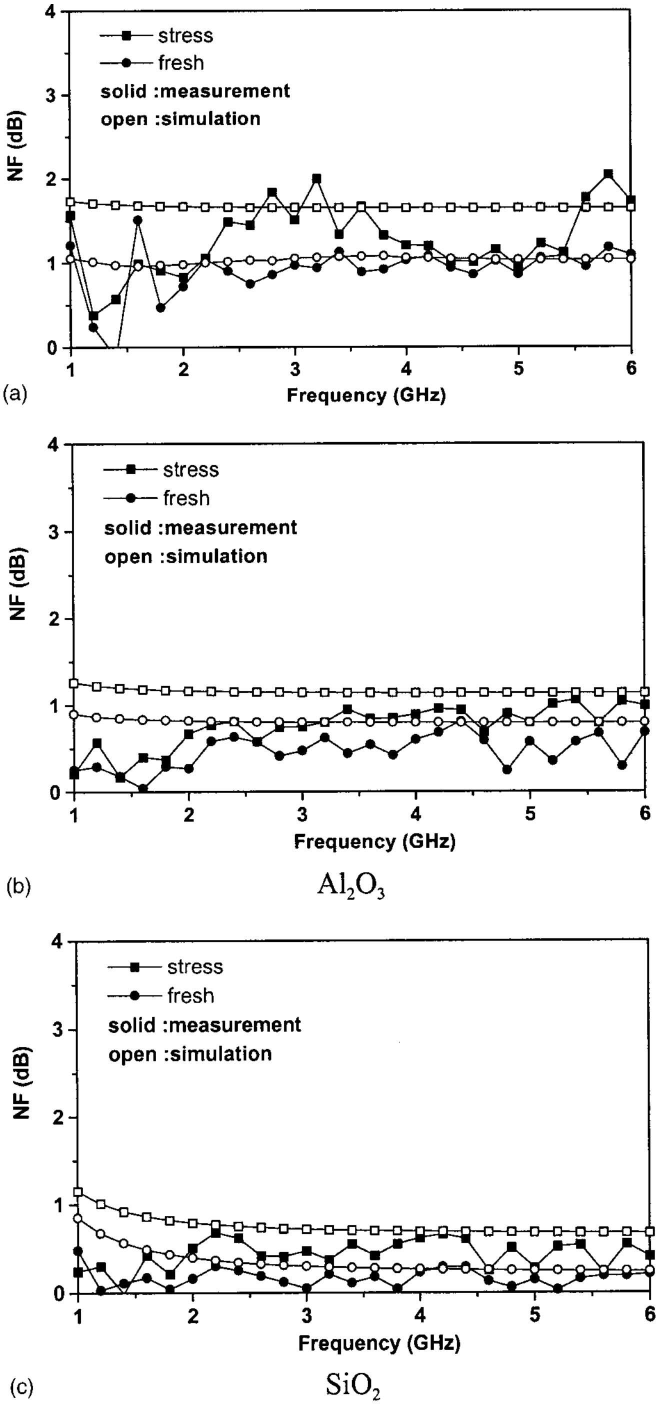

Figure 5. The simulated noise figure spectra of (a) $AlTiO_x$, (b) Al_2O_3, and (c) SiO_2 gate capacitors.

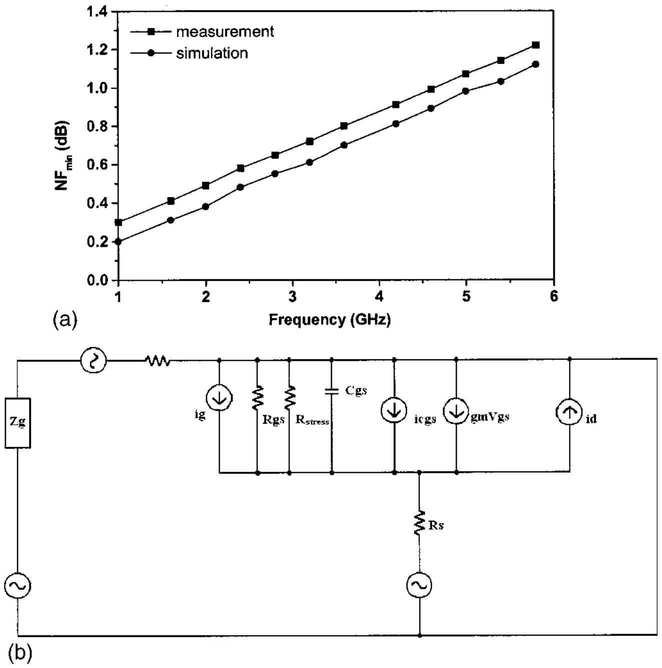

Figure 6. (a) Measured and simulated minimum noise figure for a multifingered 0.18 × 5 μm MOSFET with 21 gate fingers in parallel, and (b) the noise model for (a). Additional gate noise is included in noise current i_g for future high-*k* MOSFETs.

tween the measured and modeled noise figure indicates the good accuracy of the noise model. However, by continuously scaling down the gate dielectric thickness or replacing by high-*k* dielectric in the next generation CMOS technologies, significant thermal noise from gate dielectric resistance (R_{gs}) and resistance (R_{stress}) by SILC effects will result in higher noise in MOSFETs according to the transistor noise model. In the worst case, the gate dielectric noise may contribute a large portion of total noise.

Conclusions

We have characterized the rf noise of high-*k* $AlTiO_x$ and Al_2O_3 gate dielectrics. The dominant noise source in gate capacitors is thermal noise that increases after stress due to additional leakage-related resistance by SILC effects.

Acknowledgments

This work was sponsored by the National Science Council under contract NSC89-2215-E-009-100 and United Microelectronic Corporation.

National Chiao Tung University assisted in meeting the publication costs of this article.

References

1. S. J. Lee, H. F. Luan, C. H. Lee, T. S. Jeon, W. P. Bai, Y. Senzaki, D. Roberts, and D. L. Kwong, *Symposium on VLSI Technology*, p. 133 (2001).
2. L. Kang, Y. Jeon, K. Onishi, B. H. Lee, W.-J. Qi, R. Nieh, S. Gopalan, and J. C. Lee, *Symposium on VLSI Technology*, p. 44 (2000).
3. X. Guo, X. Wang, Z. Luo, T. P. Ma, and T. Tamagawa, Tech. Dig. Int. Electron Devices Meet., **1999**, 137.
4. A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, *Symposium on VLSI Technology*, p. 135 (1999).
5. K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, *IEEE MTT-S International Microwave Symposium*, p. 763 (2001).
6. G. Knoblinger, P. Klein, and H. Tiebout, *IEEE J. Solid-State Circuits*, **32**, 831 (2001).
7. Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, C. P. Liao, S. C. Pai, and C. C. Chi, *IEEE MTT-S International Microwave Symposium*, p. 221 (2000).

8. Y. H. Wu, A. Chin, C. S. Liang, and C. C. Wu, *Radio Frequency Integrated Circuits Symposium*, p. 151 (2000).
9. A. Chin, W. J. Chen, T. Chang, R. H. Kao, B. C. Lin, C. Tsai, and J. C.-M. Huang, *IEEE Electron Device Lett.*, **EDL-18**, 417 (1997).
10. S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, *IEEE Electron Device Lett.*, **EDL-18**, 209 (1997).
11. S. A. Campbell, D. C. Gilmer, Xiao-Chuan Wang, Ming-Ta Hsieh, Hyeon-Seag Kim, W. L. Gladfelter, and Jinhua Yan, *IEEE Trans. Electron Devices*, **44**, 104 (1997).
12. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., p. 750, John Wiley & Sons, New York (2001).