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Poly-Si Thin-Film Transistors Crystallized by Electron-Beam Annealing

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We have investigated an alternative electron-beam crystallization method for poly-Si thin-film transistor application. In contrast to the high crystallization temperature and long duration of conventional furnace crystallization, electron-beam crystallization could be performed at a low thermal budget even without substrate heating. It also provides better device characteristics than conventional furnace annealing, including smaller threshold voltage, higher mobility, smaller subthreshold swing, and larger I_{ON}/I_{OFF} ratio. The much smoother surface than the excimer laser annealed sample is also important for further gate oxide integrity and device performance improvement.
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Polycrystalline Si (poly-Si) thin-film transistors (TFTs)[1-5] have aroused widespread attention due to their applications for active matrix liquid crystal displays. Conventionally, the as-deposited amorphous Si is annealed by furnace to transform its crystallinity to polycrystalline. The furnace annealing method has the advantage of simplicity and good uniformity[1] but requires a high thermal budget of high process temperature (600°C) and long duration (15-48 h). To reduce the thermal budget, other crystallization techniques have been proposed, such as microwave annealing,[2] metal-induced lateral crystallization (MILC),[3,4] and excimer laser crystallization.[5,6] However, microwave annealing is still performed at relatively high temperature (500°C) and long annealing duration (12 h).[2] The MILC process can have a lower thermal budget than furnace crystallization, but it still requires long annealing time (several hours)[3] and is suspected to have metal contamination issues.[7,8] Although excimer laser crystallization has the advantage of low thermal budget, it suffers from surface roughness[6] and related uniformity difficulties that may prohibit further scaling down the gate oxide[9-11] and device performance improvement. In this work, we have studied the device performance of TFTs crystallized by electron-beam annealing[12] without the capping layer. Superior device performance of electron-beam crystallized TFTs over furnace annealing was achieved, even under a room substrate temperature. The relatively smooth surface is also another merit of this method for gate oxide integrity[9-11] and device performance improvement. However, it is important to notice that the electrical properties of TFTs are still inferior to excimer laser crystallized Si. Further pulsed mode and scan operation are required to reduce the gap between these two technologies.

Experimental

Thermally oxidized 4 in. Si(100) wafers were used as the substrates for TFTs. First, a 1000 Å amorphous Si channel layer was deposited by low-pressure chemical vapor deposition (LPCVD) using SiH_4. Then the wafers were annealed in an electron-beam system under vacuum for 2 min without any substrate heating, and the applied electron-beam current density, size, and voltage were 12.7 mA/cm^2, 0.79 cm^2, and -7 kV, respectively. We have attempted and achieved the optimized dose of 7.8×10^{18} cm^{-2} in our system. Above this dose, the continuous electron-beam would damage the underneath oxide and lead to mobility degradation. After active island definition, a 1000 Å silicon dioxide gate dielectric was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300°C. After gate definition of deposited 3000 Å poly-Si, the gate and source-drain regions were implanted by phosphorus at 30 keV and 4×10^{15} cm^{-2} followed by 600°C activation. Then a 3000 Å silicon dioxide passivation layer is deposited and patterned, and Al electrodes were formed by thermal evaporation. Finally, the samples were sintered at 400°C for 30 min in N_2 ambient. The gate dimension of TFTs is 10×40 μm. For comparison, conventional furnace crystallized TFTs at 600°C for 24 h were also fabricated.

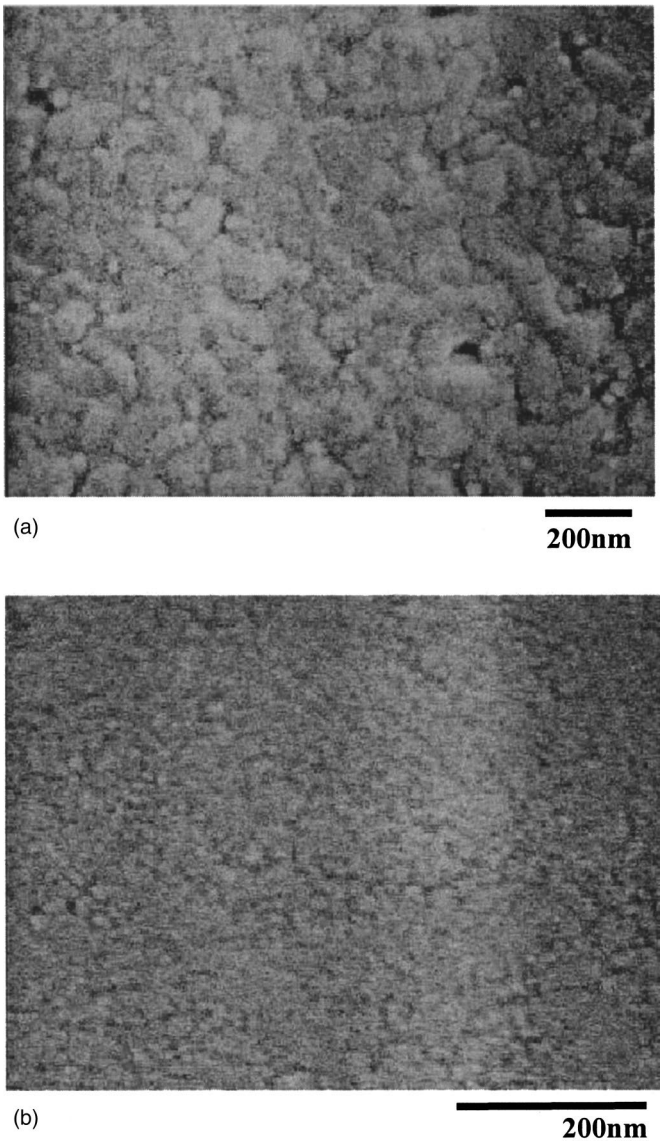

Figure 1. SEM photographs of poly-Si crystallized by (a) electron-beam and (b) furnace annealing.

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Table I. Summary of important device parameters of poly-Si TFTs crystallized by electron-beam and furnace annealing.

	V_{th} (V)	SS (V/dec)	μ_{FE} (cm^2/V s)	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF} ratio	N_t (10^{12} cm^{-2})
Furnace annealing	8.8	1.97	10.7	22.7	79.4	2.92×10^5	5.22
Electron-beam annealing	5.4	1.47	18.4	93.9	89.7	1.05×10^6	3.28

Results and Discussion

Figures 1a and b show the SEM photographs for electron-beam and conventional furnace crystallized poly-Si, respectively. The average grain size for electron-beam crystallization is ~2000 Å, while that of furnace crystallization is only 200 Å. Therefore, the electron-beam crystallization produces much larger poly-Si grain size than conventional furnace and close to excimer laser crystallized poly-Si.[6] The large grain size and the reduced grain boundary area are the important factors for electrical characteristic improvement. The mechanism for achieving the large grain size may be due to the electron-beam energy absorbed by amorphous Si. The electron-beam annealing can fix more defect densities than conventional furnace annealing because of the concentrated energy density. This is evidenced from the lower interface trap density (N_t) by electron beam annealing shown in Table I.

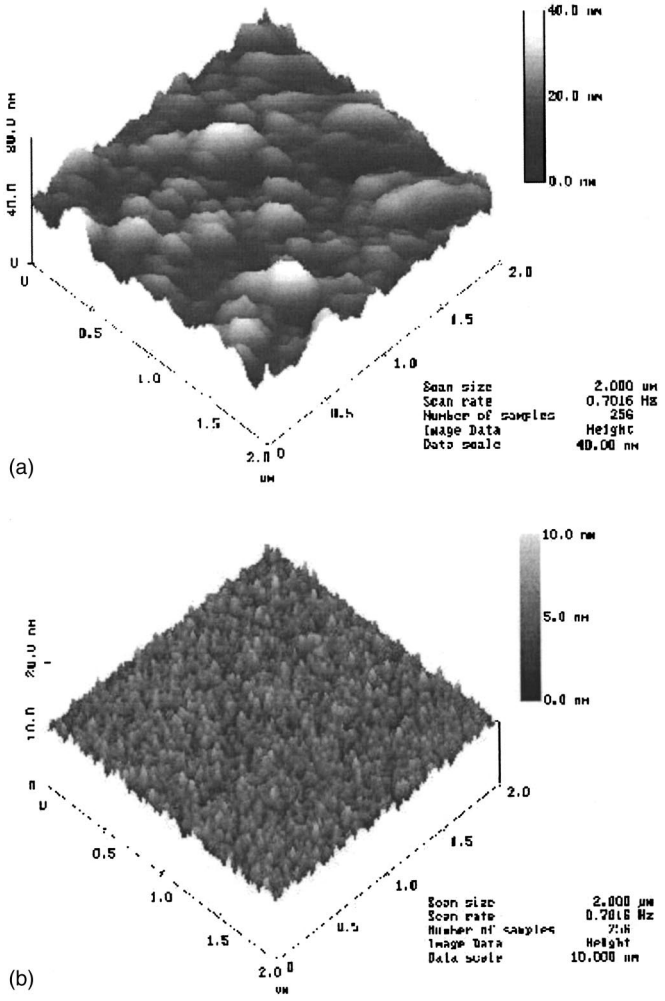

Figure 2. AFM images of poly-Si by (a) electron-beam and (b) furnace annealing.

Although the large grain size is desired, the surface roughness is another important issue because it is directly related to gate oxide integrity.[9-11] Figures 2a and b show atomic force microscopy (AFM) images of electron-beam and conventional furnace crystallized poly-Si, respectively. The root-mean-square (rms, peak) roughness values are 5.0 Å (52 Å) and 31.5 Å (335 Å) for furnace and electron-beam crystallized poly-Si, respectively. Although both rms and peak roughness are larger for poly-Si crystallized by electron-beam than furnace, these values are much lower than excimer laser crystallized poly-Si[6] and therefore good gate oxide reliability is expected. Besides, the electron-beam crystallization preserves the advantages of low thermal budget and continuous scanning operation similar to excimer laser crystallization.

Figure 3 shows I_d-V_g characteristics of poly-Si TFTs crystallized by electron-beam and furnace annealing, and the measured device parameters are summarized in Table I. The electrical characteristics for conventional furnace-crystallized TFTs are comparable to the data published in the literature,[13] suggesting the good device quality of our control sample. In contrast, the electron-beam crystallized TFTs have a low threshold voltage of 5.4 V, a small subthreshold swing of 1.47 V/dec, and a high I_{ON}/I_{OFF} ratio of 1.1×10^6 as compared with our furnace-crystallized TFTs. Apparently, electron-beam crystallization provides better device characteristics than furnace crystallization.

To understand the improved drain current, we have further plotted the electron field-effect mobility in Fig. 4. The peak field-effect mobility of electron-beam crystallized TFTs achieves a value of 18 cm^2/V s, while the mobility by furnace crystallization is only 10 cm^2/V s. The higher mobility in electron-beam crystallized TFTs is consistent with the larger grain size in Fig. 1 and smaller trap-state density in Table I. It is important to notice that although the mobility improvement is only ~80% as compared with the 600°C furnace-crystallized device, the electron-beam crystallization is performed at a room substrate temperature that has high potential for further low thermal budget TFT application. Further mobility improvement is expected using grain boundary passivation for electron-beam crys-

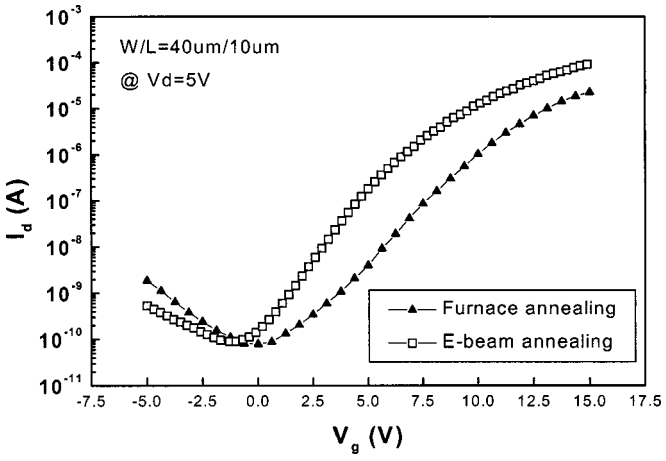

Figure 3. I_d-V_g characteristics of TFTs with poly-Si films crystallized by electron-beam and furnace annealing at 600°C for 24 h.

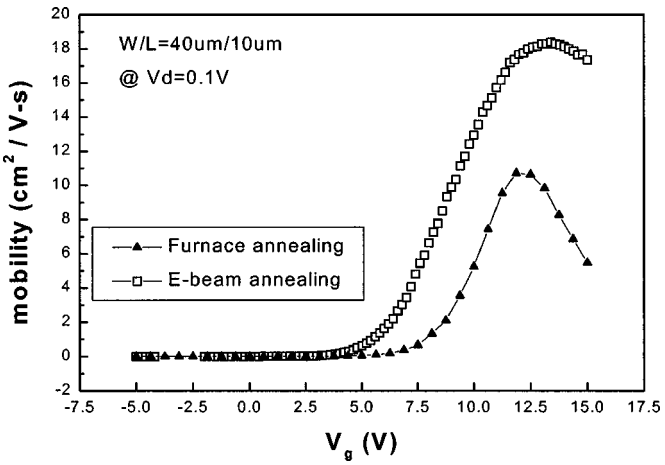

Figure 4. Field-effect mobility *vs.* gate voltage for both electron-beam annealed and furnace-annealed TFTs.

tallized poly-Si TFTs. Operating the electron-beam annealing under pulsed mode may also improve the electrical characteristics because a higher dose can be used without damaging the material underneath. This method is similar to excimer laser operation conditions and may be able to reduce the electrical performance gap between them. The modified electron-beam system with pulsed mode and scanning operation has the potential for real production, because the current system is already commercialized for evaporation and deposition similar to sputter or thermal evaporator systems.

Conclusion

We have studied the device performance of poly-Si TFTs crystallized by electron-beam annealing. In comparison to conventional furnace annealing, electron-beam annealing has the advantages of low crystallization temperature and short annealing duration. Furthermore, the electron-beam crystallized TFTs provide better device performance than furnace-annealed TFTs. The smooth surface is also the merit of this annealing technique as compared with excimer laser crystallized TFTs, which is important for gate oxide integrity and further device performance improvement.

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