A New Process-Variation-Immunity Method for Extracting Capacitance Coupling Coefficients in Flash Memory Cells

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***Abstract*—Overestimation of capacitance coupling coefficients in flash memory cells is encountered in the subthreshold slope method. By means of a two-parameters subthreshold current model $I_D = I_o \exp[q(V_{GB} - nV_{SB})/nkT]$, a mathematical formulation of the subthreshold swing ratio in the subthreshold slope method is constructed to isolate the measurement errors caused by process variations from the errors traditionally caused by bulk capacitance coupling. To minimize the effect of process variations, a new method is developed based on the model. In this method, the control gate voltage shift due to weak body effect is measured in flash memory cells in subthreshold, while the corresponding slope factor n is adequately deduced from threshold voltage versus source-to-substrate bias measurement in dummy devices. The corrected capacitance coupling coefficients show large improvements compared to the design values, and the updated errors are found to be close to that caused solely by bulk capacitance coupling. The method is also fast since only a small source-to-substrate bias of 0.1 V is needed for implementation of weak body effect, and thereby it can be used as an in-line monitor of capacitance coupling coefficients.**

***Index Terms*—Body effect, capacitance coupling, flash memory, mismatch, MOSFETs, subthreshold.**

I. Introduction

CAPACITANCE coupling coefficients are a very important performance parameter in flash memory cells. Particularly, high-speed write/erase operations can be promised provided that capacitance coupling coefficients are well controlled. Thus, precise extraction of capacitance coupling coefficients in a flash memory manufacturing process is essential. To meet fast extraction requirements, the subthreshold slope method dedicated to a pair of test vehicles (i.e., flash memory cells and dummy transistors) was devised [1] and very recently was reported to be the most accurate [2] in terms of a small error of typically 0.03 due to bulk capacitance coupling (see [2, Fig. 3]). On the other hand, current mismatch between identically drawn devices due to process variations can be more prominent if biased in subthreshold [3]–[7]. In other words, the subthreshold slope method should show considerable sensitivities to current mismatch between flash memory cells and dummy transistors, a concerned issue not yet clarified fully before [2]. In this work we will figure out that the subthreshold slope method can produce an error as large as 0.13 and an existing subthreshold conduction model can identify process variations, rather than traditionally bulk capacitance coupling, as the primary origin of the errors. To minimize the effect of process variations, a new method is straightforwardly developed.

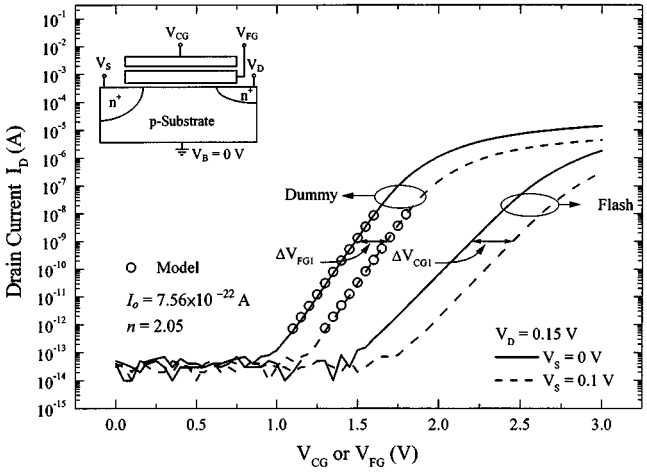

Fig. 1. Drain currents measured as a function of control gate voltage (V_{CG}) in flash memory cell and floating gate voltage (V_{FG}) in dummy transistor. $V_D = 0.15$ V and $V_S = 0$ and 0.1 V. The extracted control gate voltage shift (ΔV_{CG1}) and floating gate voltage shift (ΔV_{FG1}) are labeled at specific subthreshold current level of 10^{-9} A. The extracted values of I_o and n for two subthreshold current–voltage (I–V) of a dummy transistor are shown.

II. Subthreshold Slope Method

The NOR-type gate stack flash memory cells with gate width and length of 0.45 μm and 0.4 μm respectively were used in this work. The dummy transistors were identically drawn flash memory cells but with control gate shorted to underlying floating gate. They were manufactured by a 0.4 μm process technology with 100 Å thick tunnel oxide. The substrate was tied to ground (substrate bias $V_B = 0$) throughout the work. Fig. 1 shows the measured drain current at drain voltage $V_D = 0.15$ V and source voltage $V_S = 0$ versus control gate voltage (V_{CG}) in flash devices and floating gate voltage (V_{FG}) in dummy devices, respectively. The subthreshold slope method yielded subthreshold swing ratios as depicted in Fig. 2 for four different die positions on wafer, which are unreasonably high as compared with the design values of about 0.6. The error,

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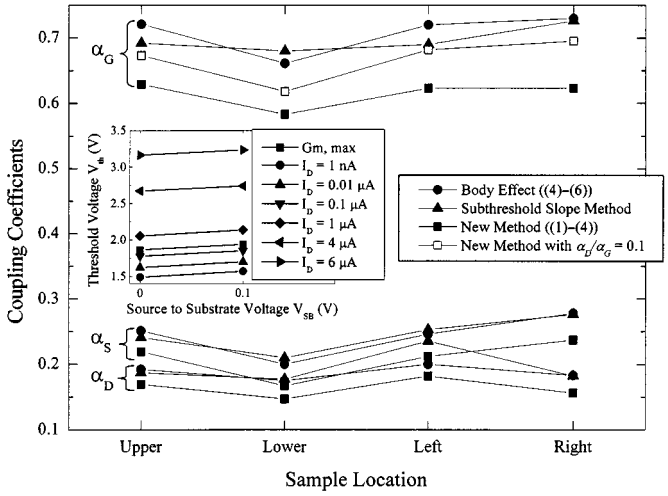

Fig. 2. Gate, drain, and source coupling coefficients extracted from various methods, plotted versus four different locations on the wafer. Involved voltage shifts are: ΔV_{CG1} ranges from 0.24 V to 0.25 V; ΔV_{CG2} from 0.24 V to 0.25 V; ΔV_{CG0} from −0.06 V to −0.05 V; ΔV_{FG1} from 0.19 V to 0.20 V; and ΔV_{FG2} from 0.19 V to 0.20 V. The inset of the figure shows the extracted V_{th} versus V_{SB} for the position "Left" by the maximum transconductance extrapolation and the constant current forcing.

which is defined the subthreshold swing ratio minus 0.6, ranges from 0.08 to 0.13, significantly exceeding that (≈0.03) arisen from bulk capacitance coupling [2]. Thus, there should exist the other origins.

We trace previous overestimation of α_Gs to process variations, as achieved by a subthreshold current model for source-to-substrate bias $V_{SB} = 0$ [7]: $I_D = I_o \exp(qV_{GB}/nkT)$, where I_o is the current factor, n is the slope factor, and $V_{GB} = V_G - V_B$. According to this model, we can have a set of current factor I_{of} and slope factor n_f to characterize a flash memory cell while due to process variations another set of I_{od} and n_d ought to be used for a "mirrored" or dummy transistor. For the first time, the subthreshold swing ratio in the subthreshold slope method is mathematically formulated: $S_d/S_f = \alpha_G(n_d/n_f)$, where S_d and S_f represent subthreshold swings in dummy transistors and flash memory cells, respectively. At least two new insights can be drawn here. Firstly, the subthreshold slope method is strikingly immune to I_o variation. Secondly, the condition of $n_d > n_f$ can satisfactorily interpret the large errors, as confirmed by the fitted n_d of around 2.0∼2.1 that is partly demonstrated in Fig. 1. Such abnormally high value of n_d, relative to the typical value of 1.7 in the same MOS process, suggests significant interface state produced when shorting the control gate to floating gate. More evidences of $n_d > n_f$ are given later.

III. New Method

Fortunately, the influence of interface state components in dummy transistors can be effectively eliminated via an expression that relates the slope factor n to threshold voltage V_{th} versus V_{SB} measurement [7]

$$n = 1 + \mathrm{d}V_{th}/\mathrm{d}V_{SB}. \tag{1}$$

Further, we limit V_{SB} to the range between 0 and 0.1 V, i.e., the case of weak body effect. Under this situation, the existing three-parameters subthreshold conduction current–voltage (I–V) model [7] can reduce to a two-parameters version: $I_D = I_o \exp[q(V_{GB} - nV_{SB})/nkT]$; that is, I_o and n are constants, regardless of V_{SB} between 0 and 0.1 V as verified in Fig. 1. The same condition also ensures use of a linear version of (1): $n = 1 + (V_{th2} - V_{th1})/0.1$ V, where V_{th1} and V_{th2} are threshold voltages measured at $V_{SB} = 0$ and 0.1 V, respectively. Two schemes for V_{th} extraction, namely, the maximum transconductance extrapolation and the constant current forcing, produce almost the same results as shown in the inset of Fig. 2. For example, both methods yield a mean of $n = 1.74$ for the position "Left" with a very small standard deviation of 0.05, which is in close proximity to 1.7 in the same MOS process.

Then incorporating the two-parameters subthreshold I–V model to a well known relationship $V_{FG} = \alpha_G V_{CG} + \alpha_D V_D + \alpha_S V_S + \alpha_B V_B + Q_{FG}/C_T$ [8], we derive out the following equation for the case of weak body effect in flash memory cells in terms of $V_S = \Delta V_S$ (=0.1 V)

$$n\Delta V_S = \alpha_G \Delta V_{CG1} + \alpha_S \Delta V_S \tag{2}$$

where ΔV_{CG1} is the control gate voltage shift as illustrated in Fig. 1 for $V_D = 0.15$ V. Similarly the bias configuration of $V_S = 0.15$ V and $V_D = \Delta V_D$ (= 0.1 V) expresses another control gate voltage shift (ΔV_{CG2}) as

$$n\Delta V_D = \alpha_G \Delta V_{CG2} + \alpha_D \Delta V_D. \tag{3}$$

Regarding drain coupling coefficient α_D, we measured a third control gate voltage shift (ΔV_{CG0}) under the same subthreshold current in flash memory cells at $V_S = 0$ for two V_Ds of 0.15 and 0.35 V. This readily leads to [1]

$$\alpha_G/\alpha_D = 0.2\ \mathrm{V}/|\Delta V_{CG0}|. \tag{4}$$

The source coupling coefficient α_S can be assessed in the similar way.

Substituting the measured voltage shifts into above equations, the capacitance coupling coefficients can be solved out as displayed in Fig. 2. Indeed, the corrected α_Gs in Fig. 2 show improved agreements and except for the position "Lower," the errors are substantially reduced down to that due to bulk capacitance coupling only. In Fig. 2, the new method yields α_D/α_G of around 0.27. If this ratio is intentionally reduced to 0.1 such as to reflect the situation quoted in [2], the resultant error for position "Lower" again can be described by bulk capacitance coupling.

Finally, we present more evidences. Firstly, the I–V in dummy devices measured under $V_S = \Delta V_S$ (=0.1 V) and $V_D = 0.15$ V is together plotted in Fig. 1. For the same subthreshold current, the corresponding floating gate voltage shift (ΔV_{FG1}) traditionally could be related to the control gate voltage shift (ΔV_{CG1}) by

$$\Delta V_{FG1} = \alpha_G \Delta V_{CG1} + \alpha_S \Delta V_S. \tag{5}$$

The bias configuration of $V_S = 0.15$ V and $V_D = \Delta V_D$ (=0.1 V) deals with another floating gate voltage shift (ΔV_{FG2}) in dummy transistors

$$\Delta V_{FG2} = \alpha_G \Delta V_{CG2} + \alpha_D \Delta V_D. \quad (6)$$

The resulting α_Gs as shown in Fig. 2 are found to be comparable with those from the subthreshold slope method, revealing that i) they have the common origins of $n_d > n_f$ and ii) to meet equal subthreshold current between flash and dummy devices, current mismatch inevitably introduces significant errors in floating gate potential shifts such as ΔV_{FG1} in Fig. 1. Secondly, all the αs of the new method in Fig. 2 sum up to an amount of very close to unity, indicating that the bulk coupling coefficient α_B is considerably very small, consistent with the error of 0.03 due to bulk capacitance coupling [2].

IV. Conclusion

The subthreshold slope method has practically experienced overestimation of α_Gs in flash memory cells. Process variations as the primary origin of the errors have been judged by means of a two-parameters subthreshold current model. A new method incorporating weak body effect has been developed. The errors have been substantially improved down to that constituted by bulk capacitance coupling itself.

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