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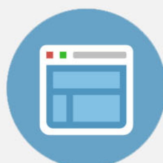
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Silicon nanostructures fabricated by scanning probe oxidation and tetra-methyl ammonium hydroxide etching

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Fabrication of silicon nanostructures is a key technique for the development of monolithically integrated optoelectronic circuits. We demonstrated that the process of scanning probe microscope (SPM) oxidation and anisotropic tetra-methyl ammonium hydroxide (TMAH) etching is a low-cost and reliable method to produce smooth and uniform silicon nanostructures on a variety of silicon substrates. Etched structures with a pitch of 100 nm, positive- and negative-contrast structures, and features height greater than 100 nm have been produced on bare silicon, and Si_3N_4-coated and silicon-on-insulator wafers. Evolution of hexagonal pits on two-dimensional grid structures were shown to depend on the pattern spacing and orientation with respect to Si(110) crystal directions. We successfully combined SPM oxidation with traditional optical lithography in a mixed, multilevel patterning method for realizing micrometer-and nanometer-scale feature sizes, as required for photonic device designs. The combination of SPM oxidation and TMAH etching is a promising approach to rapid prototyping of functional nano-photonic devices. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1476072]

I. INTRODUCTION

Silicon-based structures have attracted considerable attention because of increasing demands for monolithically integrated optoelectronic systems.[1] These systems are important since they offer significant advantages in terms of compactness, functional enhancement, and cost reduction. Nanometer-scale structured features are required for specific purposes, such as photonic crystals[2,3] and subwavelength structures.[4–6] A low-cost, yet high-flexibility approach to fabricate the Si nanostructures is desirable for exploratory studies of nano-photonic devices at infrared and visible regions. Scanning probe microscope (SPM) oxidation is regarded as a direct-writing and resistless lithography,[7] where a conductive proximal probe is used to provide a local intense electric field near the sample to modify the sample surface (i.e., local anodic oxidation). It has been demonstrated as a promising method to perform nanometer-scale lithography and widely applied to pattern semiconductors, metals,[8–10] and insulators.[11] The growth kinetics,[12,13] reaction model,[14,15] and property of scanning-probe-induced oxide[16,17] have been extensively studied recently. The sub-50-nm linewidth of SPM oxidation demonstrates its potential to nanotechnology.[18,19] In practice, SPM oxidation is conducted with an ambient atomic force microscope (AFM). Because of its inherent simplicity, generality, positioning precision, and low cost, this method is regarded as a key technique for rapid prototyping of nanometer scale devices. For example, SPM oxidation is considered to be useful for the development of multipassband integrated optical filters, which require placement precision and feature sizes that are finer than for periodic gratings.[20]

The material contrast between scanning-probe-induced oxides and silicon substrates can be employed to selective wet and dry etching with the oxide pattern as a mask.[7,21] Positive-contrast, high-aspect-ratio nanostructures (e.g., ridges) with vertical sidewalls were produced by KOH etching, as reported by some of us recently.[22] We also reported SPM oxidation of silicon nitride thin film as a mask to produce negative-contrast nanostructures (e.g., trenches).[23] Furthermore, the scanning-probe-induced oxide also can be a mask for selective plasma nitridation of silicon to reverse the pattern, and negative-contrast structures are made by a subsequent KOH etching.[24] Due to mobile ion (K^+) contamination, however, KOH is not favorable to the integrated circuit (IC) process. In addition, the aggressive etching property of KOH leads to noticeable roughness on the surface and sidewalls. Cohn *et al.*[20] have proposed an alternative to KOH etching through the combination of SPM oxidation and tetra-methyl ammonium hydroxide (TMAH) etching (SPM oxidation+TMAH etching). Tabata *et al.*[25] demonstrated anisotropic etching of silicon by TMAH solution, which has the advantage of smoothness, selectivity, nontoxicity, and IC compatibility. Its boiling point is 102 °C and it does not decompose below 130 °C. Therefore TMAH is very stable under a normal etching process. At concentrations above 22 wt %, a very smooth surface can be obtained. The etch rate in

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TMAH is not as high as that in KOH. However, for example, the etch rate of Si(100) in a 22 wt % TMAH solution at 80 °C is 0.5 μm/min, enough for practical usage. Furthermore, TMAH hardly attacks silicon oxide and silicon nitride mask layers. The etch rate of silicon oxide is 0.1 nm/min, corresponding to a selectivity of 5×10^3. Since no etching is observed for silicon nitride films deposited by low-pressure chemical vapor deposition (LPCVD), the selectivity of Si/Si_3N_4 is even higher than that of Si/SiO_2. A mixture of TMAH and isopropyl alcohol (IPA) solutions will reduce the etch rate, but it further improves the smoothness of the sidewalls.[26] Because smoothness is our major concern, we chose the mixture of TMAH and IPA solutions to fabricate silicon nanostructures in our study.

In this article we present results which demonstrate the fine control possible with SPM oxidation+TMAH etching. First, we present scanning electron microscopy (SEM) micrographs of fine and uniform silicon ridges on a Si(110) substrate. To explore prospective applications of this approach, we studied the variety of structures produced on (100)- versus (110)-oriented silicon substrates. The evolution of hexagonal pits and the dependence of the hexagonal pits on the size and pattern orientation on Si(110) wafers were studied. The terminal geometry of silicon nanostructures produced by this process is shown to be strongly dependent on the geometric relationship between the oxide pattern and slow-etched {111} planes. We also produced positive- and negative-contrast nanostructures with vertical sidewalls on a Si(100) wafer and isolated structures on (100)-oriented silicon-on-insulator (SOI) substrates. Finally, we combined SPM oxidation with optical lithography, which we deem necessary for practical applications. In this combined approach both micrometer- and nanometer-scale features were produced. An example of a multilayer structure is shown. From the various silicon nanostructures produced by this process and the compatibility with optical lithography, we conclude that SPM oxidation+TMAH etching is a convincing approach to fabricate Si nanostructures.

II. EXPERIMENT

The silicon wafers used to fabricate various structures were bare (110) wafers, bare (100) wafers, Si_3N_4-coated (100) wafers, and (100)-oriented SOI wafers. Conductivity of these substrates ranged from less than 1 to over 20 Ω cm. Silicon substrate samples were cleaved along the {111} planes to produce a parallelogram in the case of a (110)-oriented wafer and along the {110} planes to produce a rectangle in the case of a (100)-oriented wafer. The SOI wafer consisted of a 100-nm silicon top layer over a 200-nm buried oxide layer. Bare silicon and SOI wafers were dipped in 2% HF solution for 30 s and rinsed with deionized (DI) water to remove native oxide. The Si_3N_4 thin-film samples were prepared by LPCVD on (100) wafers and further densified by rapid thermal annealing to obtain a film thickness of approximately 4 nm. Prior to SPM oxidation, the Si_3N_4 substrate was dipped in 1% HF solution for 120 s to thin the film.

SPM oxidation was performed using a commercial AFM,[27] which has a tripod piezoelectric scanner with integrated strain gauges for closed-loop control in each scan axis to monitor and feedback the scanner motion. The linearity error was estimated to be less than 2% over a span of 80 μm. Commercial highly doped-silicon contact mode AFM cantilevers coated with conductive tungsten carbide were used.[28] Their typical force constant and resonance frequency was 0.95 N/m and 105 kHz, respectively. For SPM oxidation, a bias of 9–12 V was applied to the sample depending on the condition of a particular cantilever at a writing speed of approximately 2 μm/s. After patterning, the substrates were etched in a 25 wt % TMAH solution and rinsed in DI water. Typically isopropyl alcohol (IPA) was added to achieve a solution of 83 ml TMAH+17 ml IPA (TMAH+IPA solution). According to our data, the etch rate of a TMAH+IPA solution was about 45% of a TMAH solution for {110} planes and 70% of a TMAH solution for {100} planes.

III. RESULTS AND DISCUSSIONS

A. Structures on Si(110)

A Si(110) sample was mounted with one of its cleaved {111} edges oriented along the *Y* scan direction of the AFM scanner, Fig. 1(a). A series of parallel oxide lines was produced along the *Y* scan direction. The pitch of these lines varied from 100 to 500 to 200 nm with lengths of 3, 5, and 10 μm, respectively, from left to right in Fig. 1(b). The sample was etched in a 60 °C TMAH+IPA solution for 40 s, resulting in a height of the silicon ridges on the order of 100 nm and a width of about 40 nm, Figs. 1(c) and 1(d). The silicon ridges possess very homogeneous surfaces because of the smoothness of the TMAH etching, resulting in estimated sidewall roughness below 5 nm. Not only the ridge width, but also the spacing between ridges has been remarkably improved to sub 100 nm from 250 nm.[22] We have never achieved such fine and uniform ridges by KOH etching before. For nanomachining, fineness, precision, and smoothness are important criteria, so TMAH is obviously a better etching solution to fabricate silicon nanostructures than KOH.

Anisotropic wet etching also can make a two-dimensional (2D) hexagonal pit array by patterning a 2D oxide grid.[22] It is essential to know how these hexagonal pits evolve, i.e., how the terminal geometry depends on the size and orientation of the initial oxide grid for practical control of feature dimensions. 2D oxide grid patterns oriented to the *X* and *Y* scan directions were prepared, as shown in Fig. 2(a). The pitch of the resulting features is 500 nm in both the *X* and *Y* directions. The samples were then etched in a 60 °C TMAH+IPA solution for 15, 40, and 80 s, Figs. 2(b)–2(d), respectively, and in a 70 °C TMAH solution alone for 70 s, Fig. 2(e). This result illustrates how hexagonal pits evolve from a square grid with increasing etched depths. The mean etching rate of Si(110) in a TMAH+IPA solution at 60 °C is 3.2 nm/s. For 15 s etching, the depth is 40 nm and the anisotropy begins to develop along the diagonal [Fig. 2(b)]. For 40 s etching, the depth is 130 nm, and the {111} planes appear and underetching occurred under the horizontal oxide lines [Fig. 2(c)]. So far, the hexagon is not shaped yet, and the bottom is a rectangle. For 80 s etching, the depth reaches

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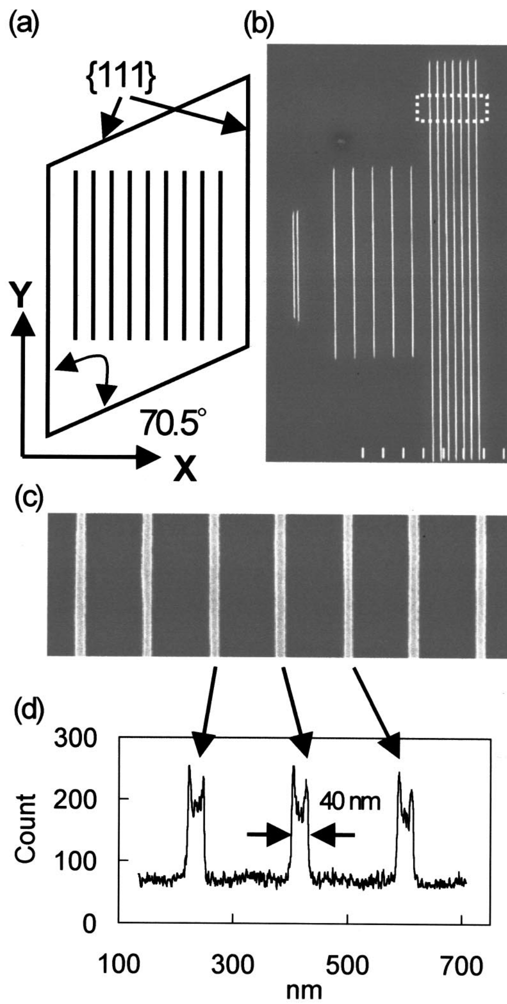

FIG. 1. (a) Alignment of a Si(110) sample and 1D oxide pattern with respect to the coordinate of the AFM scanner, (b) SEM image of 1D Si ridges of 100, 500, and 200 nm pitches (from left to right) etched in a 60 °C TMAH+IPA solution, (c) and (d) close-up SEM image and its cross-section profile of the marked area in (b).

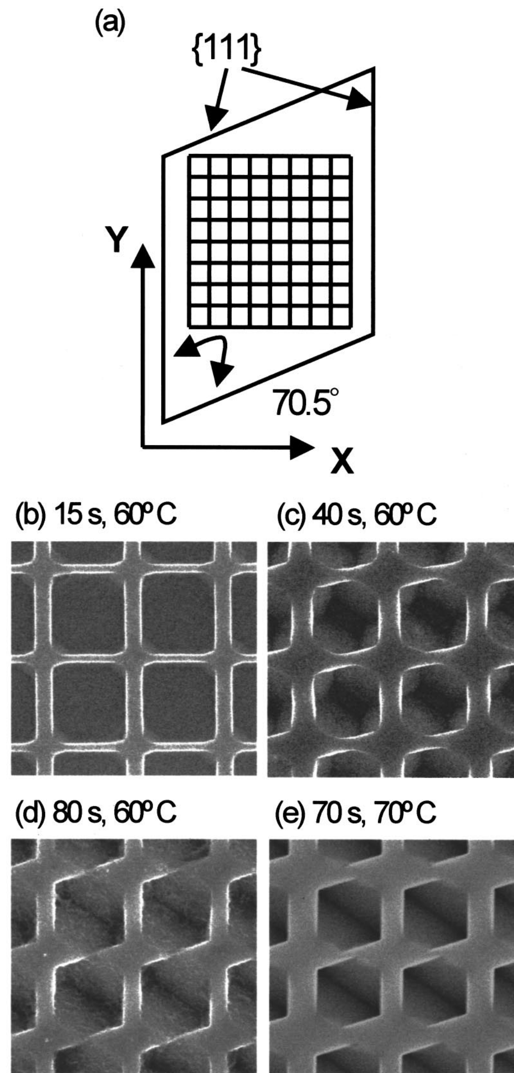

FIG. 2. (a) Alignment of a Si(110) sample and 2D oxide pattern of a 500 nm pitch, (b)–(e) SEM images of 2D silicon structures etched in a 60 °C TMAH+IPA solution [except (e) in a 70 °C TMAH solution], marked with individual etching time and temperature. The sample in (d) was contaminated during the chemical process.

260 nm, and the hexagonal pit surrounded by four vertical and two slanted {111} planes is nearly completed [Fig. 2(d)]. After further etching, the hexagonal pit is completed and the etching is terminated by six {111} planes [Fig. 2(e)], although the overall etch depth is 760 nm outside of the grid pattern.

Figures 3(a)–3(f) show etched 2D grid structures of various pitches prepared by TMAH+IPA solution. The pit structures of $0.25\times0.5\ \mu\text{m}^2$ grid shown in Figs. 3(a) and 3(b) were etched for 15 and 50 s, respectively. The elongated hexagonal pits developed well, as the elongated direction was oriented along the vertical {111} planes so that the etch front was confined laterally as it progressed along the Y direction. The $1\times0.25\ \mu\text{m}^2$ grid structures appearing in Figs. 3(c) and 3(d) were etched for 15 and 40 s, respectively. In this case, the elongated direction is far apart from the {111} planes so that etching is less preferential. Hexagonal pits do not readily develop even though the dimensions are double those of the previous case. The $1\times1\ \mu\text{m}^2$ and $2\times2\ \mu\text{m}^2$ grid structures shown in Figs. 3(e) and 3(f) were etched for 50 and 40 s. The oxide pattern of $2\times2\ \mu\text{m}^2$ was reinforced by patterning double parallel oxide lines. Since the opening is larger than $1\times1\ \mu\text{m}^2$, it is not possible to develop hexagonal pits.

If the 2D pattern is rotated counterclockwise by 35°, Fig. 4(a), oxide gridlines are no longer oriented along the vertical and slanted {111} planes. The sample, etched in a 70 °C TMAH solution for 40 s, shows evidence of underetching below the oxide lines. Oxide lines appear shaped in a zigzag pattern, Fig. 4(b), and the hexagon is severely distorted. For the extreme case, if the 2D pattern is rotated counterclockwise by 55°, Fig. 4(c), the leftward oxide lines are now oriented along the slanted {111} planes, which have an angle of 35.27° with respect to the (110) surface. The rightward lines bisect the 70.5° angle between vertical {111} planes. In this case, the etch front is completely guided by the leftward lines capping the slanted {111} planes, whereas rightward lines have no etch resistance to the etch front and are completely removed. Consequently a 1D sawtooth structure bounded by slanted {111} planes as shown in Fig. 4(d) is produced. Apparently, anisotropic wet etching is strongly affected by the

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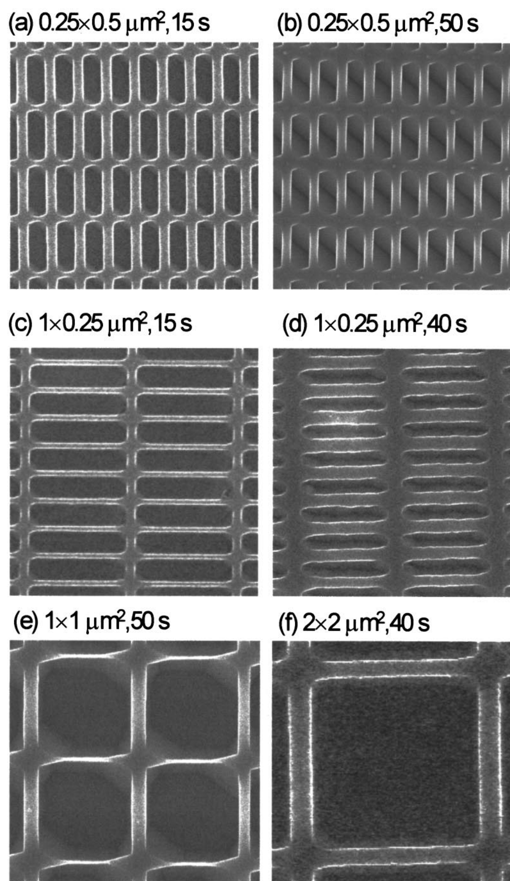

FIG. 3. 2D silicon structures of various pitches on Si(110) samples etched in a 60 °C TMAH+IPA solution, marked with individual grid size and etching time.

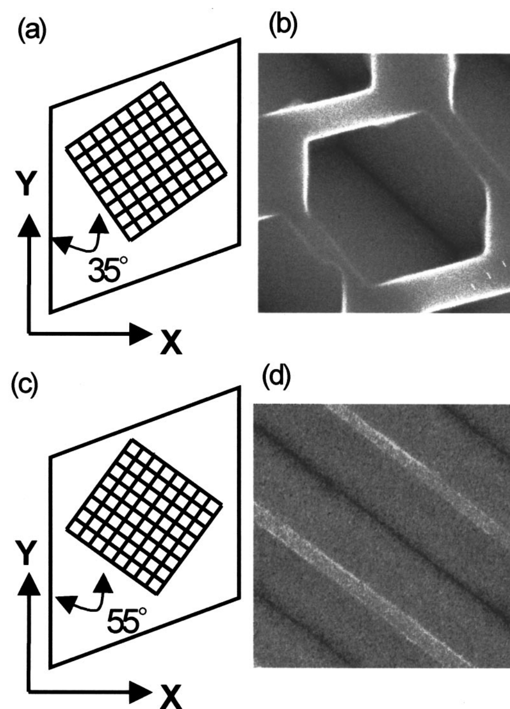

FIG. 4. (a) 2D oxide pattern of 35° misalignment on a Si(110) sample, (b) 500-nm-pitch distorted hexagonal silicon structure with the mask in (a),(c) 2D oxide grid mask of 55° misalignment, (d) 1-μm-pitch sawtooth silicon structure with the mask in (c). Both were etched in a 70 °C TMAH solution.

orientation of the oxide pattern with respect to the {111} planes.

Etching anisotropy at the nanometer scale is different from its conventional behavior at larger scales. The nanometer-scale oxide pattern imposes an ''initial condition'' on the etch front. The etch front is preferential in the direction where the oxide pattern and {111} planes are less correlated. Hence the etching is a diffusion-limited reaction within the local nanometer-scale region of a grid opening and the terminal geometry is influenced by the relative stability of the oxide pattern and {111} planes. Formation of the elongated hexagonal pits and 1D sawtooth structures can be attributed to such reaction conditions.

B. Structures on Si(100)

On Si(100) substrates, structures bounded by slanted {111} sidewalls are commonly produced at an angle of 54.73° to the surface. The pyramid structure is one of the most familiar examples of anisotropic etching at Si(100). However, the geometry bounded by {111} planes imposes many limitations in our efforts to achieve specific 3D structures due to the fixed intersection angle of {100} and {111} planes. For photonic devices, however, vertical sidewalls are preferable since low-light scattering and high spatial density of grating structures are factors that can strongly influence performance.

Vertical sidewalls can be produced on Si(100) by KOH etching if the oxide grid pattern is aligned with the ⟨100⟩ direction, i.e., at a 45° angle to the primary $(01\bar{1})$ wafer flat.[29] In this case, sidewalls consist of {100} planes, perpendicular to the surface. The sidewalls and bottom surfaces are all {100} planes and etch rates are almost equal. The effect of KOH and TMAH concentration on sidewalls, with and without IPA, has been studied.[30,31] Vertical sidewalls tend to be produced by high-concentration KOH and TMAH solutions. Here, we investigate this approach in conjunction with SPM oxidation to produce vertical nanostructures on Si(100) substrates.

1D and 2D oxide patterns with a pitch of 700 nm were prepared on Si(100) substrates at a 45° angle to the primary $(01\bar{1})$ flat, Fig. 5(a). The sample was etched in a 60 °C TMAH solution for 40 s to produce positive-contrast structures. Shown in Fig. 5(b) is a ridge structure with a 1D grating pattern. The well-defined silicon ridges appear bounded by vertical {100} planes and the right-angle corners at both ends are bounded by slanted {111} planes. Widths of these ridges are about 240 nm according to SEM images and the well depth was determined to be about 120 nm as measured by AFM. As the pattern is a 2D grid, the etched structure is an array of octagonal pits, bounded by {110} and {111} planes, Fig. 5(c). It is similar to the previous result made by KOH+IPA solution.[30] The pits could be selectively changed with respect to the {100} and {111} planes as the etchant temperature is raised.

Conversely, negative-contrast structures can be made using a mask of silicon nitride thin film patterned by SPM oxidation. Oxide patterns oriented at 45° were made on the

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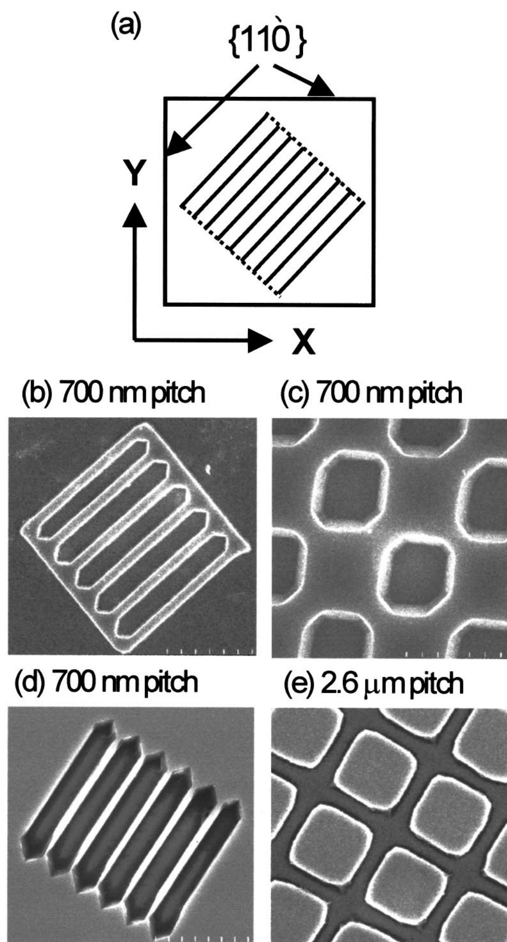

FIG. 5. (a) Oxide pattern of 45° misalignment on a Si(100) sample, only the 1D pattern is shown here. The dashed lines are additional oxide lines only for the case in (b) to protect the 1D positive structure against the etching at the ends. (b) and (c) 1D and 2D positive-contrast structures with the masks of oxide pattern, (d) and (e) 1D and 2D negative-contrast structures with Si_3N_4 thin film masks patterned by SPM oxidation. All were etched in a TMAH solution.

nitride film and removed by HF dipping to expose the underlying silicon substrate. Subsequently, the sample was etched in a 60 °C TMAH solution for 120 s. Figure 5(d) shows 1D trenches with a pitch of 700 nm. The widths of trenches are about 550 nm as estimated from SEM images and depth was found to be about 280 nm as measured by AFM. As a counterpart of the 1D ridge structure, the 1D trench structure has the identical geometry of Fig. 5(b) since they both are formed by {100} and {111} planes. Due to the longer etching time, vertical walls are reduced to a width of about 150 nm. It is possible to achieve a 1D grating pitch smaller than 700 nm by appropriately adjusting the oxide linewidth, grating pitch, and etching time. Figure 5(e) is an SEM image of a 2D grid of vertical trenches with a pitch of 2.6 μm. Square mesas are bounded by four vertical {100} planes. The trench widths are about 550 nm as well. Instead of being a right angle, the corners were attacked on two sides and became somewhat rounded. The patterned silicon nitride film appears to be a perfect mask for TMAH etching. Apparently, the method of 45° mask alignment to produce vertical structures on Si(100) substrates can be implemented by the process of SPM oxidation+TMAH etching and is applicable to nanometer scale for both positive and negative contrast.

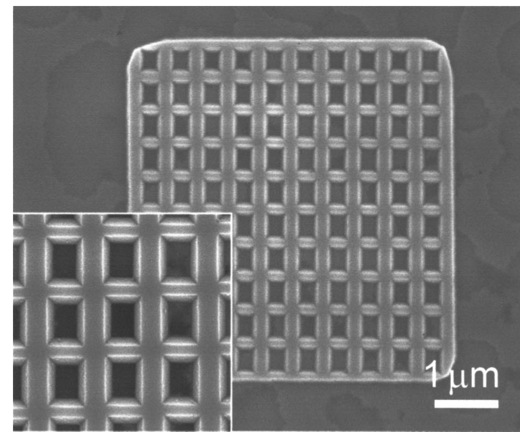

FIG. 6. SEM image of a truncated inverted pyramid structure with a pitch of 500 nm on a (100)-oriented SOI sample. The inset is a close-up image of the structure.

C. Structures on (100)-oriented SOI

SOI wafers are suitable for planar and channel waveguides and allow the incorporation of silicon microelectronics with integrated optics into an optoelectronic system. We have extended the SPM oxidation+TMAH etching to SOI subtracts. 2D oxide grid patterns with a pitch of 500 nm were produced parallel to the primary flat. The 100 nm silicon top layer of the SOI substrate was etched in a 60 °C TMAH+IPA solution for 50 s. The etched silicon structure is a truncated, inverted pyramid bounded by four {111} planes, Fig. 6. AFM measurements show that the height of the structure is 100 nm, indicating that the buried oxide layer acts as an etch stop. The isolated silicon structure with high uniformity and homogeneity was prepared as shown in the inset. Note the presence of random islands on the exposed SiO_2, which AFM indicates to be approximately 6 nm in height from incomplete etching of the silicon top layer. Electric force microscopy confirms that the islands are residual silicon, and efforts are underway to prepare controlled geometry, free-standing 1D silicon wires, and 2D structures without such residual silicon islands.

D. Combination of optical lithography and SPM oxidation

In practice, SPM oxidation is not suitable for patterning large features, since writing speed is limited by the inherent low throughput of single-probe lithography and the high-scan-speed stability of typical probe-based instrumentation. Since photonic device structures require both coarse and fine patterning, an alternative approach for prototyping such devices is to combine optical lithography and SPM oxidation, where the optical lithography defines micrometer-sized coarse structures and the SPM oxidation defines only sub-100-nm fine structures.

Here we present a preliminary demonstration of mixed, multilevel patterning, Fig. 7. A 20-nm thick, thermal oxide was grown on a Si(110) wafer. Micrometer-sized mesa struc-

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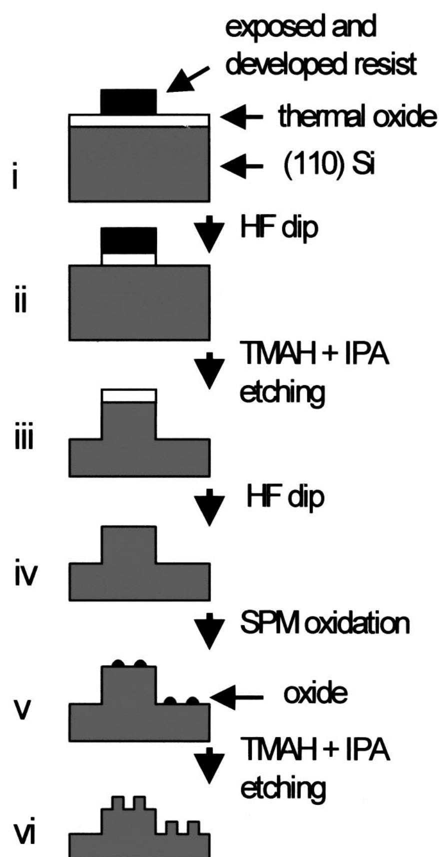

FIG. 7. Schematic flowchart of the combination of optical lithography and SPM oxidation.

tures were defined by optical lithography (step i) and transferred to the thermal oxide by HF etching (step ii) and the resist was removed. The patterned SiO_2 was used as a mask for silicon etching in a TMAH+IPA solution for 80 s (step iii), after which the oxide was removed by an HF etch (step iv). Next, patterns were produced by SPM oxidation on top of the silicon mesa as well as on the lower silicon surface (step V). After a second TMAH etch (step vi), this time for 40 s, fine structures were produced, Fig. 8. The height of the silicon mesa, defined by the first TMAH etch, was determined to be about 240 nm by AFM measurement and the height of the 1D grating structures, defined by the second TMAH etch step, were found to be about 130 nm. A close-up image of the fine grating structure next to the mesa shown in the inset presents the positioning capability of SPM oxidation during multilevel patterning. Functional photonic devices can be made with such a combined process. For example, to make a waveguide grating, optical lithography can be employed to define the waveguide structure and SPM oxidation to define the grating structure.

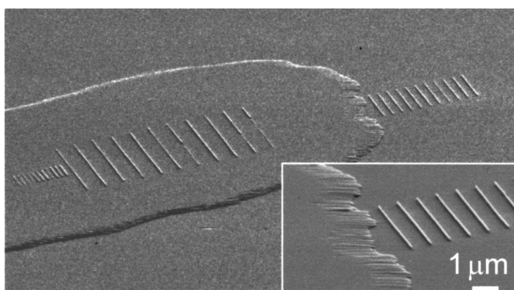

FIG. 8. Tilted-angle SEM image of the coarse mesa and fine 1D grating structures made by the combined lithographic technique, where the grating pitches are 0.5, 2, and 1 μm from left to right, respectively. The inset is a close-up image of the 1 μm grating structure next to the mesa.

IV. CONCLUSIONS

The process of SPM oxidation+TMAH etching has been applied to produce a variety of silicon nanostructures. Anisotropic etching of silicon by TMAH is shown to be suitable to reliably fabricate smooth, uniform, and delicate nanostructures. The evolution of hexagonal pits produced on Si(110) substrates and its dependence on the size and pattern orientation has been studied in some detail. At the nanometer scale, anisotropic etching is a diffusion-limited reaction, so the anisotropy is affected by the local orientation of the oxide or nitride etch mask with respect to the slow-etched {111} planes. This process is successfully applied to Si_3N_4-coated Si wafers and to SOI wafers. The method of 45° mask alignment to produce vertical sidewalls on Si(100) can be achieved at the 100-nm scale with both positive and negative contrast. Finally, a combined technique of optical lithography and SPM oxidation has been proposed, and we have shown it to be a promising approach for prototyping nanophotonic devices.

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