# Fully Process-Compatible Layout Design on Bond Pad to Improve Wire Bond Reliability in CMOS ICs

Ming-Dou Ker, *Senior Member, IEEE,* and Jeng-Jie Peng, *Member, IEEE*

***Abstract*—During manufacture of wire bonding in packaged IC products, the breaking of bond wires and the peeling of bond pads occur frequently. The result is open-circuit failure in IC products. There were several prior methods reported to overcome these problems by using additional process flows or special materials. In this paper, a layout method is proposed to improve the bond wire reliability in general CMOS processes. By changing the layout patterns of bond pads, the reliability of bond wires on bond pads can be improved. A set of different layout patterns of bond pads has been drawn and fabricated in a 0.6-$\mu$m single-poly triple-metal CMOS process for investigation by the bond wire reliability tests, the ball shear test and the wire pull test. By implementing effective layout patterns on bond pads in packaged IC products, not only the bond wire reliability can be improved, but also the bond pad capacitance can be reduced for high frequency application. The proposed layout method for bond pad design is fully process-compatible to general CMOS processes.**

***Index Terms*—Ball shear test, bond pad, bond wire, layout, reliability, TAB, wire pull test.**

## I. INTRODUCTION

FOR integrated circuits (IC) products, three conventional technologies of connection between bond pads and package leads are known as wire bond, tape automated bond (TAB), and flip chip bond. For low cost consideration, wire bond method has been widely used in IC products. Although considerable improvements on wire bond have taken place over years, some bond wire related failures still constitute a reliability risk. In wire bond IC products, bond pad peeling and bond wire breaking have been recognized as two dominant weaknesses on bonding reliability. There have been several methods proposed to overcome these problems. One of the proposed methods is to use special materials for replacement of the original material of on-chip bond pads before the wire-bonding step of IC fabricating process. Materials which have ever been substituted on the bond pad are oxide [1], metal [1], inter-layer material [2], dielectric layer [3], [4], and the top surface material of the bond pad [5]. This modified bond pad was found to give either improved bond pad cracking prevention due to bond-process-induced stresses or adhesion of the bond wire on the bond pad. A second proposal is to use different device structures to improve the bond wire stiffness. The structural reinforcement of inter-metal dielectrics shown in Fig. 1 was developed by Texas Instruments to eliminate

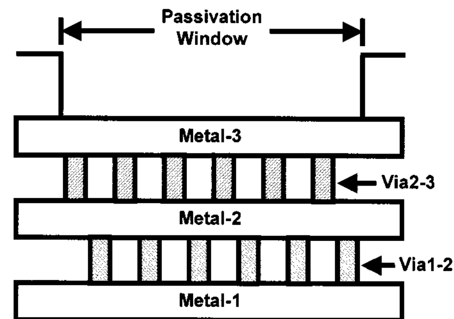

Fig. 1. Sea-of-vias bond-pad layer structure: two via array levels under the bonding metal for elimination of bond-pad damage through structural reinforcement of intermetal dielectrics [6].

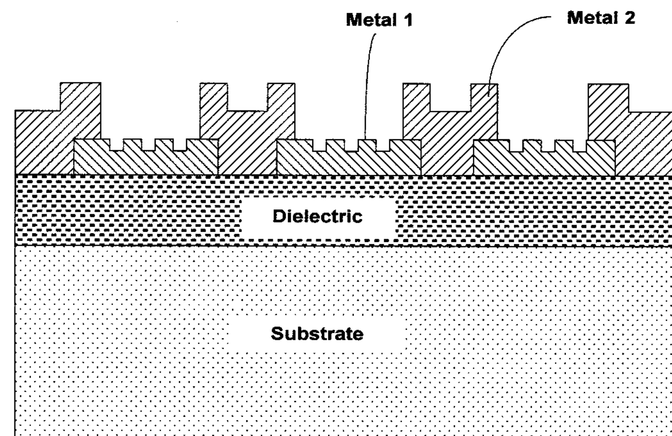

Fig. 2. Example of multimetal layer notched structure on the bond pad to increase the adhesion of the bond pad [7].

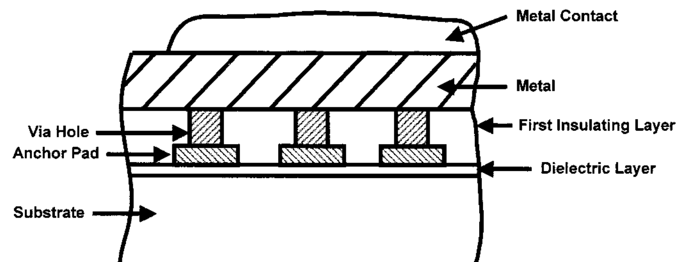

Fig. 3. Paling dielectric layer is used to reduce the stress of pad bonding and to rise up the bonding yield [8]–[10].

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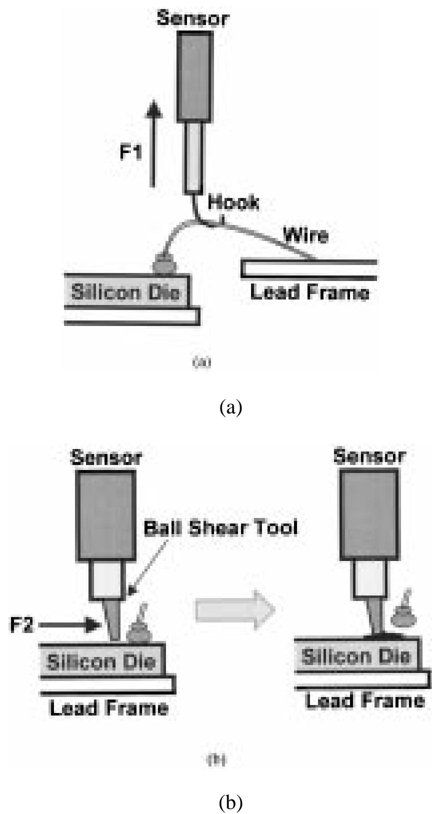
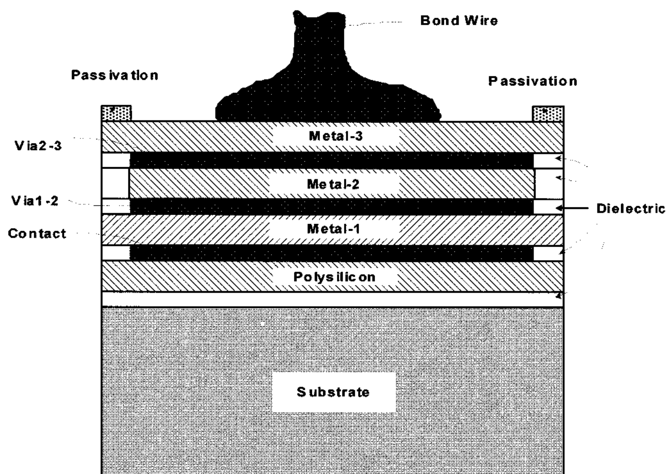



(a)




(b)

Fig. 4. Two general test methods on bond wires for qualifying the reliability of bond wires [14]: (a) wire pull test and (b) ball shear test.

Fig. 5. Conventional bond pad structure with the layout pattern of each metal layer is realized by one flat plate and the electrical connection between two metal layers is only a large area of via plug.

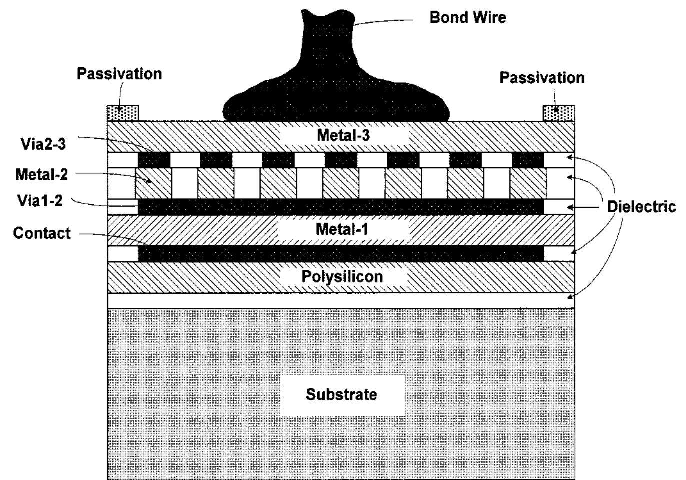



Fig. 6. Cross-sectional view of the proposed layout design method realized in a single-poly triple-metal CMOS process.

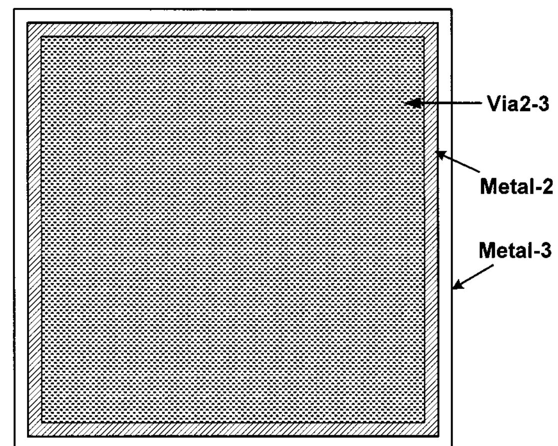



Fig. 7. Conventional layout patterns of Metal-2, Via2-3, and Metal-3 layers on a bond pad. The layout pattern of each metal layer is realized by one flat plate and the electrical connection between two metal layers is only one large via plug.

bond pad damage [6]. A multimetal layer notched surface, as shown in Fig. 2, was presented by Micron Technology to increase the adhesion of the bond pad [7]. The pad structure with multimetal layers on the dielectric layer is designed to form a paling surface for improving the stiffness of bond wires. An also paling dielectric layer used to reduce the stress of pad bonding, as shown in Fig. 3, has been reported by Motorola, Taiwan Semiconductor Manufacturing Company (TSMC) and United Microelectronics Corporation (UMC) [8]–[10] to improve bonding yield. A third approach, control of bonding stress, is also effective for the reliability issue of bond pads [11], [12]. To get a better bonding reliability, a fourth method of a wider bond pitch has been used [13]. However, a wider bond pitch often increases the chip sizes of IC products. Although the above four methods can improve the bond wire reliability, some extra modifications on conventional bond pad should be done for them. In summary, one modification is change of IC process flow or materials of bond pad to implement special structures for enhancement of bond pad stiffness. Another modification is to control the bonding force, or to increase the layout area for bond pads. All of these prior methods indicate the raise of product cost and fabrication time.

There are two test standards to qualify the bond pad reliability [14]. One is the wire pull test via a hook pulling the bond wire, as shown in Fig. 4(a). The hook is inserted under the bond wire while a pulling force is applied approximately at the center of the bond wire by the hook. The pulling force applied on the bond wire is vertical to the silicon die with a force sensor at

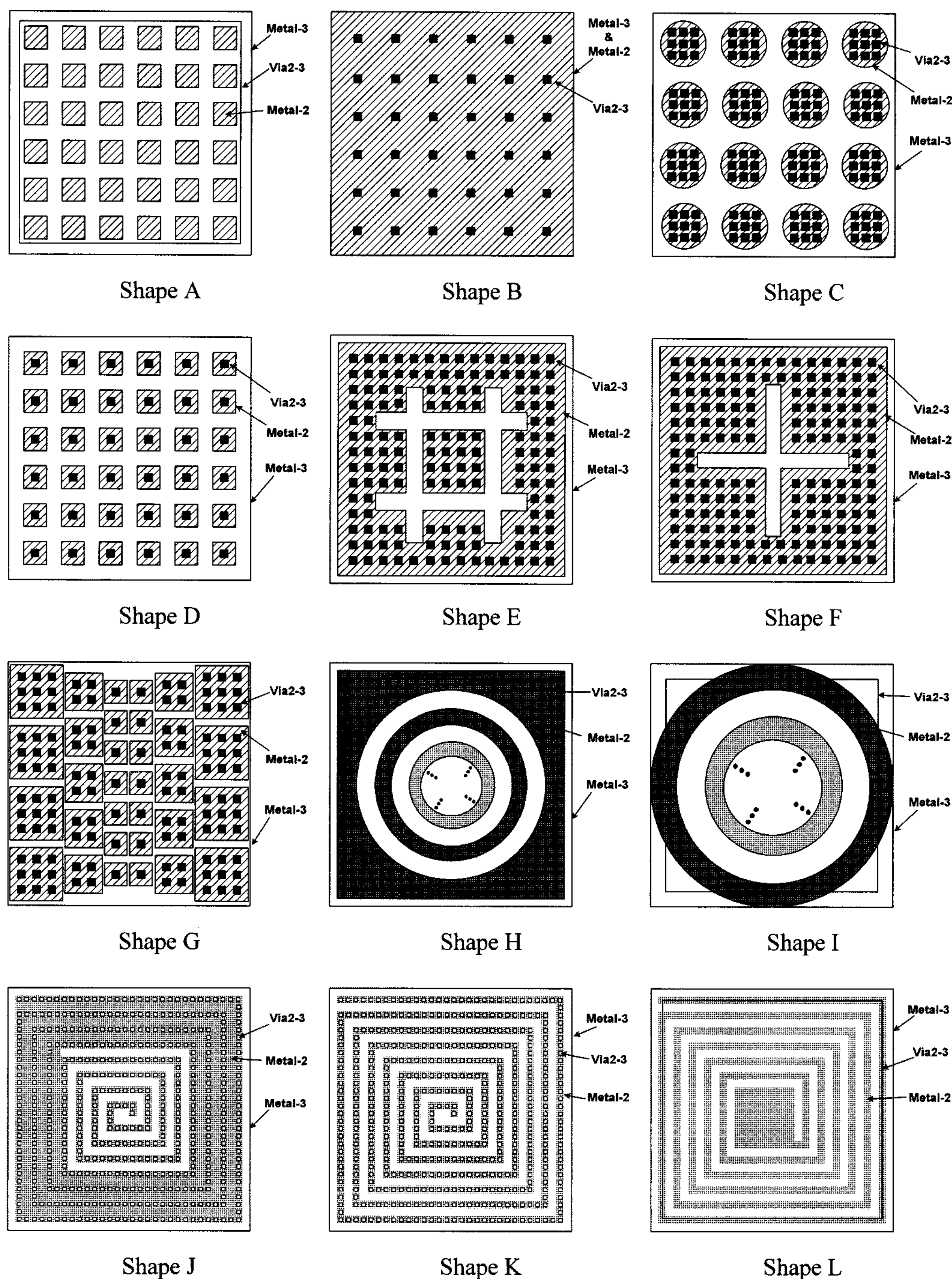



Fig. 8. Designed layout patterns of Metal-2, Via2-3, and Metal-3 layers are defined as the shape names at the bottoms of these layout patterns for the experimental test chips.

the top of the hook. When the applied force on the bond wire is increased continuously, the wire-pull force to break the bond wire can be measured from the force sensor. The other test, as shown in Fig. 4(b), is the ball shear test with a horizontal force in parallel with the die surface to push the silicon die. A tool is brought in contact with the die at a point just above the substrate. A force is then applied perpendicularly to one edge of the die and parallel to the substrate to cause bond failure by shear. When a failure occurs, the applied force at the moment of failure is detected by the sensor on the top of the ball shear tool. The applied force at failure is known as the ball shear force sustaining ability of the bond ball. According to these test methods of bond wire reliability, bond wires and bond balls on the bond pads are expected to sustain at least 5 g of pull-off force and 30 g of ball-shear force, respectively [14].

This paper presents an on-chip layout design method on bond pad to improve the bond wire reliability without extra process steps or material replacements in general CMOS processes, i.e., without any extra fabrication cost. By changing layout patterns of metal layer beneath the top metal of bond pads, bonding reliability of IC products can be effectively improved in general CMOS technologies [15].

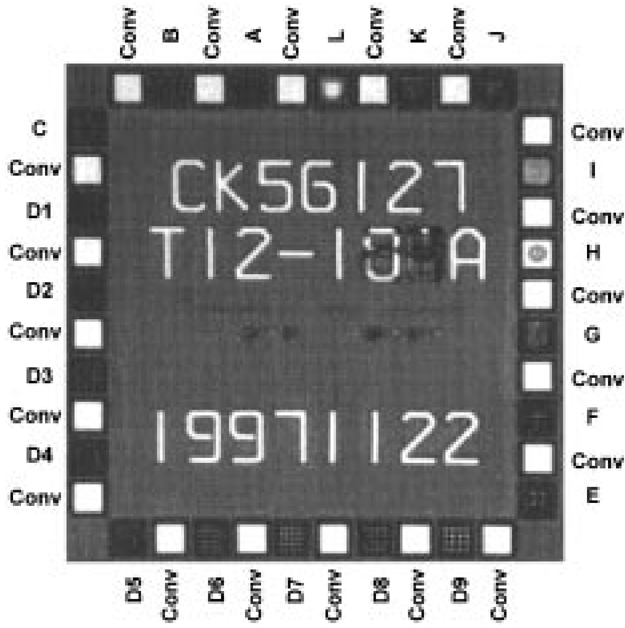



Fig. 9. Photograph of the test chip fabricated in a 0.6-$\mu$m CMOS process with three metal layers. The denoted "Conv" pads are bond pads realized by the conventional layout shape, and the other pads are realized by experimental layout patterns with different shapes of Fig. 8. Shapes D1–D9 are all similar to shape D of Fig. 8, but with varied layout spacing.

## II. Layout Design for Increasing Bond Wire Reliability

Cross-sectional views of the conventional bond pad structure and the proposed new layout design in a 0.6-$\mu$m single-poly triple-metal CMOS process are shown in Figs. 5 and 6, respectively. In the conventional pad structure, the layout pattern of each metal layer is one large square area of flat plate (96 $\mu$m $\times$ 96 $\mu$m) and the electrical connection between each two metal layers is performed by only one large size via plug. This bond pad structure is generally fabricated to be a flat plate on its top surface, which the adhesion of the bond ball with the bond pad is not good enough and bonding reliability is then lowered. In order to increase the adhesion of the bond ball on the bond pad, the surface of the top metal denoted by Metal-3 in Fig. 5 should be designed to be rough. To make a rough surface on the top metal of the bond pad, the Metal-2 layer beneath the top metal in Fig. 6 is designed with relatively very small pieces (i.e., 5 $\mu$m $\times$ 5 $\mu$m) of varied regular or irregular layout test patterns on each single bond pad area for investigation. The electrical connection between Metal-3 and Metal-2 is performed by a plurality of via-plugs (named as Via2-3) with area (0.7 $\mu$m $\times$ 0.7 $\mu$m) smaller than the mentioned small Metal-2 pieces. This arrangement will cause a ragged surface of the Metal-2 layer in the cross sectional view of the bond pad structure. The interface layer dielectric deposited on the ragged Metal-2 then has an undulating surface. Therefore, the top metal deposited on the undulating interface layer dielectric is formed as a rough surface that is able to improve the stiffness of bond ball on the bond pad. Several experimental layout patterns of Metal-2 and Via2-3 have been designed and fabricated in a 0.6-$\mu$m single-poly triple-metal CMOS process to investigate their performance. It is expected that the top surface of the bond pad would be rough enough to improve the bond wire stiffness on the bond pad.

Fig. 7 shows the layout patterns of conventional bond pad. Figs. 8 and 9 show the experimental layout patterns and the photograph of the fabricated test chip, respectively. In Fig. 9, the pads denoted as "Conv" are all drawn with conventional bond pad layout patterns and treated as the reference set of this experiment. The other pads of Fig. 9, which are denoted as shapes A–C, D1–D9, E–L, are drawn with various experimental layout patterns as shown in Fig. 8. The experimental layout patterns of bond pads denoted as shapes D1–D9 are all designed as the shape D of Fig. 8, but with varied feature sizes of the small pieces of Metal-2 polygons and number of Via2-3 plugs located on each piece of Metal-2.

The bond pad with conventional layout structure can be more easily damaged by relatively higher bonding stress than the paling structure of the proposed layout method. In other words, bonding reliability robustness can be effectively improved while bonding stress is applied on the bond pad with proper layout designs.

The proposed layout design method can improve the bond wire reliability by only changing the layout patterns of the bond pad. In addition, the advantages of bond pad robustness to the bonding stress and low parasitic capacitance of bond pad are also achieved by using the same layout method. Without any extra fabrication cost, the yield of packaged IC products can be effectively improved.

## III. Experimental Results

Fig. 10(a) shows the measurement results of the wire pull test applied on the bond pads with conventional layout shape. Three silicon samples of the designed experimental chip were taken for this test. The horizontal axis of Fig. 10(a) is the relative location of pad with conventional layout shape on the test chip. As shown in Fig. 10(a), the measured pull-off sustaining forces applied on the bond pads, which have the same conventional layout shape but different locations of the test chip, have a wide-range variation. Moreover, the minimum value in Fig. 10(a) is 5.3 g, which is only a little greater than the required 5 g wire-pull sustaining ability listed on the test standard. The measurement results of the wire pull test on the bond pads with the proposed layout method in different experimental layout shapes are shown in Fig. 10(b). The horizontal axes of Fig. 10(b) and (c) indicate both the test layout shapes on the bond pads shown in Fig. 8 and the relative pad locations on the test chip. The minimum value in Fig. 10(b) is 6.1 g, which is greater than that of the conventional layout shape. Fig. 10(c) shows the mean values of the sustained pull-off forces measured from each pad locations of the three test chip samples. The minimum mean value of sustained pull-off force for pads with drawn experimental layout shapes is 6.7 g and occurred on the pad location of shape H of Fig. 8. This value is still greater than that of 6.47 g with the conventional layout shape.

Fig. 11 shows the measurement results of the ball shear test. The measurement results of the ball shear test on the pads with conventional and different experimental layout shapes are shown in Fig. 11(a) and (b), respectively. Fig. 11(c) shows the mean sustained forces of the ball shear tests measured from the three test chips. For bond pads with the conventional layout shape, the measured minimum and the mean value of sustained

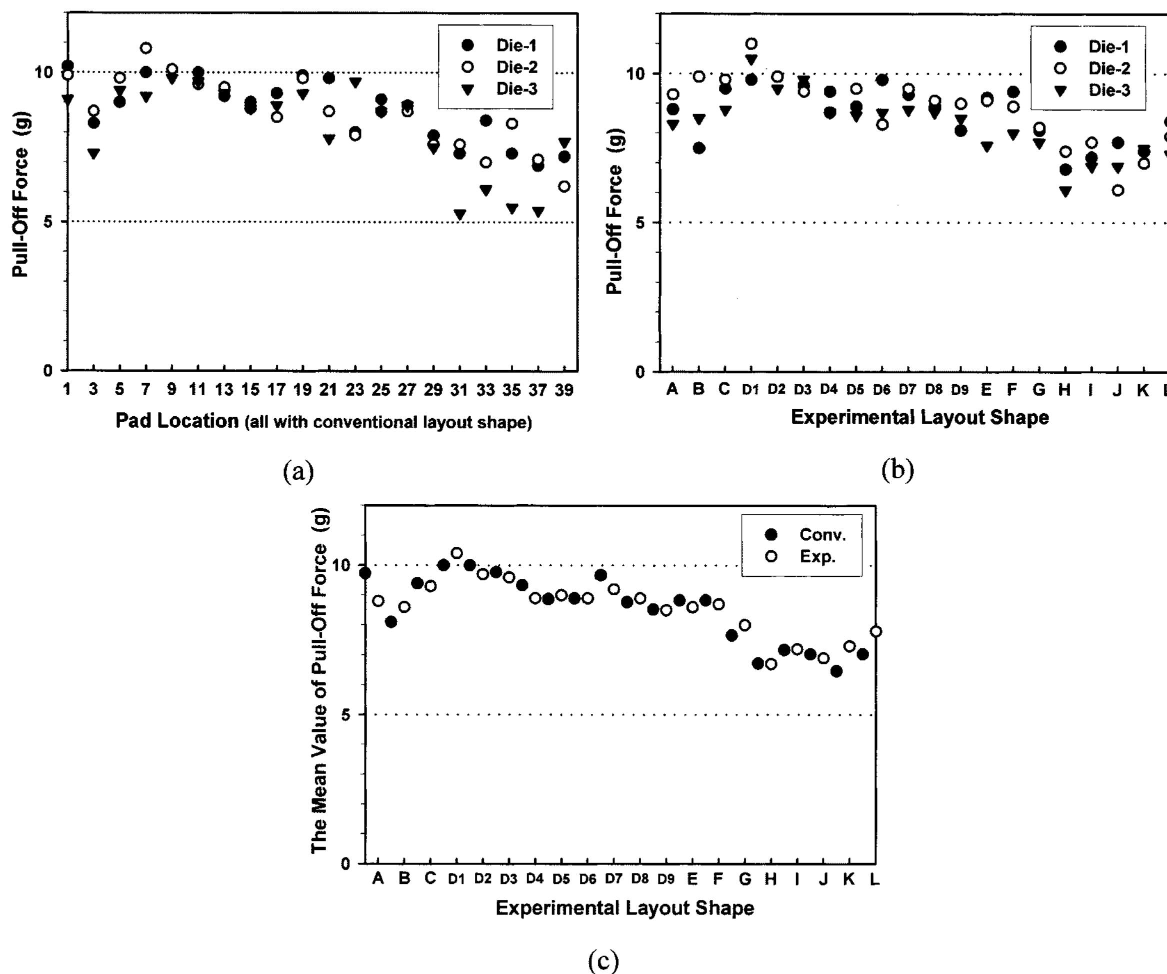



Fig. 10. Experimental results of wire pull test on: (a) the pads with conventional layout shape, (b) the pads with experimental layout shapes, and (c) the comparison of the mean values of the pull-off force between the conventional and experimental layout shapes. In the industrial standard of this test, bond wires have to stand at least 5 g pull-off force treated on them.

ball shear force applied on them are 31.5 g and 34.97 g which are shown in Fig. 11(a) and (c), respectively. Both of the values are greater than 30 g of the expected value in the test standard. On the other hand, for bond pads with various experimental layout shapes, the minimum sustained force of the ball shear test is 26.3 g shown in Fig. 11(b) with shape A layout patterns of Fig. 8. The minimum and maximum mean sustained forces of the ball shear test for the bond pads with experimental layout shapes shown in Fig. 11(c) are 31.2 g and 47.8 g with layout patterns of shape D9 and shape D1, respectively. The maximum mean value of pads with experimental layout shapes is much greater than the required value listed on the test standard.

Figs. 10 and 11 show that most of the bond pads with experimental layout shapes have better bond wire reliability than the ones with conventional layout shape under the wire pull test. However, the performances of lots of the bond pads with experimental layout shapes in ball shear test are not better than the ones with conventional layout shape. The experiment results are led to the conclusion that bond wire reliability of bond pad with proper layout design can be much better than the one of bond pads with conventional layout shape under both wire pull and ball shear tests. According to the results of the experiment, the experimental layout patterns of shape D1 shown in Fig. 8 is the most valuable design in the silicon test chip for both of the wire pull and ball shear tests. Fig. 12(a) shows the photograph of the shape D1 layout patterns in which the Metal-2 layer was shaped into pieces of small foursquare rectangular. Each piece is connected to Metal-3 through one Via2-3 plug. Fig. 12(b) shows the dimensions of the corresponding layout patterns.

## IV. Discussion

The pad with shape D1 layout patterns was discovered to have the highest sustaining ability of both the lift-off and the push-shear forces. Therefore, it might be meaningful to collect and analyze all the data obtained from the pads with similar foursquare rectangular metal-2 layout pieces but different feature sizes. By summarizing all the measurement data of the bond pads (which are named shapes D1–D9 in Fig. 8) with pieces of small foursquare rectangular, the obtained results are shown in Fig. 13. Fig. 13(a) shows the relationship between the wire-pull force sustaining ability and the varied side widths (or lengths) of Metal-2 layout patterns drawn on different bond pads. The applied pull-off forces are on the downward trend when the side width of the corresponding Metal-2 foursquare rectangle is getting larger. Similarly, Fig. 13(b) shows the relationship of

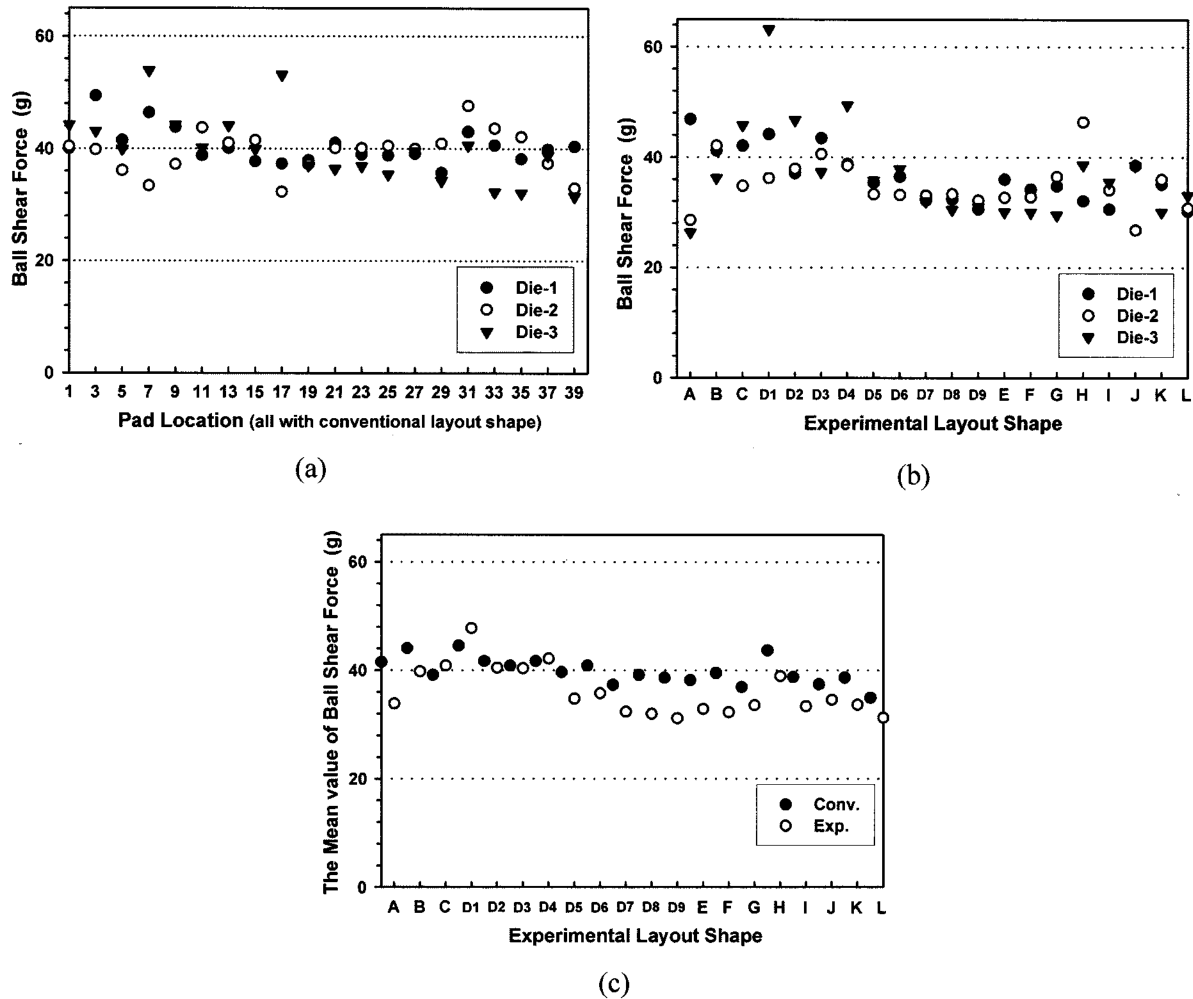


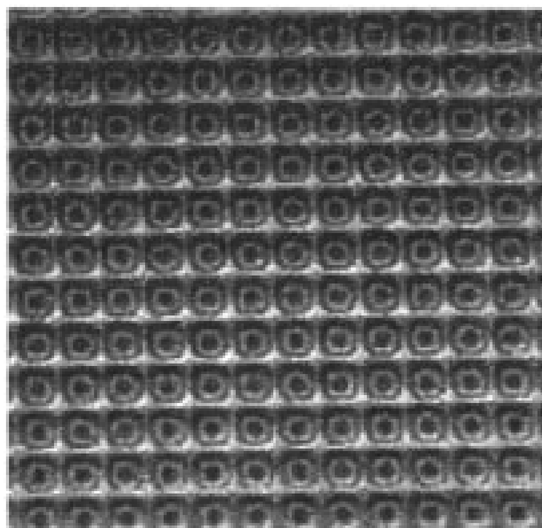

Fig. 11. Experimental results of ball shear test on (a) the pads with conventional layout shape, (b) the pads with experimental layout shapes, and (c) the comparison of the mean values of the ball shear force of the conventional and experimental layout shapes. In the industrial standard, the bond wires have to stand at least 30 g push-off force treated on them.

ball-shear forces applied on the bond pads versus different side widths (or lengths) of Metal-2 layout patterns drawn on different bond pads. Also, the applied pushed-off forces are on the downward trend when the side width of the corresponding Metal-2 foursquare rectangle is getting larger.

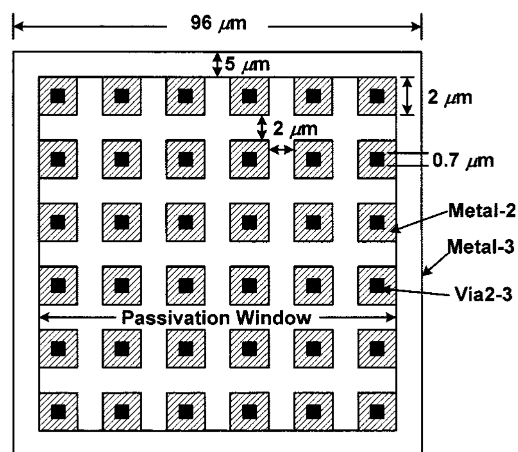
Intuitively, better bond-wire reliability for both of the wire pull and ball shear tests should be obtained if the layout pattern of the metal layer beneath the top bonding metal layer is designed in small pieces of polygons instead of the conventional flat plate. But, the aforementioned measurement results indicate that not all of the designed experimental layout shapes have a better bond wire reliability than the conventional one in both the wire pull and ball shear tests, except for the layout patterns of shape D1 of Fig. 8. This indicates that changed layout design on bond pad can improve the bond wire reliability for proper layout patterns. The experiment was then focused on test results of small pieces of Metal-2 (the metal layer beneath the top bonding metal layer) layout patterns on the bond pads with similar layout patterns of shape D1 in Fig. 8. The measurement data showed a downward trend for the sustained forces applied on them when the sizes of the Metal-2 foursquare rectangular layout patterns are getting larger.

Prior work demonstrated that the paling structures of via plugs, metal layer, or interface dielectric layers did help in the robustness of the bond pad for bonding stress, and paling structure were used for prevention of bond pad damage while pad bonding [6]–[10]. By using the proposed layout method on the bond pad, the metal layer and via plugs beneath the top metal layer are also shaped in a paling structure to take the mentioned advantage.

The performance of different layout shapes on bond pads have been fabricated and analyzed through experimentation. Packaging nowadays causes an important limitation in speed due to the following three reasons. The first one is the demand for higher clock frequencies in computers, the second is higher signal bit rates in data and communication systems due to the development of faster IC technologies; the third reason is the trend of both miniaturization of systems and higher I/O counts. Because less of the metal area on the bond pads is used while comparing the proposed layout method with the conventional pad structure, the capacitance of the bond pad can be effectively reduced by this new proposed layout design for improving bond pad reliability. This implies that the operating speed and circuit performance of IC product is therefore enhanced.

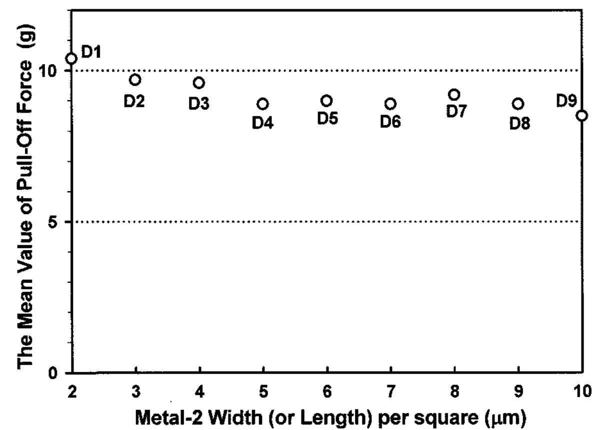


(a)

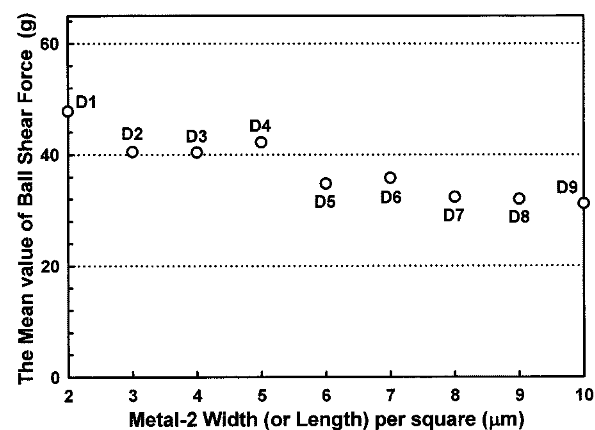



(b)

Fig. 12. (a) Photograph of the fabricated bond pad with the layout pattern of shape D1 and (b) the detailed dimensions of the layout pattern of shape D1.




(a)




(b)

Fig. 13. Dependence of the mean value of (a) wire-pull force and (b) ball-shear force on the size of Metal-2 area. The notations beside the hollow dots are the shape names of different experiment layout patterns.

## V. Conclusion

Without any extra fabrication cost in CMOS processes, a layout design method has been proposed to increase the bond wire reliability for packaged IC products. The metal layer beneath the top bonding metal layer is designed with regular or irregular layout patterns to make the surface of the top metal to be rough. This rough surface of the bond pad is effective in increasing the adhesion of the bond ball on the bond pad. Several experimental layout shapes have been designed and fabricated in a general CMOS process. The results show that the proposed layout method can effectively improve the bond wire reliability when the layout patterns are chosen properly. Just by changing layout patterns on the bond pad, the bond wire reliability can be effectively improved. Besides, the total area of the metal layers and via plugs of the proposed layout design method is less than that of the conventional bond pad layout. This indicates that the new proposed bond pad has a lower parasitic capacitance and a better circuit performance for high-frequency circuit application. By using the paling structure of the metal layers and via-plugs, the advantage of better bonding stress robustness is also achieved while using the proposed layout method on bond pads.

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