

# Investigation of Inductively Coupled Plasma Gate Oxide on Low Temperature Polycrystalline-Silicon TFTs

Chang-Ho Tseng, Ting-Kuo Chang, Fang-Tsun Chu, Jia-Min Shieh, Bau-Tong Dai, *Member, IEEE*, Huang-Chung Cheng, *Member, IEEE*, and Albert Chin, *Senior Member, IEEE*

**Abstract**—By optimizing the inductively coupled plasma (ICP) oxidation condition, a thin oxide of 10 nm has been grown at 350°C to achieve excellent gate oxide integrity of low leakage current  $< 5 \times 10^{-8}$  A/cm<sup>2</sup> (at 8 MV/cm), high breakdown field of 9.3 MV/cm and low interface trap density of  $1.5 \times 10^{11}$ /eV cm<sup>2</sup>. The superior performance poly-Si TFTs using such a thin ICP oxide were attained to achieve a high ON current of 110  $\mu$ A/ $\mu$ m at  $V_D = 1$  V and  $V_G = 5$  V and the high electron field effect mobility of 231 cm<sup>2</sup>/V · s.

**Index Terms**—Breakdown field, gate oxide, inductively coupled plasma (ICP), leakage current, thin-film transistor (TFT).

## I. INTRODUCTION

**D**IRECT oxidation to obtain thin and reliable gate oxide is the future scaling trend of poly-Si thin-film transistors (TFTs) [1]. To achieve this goal, plasma oxidation is one of the potential candidates due to its low process temperatures and good reliability as compared with furnace-formed gate oxides [2]–[7]. Among various plasma deposition methods, inductively coupled plasma (ICP) oxidation is very attractive due to its remote plasma source that has smaller plasma damage to gate-oxide during oxidation. In addition, ICP also has advantages of high radical concentrations, low plasma sheath voltage, and the capability of good uniformity over large area that is important for TFT manufacturing. Nevertheless, few studies of the ICP plasma oxide on the low temperature poly-Si TFTs were reported. In this letter, we report a thin 10-nm-thick gate oxide formed by low temperature ICP Ar/O<sub>2</sub> oxidation. By optimizing the oxidation condition, excellent gate oxide integrity of high breakdown field, low leakage current and small interface trap density are obtained simultaneously. High performance low temperature poly-Si TFTs are also achieved by using the very thin 10-nm ICP gate oxide. These results suggest the good possibility integrate ICP for next generation TFTs manufacturing with the thin gate oxide.

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C.-H. Tseng, T.-K. Chang, F.-T. Chu, H.-C. Cheng, and A. Chin are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

J.-M. Shieh and B.-T. Dai are with the National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

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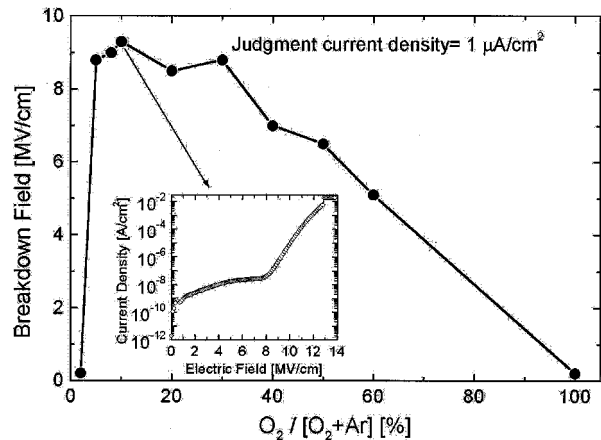


Fig. 1. The breakdown field of ICP oxide film as a function of O<sub>2</sub> percentage in Ar/O<sub>2</sub> gas mixtures. The total gas flow rate is 150 sccm. The breakdown field is determined at a current density of 1  $\mu$ A/cm<sup>2</sup>. The inserted figure is the J-E characteristics of gate oxide formed at optimized condition.

## II. EXPERIMENTS

The TFTs were fabricated on 4-in thermally oxidized Si wafers. We have first deposited amorphous Si on thermally oxidized Si with 100 nm thickness and crystallized by KrF excimer laser at 320 mJ/cm<sup>2</sup> energy density and 400°C substrate heating [8], [9]. Then, 10 nm-thick gate oxide was formed by ICP oxidation with oxygen and argon mixtures. The Ar/O<sub>2</sub> ICP oxidation was performed at 350°C substrate heating, 5 mtorr plasma pressure and 900 W RF power. To optimize the quality of gate-oxide, various O<sub>2</sub> percentage diluted by Ar were investigated with a fixed total flow rate of 150 sccm. For the comparison, gate oxide formed by PECVD TEOS was also studied with a larger 100 nm thickness and a higher 400 °C substrate heating. A 200 nm-thick poly-Si was deposited and patterned for gate electrode. A self-aligned P<sup>+</sup> implantation was performed at a  $5 \times 10^{15}$ /cm<sup>2</sup> dosage and 40 keV energy. Dopant activation was performed at 600 °C furnace annealing at N<sub>2</sub> ambient for 12 h after depositing a 400-nm oxide passivation layer. Then, 500 nm Al was deposited and patterned as electrode after contact hole definition. Sintering was carried out at 400 °C for 30 min. without using hydrogenation plasma to passivate grain boundary or interface.

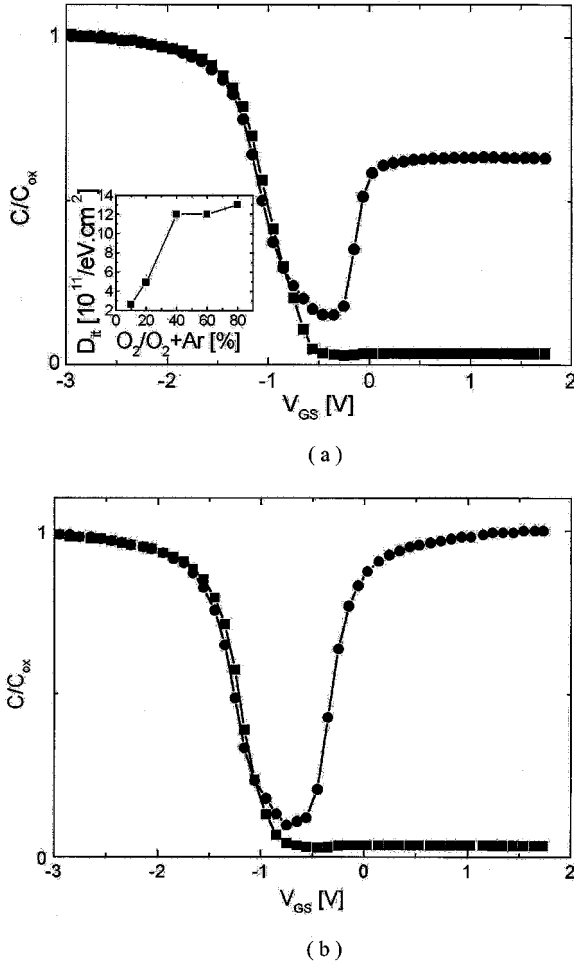


Fig. 2. Quasi-frequency and high-frequency (100 KHz)  $C-V$  characteristics of gate oxide formed with 10%  $O_2$  in gas mixtures (a) before and (b) after 600 °C furnace annealing for 6 h. The inserted figure shows the interface trap density dependence on  $O_2\%$  in gas mixtures.

### III. RESULTS AND DISCUSSION

Fig. 1 shows the breakdown field of gate oxide formed by ICP at various Ar/ $O_2$  ratios. The gate-oxide shows a general trend of improving breakdown field as decreasing  $O_2$  content in plasma gas mixtures except the lowest one. It is well known that noble gas can enhance the dissociation of reaction gas in plasma and the density of oxide. A maximum breakdown field as high as 9.3 MV/cm is achieved by ICP oxidation under an optimum  $O_2$  concentration of 10% in gas mixtures with an oxidation rate of 6.3 Å/min. We also inserted the measured  $J-E$  characteristics of gate oxide formed in the optimized condition. Good gate-oxide quality is evidenced from the small leakage current of  $< 5 \times 10^{-8}$  A/cm<sup>2</sup> at electric field of 8 MV/cm followed on F-N tunneling at higher field. The small pre-F-N tunneling current suggests the low trap density inside the oxide for trap-assisted tunneling, which also suggests high quality oxide can be formed by ICP [10]–[12].

We further used capacitance–voltage ( $C-V$ ) measurement to evaluate the gate oxide quality. Figs. 2(a) and 2(b) show the quasi-static and high frequency  $C-V$  characteristics of ICP oxide formed with 10%  $O_2$  in gas mixtures before and after 600 °C post annealing for 6 h used for implantation activation. The

TABLE I  
SUMMARY OF DEVICE CHARACTERISTICS OF MOS CAPACITOR AND POLY-Si TFTS. THE BREAKDOWN FIELD OF MOS CAPACITOR IS DEFINED AT  $1 \mu\text{A}/\text{cm}^2$  LEAKAGE CURRENT DENSITY. THE THRESHOLD VOLTAGE WAS DEFINED AT  $I_D$  OF  $10 \text{ nA} \times W/L$  AND  $V_D$  OF 1 V. THE  $I_{ON}$  AND  $I_{OFF}$  CURRENTS ARE MEASURED AT  $V_G = 5 \text{ V}$  AND  $V_D = 1 \text{ V}$ . THE MAXIMUM FIELD EFFECT MOBILITY WAS MEASURED AT  $V_D = 0.1 \text{ V}$

	MOS capacitor		Poly-Si TFT ( $L = 2 \mu\text{m}$ )		
	As deposited	After 600°C, 6 hrs annealing		PECVD TEOS oxide TFT	ICP Ar/ $O_2$ plasma oxide TFT
Flat band Voltage (V)	-0.64	-0.98	Threshold Voltage (V)	-1.35	0.42
Interface trap state density ( $1/\text{eV}\cdot\text{cm}^2$ )	$2.6 \times 10^{11}$	$1.5 \times 10^{11}$	Sub-threshold Swing (V/dec.)	0.626	0.207
Breakdown Field (MV/cm)	9.3	9.0	Maximum Field effect mobility ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	58.4	231
Oxide charge density ( $1/\text{cm}^2$ )	$-4.2 \times 10^{10}$	$5.6 \times 10^{11}$	$I_{ON}/W$ ( $\mu\text{A}/\mu\text{m}$ )	2.5	110
Doping concentration ( $N_A$ )( $1/\text{cm}^3$ )	$2.5 \times 10^{15}$	$2.8 \times 10^{15}$	$I_{ON}/I_{OFF}$ ( $\times 10^7$ )	0.89	1.24

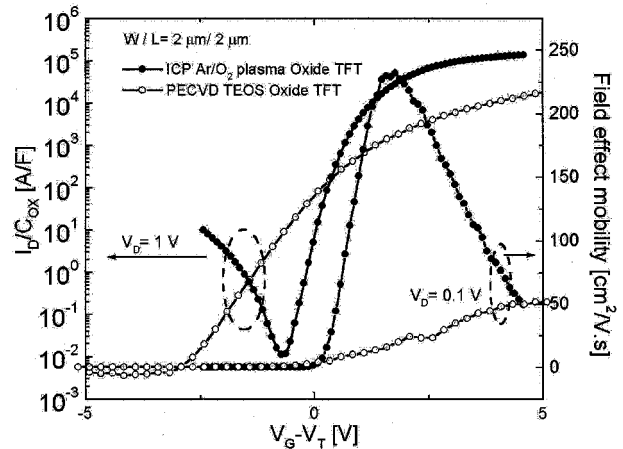


Fig. 3.  $I_D/C_{OX}$  and  $(V_G - V_T)$  transfer characteristics of poly-Si TFTs with ICP Ar/ $O_2$  gate oxide and PECVD TEOS oxide.

obtained oxide charge density and interface trap density from  $C-V$  curves are summarized in Table I. The ICP oxide shows a small interface trap density of  $2.6 \times 10^{11}/\text{eV} \cdot \text{cm}^2$  for as-grown oxide; the annealing has a small effect on interface trap density improvement. These results indicate good oxide interface can be achieved by ICP oxidation and exhibit as good interface quality as previously reported Kr/ $O_2$  plasma oxide [7]. However, as shown in the insert figure, the interface trap density increases rapidly as increasing  $O_2$  content in gas mixtures that is consistent with the decreasing trend of breakdown field shown in Fig. 1. The achieved good gate oxide integrity [10]–[12] of low interface trap density, high breakdown electric field and the low leakage current of ICP Ar/ $O_2$  oxide are promising for further scaling down the gate oxide thickness in low temperature poly-Si TFTs [1]. It is noticed that the inversion capacitance in Fig. 2(a) is less than the value under accumulation. Similar result is also reported in the literature [13] and is attributed to the effect of minority carrier generation rate. Because the oxygen plasma may damage the underneath Si and create traps, this may

reduce the minority carrier generation rate and gives lower inversion capacitance.

Fig. 3 shows the  $I_D/C_{ox}$  and  $(V_G - V_T)$  transfer characteristics of poly-Si TFTs with either 10 nm ICP Ar/O<sub>2</sub> gate oxide or 100-nm PECVD TEOS oxide. The important device parameters are listed again in Table I for comparison. It notices that the oxide thickness is normalized even though the PECVD oxide requires large thickness to achieve good dielectric integrity. The TFT formed by ICP Ar/O<sub>2</sub> oxide exhibits high ON current of 110  $\mu\text{A}/\mu\text{m}$ , low sub-threshold swing of 0.207 V/dec and high electron field effect mobility of 231  $\text{cm}^2/\text{V} \cdot \text{s}$  that demonstrate the excellent TFT device performance and are better than PECVD oxide formed TFT. The improved mobility by ICP oxidation may be caused by the high density O<sub>2</sub> plasma oxidation to eliminate the dangling bonds in the polycrystal grain [14]. The good TFT device performance using such a thin 10-nm ICP oxide indicates the high possibility to integrate ICP oxidation for future TFT manufacturing.

#### IV. CONCLUSIONS

We have investigated the ICP Ar/O<sub>2</sub> oxide for TFT application. Good gate-oxide integrity of low-leakage current, high breakdown field and low interface trap density are obtained using 10-nm ICP Ar/O<sub>2</sub> oxide. High performance poly-Si TFTs were also achieved by using ICP Ar/O<sub>2</sub> oxide with low threshold voltage and high electron-field effect mobility. Such the high performance poly-Si TFTs are promising for the application of integrated circuits on LCD panel.

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